# INSTRUCTION MANUAL

# MVDS
# RC-1
# MT-3
# B-SERIES FM TRANSMITTER DIAGNOSTICS AND REMOTE CONTROL OPTIONS

April, 1996

IM No. 597-0114

BROADCAST ELECTRONICS, INC.

# IMPORTANT INFORMATION

## EQUIPMENT LOST OR DAMAGED IN TRANSIT

When delivering the equipment to you, the truck driver or carrier's agent will present a receipt for your signature. Do not sign it until you have (a) inspected the containers for visible signs of damage and (b) counted the containers and compared with the amount shown on the shipping papers. If a shortage or evidence of damage is noted, insist that notation to that effect be made on the shipping papers before you sign them.

Further, after receiving the equipment, unpack it and inspect thoroughly for concealed damage. If concealed damage is discovered, immediately notify the carrier, confirming the notification in writing, and secure an inspection report. This item should be unpacked and inspected for damage WITHIN 15 DAYS after receipt. Claims for loss or damage will not be honored without proper notification of inspection by the carrier.

## TECHNICAL ASSISTANCE AND REPAIR SERVICE

Technical assistance is available from Broadcast Electronics by letter or prepaid telephone or telegram. Equipment requiring repair or overhaul should be sent by common carrier, prepaid, insured and well protected. Do not mail equipment. We can assume no liability for inbound damage, and necessary repairs become the obligation of the shipper. Prior arrangement is necessary. Contact Customer Service Department for a Return Authorization.

## FOR TECHNICAL ASSISTANCE DURING 8:00 AM TO 5:00 PM CENTRAL TIME

Digital Product Customer Service – Phone (217) 224–9600

RF/Studio Product Customer Service – Phone (217) 224–9617

## FOR TECHNICAL ASSISTANCE DURING NON–BUSINESS HOURS

Phone (217) 224–9600 Customer Service

## FOR DIGITAL PRODUCTS BULLETIN BOARD SERVICE

Phone (217) 224–1926

## WARRANTY ADJUSTMENT

Broadcast Electronics, Inc. warranty is included in the Terms and Conditions of Sale. In the event of a warranty claim, replacement or repair parts will be supplied F.O.B. factory. At the discretion of Broadcast Electronics, the customer may be required to return the defective part or equipment to Broadcast Electronics, Inc. F.O.B. Quincy, Illinois. Warranty replacements of defective merchandise will be billed to your account. This billing will be cleared by a credit issued upon return of the defective item.

## RETURN, REPAIR AND EXCHANGES

Do not return any merchandise without our written approval and Return Authorization. We will provide special shipping instructions and a code number that will assure proper handling and prompt issuance of credit. Please furnish complete details as to circumstances and reasons when requesting return of merchandise. All returned merchandise must be sent freight prepaid and properly insured by the customer.

## REPLACEMENT PARTS

Emergency and Warranty Replacement Parts may be ordered from the address below. Be sure to include equipment model and serial number and part description and part number. Non–Emergency Replacement Parts may be ordered directly from the Broadcast Electronics stock room by Fax at the number shown below.

**EMERGENCY AND WARRANTY REPLACEMENT PARTS**

Broadcast Electronics, Inc.
4100 N. 24th St. P.O. BOX 3606
Quincy, Illinois 62305
Tel: (217) 224–9600 Digital Products (8 AM to 5 PM Central Time)
Tel: (217) 224–9617 RF/Studio Products (8 AM to 5 PM Central Time)
Tel: (217) 224–9600 (Non–Business Hours)
Telex: 25–0142
Fax: (217) 224–9607

**NON–EMERGENCY REPLACEMENT PARTS**

FAX (217) 224–9609

## PROPRIETARY NOTICE

This document contains proprietary data of Broadcast Electronics, Inc. No disclosure, reproduction, or use of any part thereof may be made except by prior written permission.

## MODIFICATIONS

Broadcast Electronics, Inc. reserves the right to modify the design and specifications of the equipment in this manual without notice. Any modifications shall not adversely affect performance of the equipment so modified.

# SCOPE OF MANUAL

This manual consists of three parts providing the following information for the Broadcast Electronics optional RF equipment.

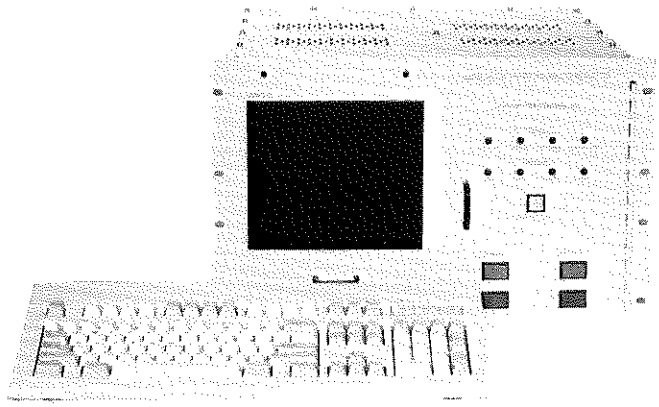
**PART I –** Contains information relative to the installation, operation, and maintenance of the optional MVDS (microprocessor video diagnostics system). MVDS continuously monitors and displays major transmitter operating parameters and diagnostics.

**PART II –** Contains information relative to the installation and operation of the optional RC–1 MVDS remote control system. RC–1 operates in association with the MVDS diagnostic system to provide control of one MVDS equipped FM transmitter from the studio site.

**PART III –** Contains information relative to the installation operation and maintenance of the optional MT–3 multiple transmitter interface. In conjunction with MVDS and RC–1, MT–3 provides control of two MVDS equipped FM transmitters and one transmitter unequipped with MVDS from the studio site.

© Broadcast Electronics 1990
ALL RIGHTS RESERVED
Printed in the U.S.A.

# TECHNICAL MANUAL
# MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM OPTION



COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597-0036-1

| PART NUMBER | DESCRIPTION |
|---|---|
| 909-0091-014 | OPTIONAL MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM, FACTORY INSTALLATION, FM-30B TRANSMITTER. |
| 909-0091-024 | OPTIONAL MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM, FACTORY INSTALLATION, FM-3.5B TRANSMITTER. |
| 909-0091-034 | OPTIONAL MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM, FACTORY INSTALLATION, FM-5B TRANSMITTER. |
| 909-0091-054 | OPTIONAL MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM, FACTORY INSTALLATION, FM-10B TRANSMITTER. |
| 909-0091-064 | OPTIONAL MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM, FACTORY INSTALLATION, FM-35B TRANSMITTER. |
| 909-0091-074 | OPTIONAL MICROPROCESSOR VIDEO DIAGNOSTIC SYSTEM, FACTORY INSTALLATION, FM-20B TRANSMITTER. |

BROADCAST ELECTRONICS INC

## SOFTWARE KITS

| | |
|---|---|
| 979–0091–014 | KIT OF 24 EPROMS WHICH CONTAIN THE MVDS SOFTWARE INSTRUCTIONS FOR THE FM–30B TRANSMITTER. |
| 979–0091–024 | KIT OF 24 EPROMS WHICH CONTAIN THE MVDS SOFTWARE INSTRUCTIONS FOR THE FM–3.5B TRANSMITTER. |
| 979–0091–034 | KIT OF 24 EPROMS WHICH CONTAIN THE MVDS SOFTWARE INSTRUCTIONS FOR THE FM–5B TRANSMITTER. |
| 979–0091–054 | KIT OF 24 EPROMS WHICH CONTAIN THE MVDS SOFTWARE INSTRUCTIONS FOR THE FM–10B TRANSMITTER. |
| 979–0091–064 | KIT OF 24 EPROMS WHICH CONTAIN THE MVDS SOFTWARE INSTRUCTIONS FOR THE FM–35B TRANSMITTER. |
| 979–0091–074 | KIT OF 24 EPROMS WHICH CONTAIN THE MVDS SOFTWARE INSTRUCTIONS FOR THE FM–20B TRANSMITTER. |

# TABLE OF CONTENTS


| PARAGRAPH | DESCRIPTION | PAGE NO. |
|---|---|---|
| **SECTION I** | **GENERAL INFORMATION** | |
| 1–1 | Introduction | 1–1 |
| 1–3 | Equipment Description | 1–1 |
| 1–11 | Options and Accessories | 1–1 |
| 1–13 | Equipment Specifications | 1–2 |
| **SECTION II** | **INSTALLATION** | |
| 2–1 | Introduction | 2–1 |
| 2–3 | Unpacking | 2–1 |
| 2–6 | Installation | 2–1 |
| 2–7 | MVDS Switch and Jumper Programming Check | 2–1 |
| 2–11 | Video Monitor and Circuit Board Installation | 2–1 |
| 2–15 | Communication Equipment Connections | 2–5 |
| 2–16 | Keyboard | 2–5 |
| 2–17 | Logging Devices | 2–5 |
| 2–24 | Cable Routing | 2–8 |
| 2–25 | External Video Output | 2–8 |
| 2–26 | Status Inputs | 2–8 |
| 2–29 | AC Power Connection | 2–9 |
| **SECTION III** | **OPERATION** | |
| 3–1 | Introduction | 3–1 |
| 3–3 | Initial Operation | 3–1 |
| 3–4 | Keyboard | 3–1 |
| 3–6 | Turn–On | 3–1 |
| 3–10 | Normal Display Screen | 3–1 |
| 3–27 | Customer Configuration Screen | 3–5 |
| 3–94 | Transmitter Operation With MVDS | 3–10 |
| 3–96 | Operation Of The Normal Display Screen | 3–10 |
| 3–100 | Overloads | 3–10 |
| 3–101 | Tolerance Highlighting | 3–11 |
| 3–102 | Non–Volatile Memory Monitoring | 3–12 |
| 3–103 | Operation Of The Bar Graph Screen | 3–12 |
| 3–105 | Procedure | 3–12 |
| 3–109 | MPU/Digital Controller Control | 3–15 |
| 3–113 | Transmitter Logs | 3–15 |
| 3–115 | Transmitter Operation Without MVDS | 3–16 |
| **SECTION IV** | **THEORY OF OPERATION** | |
| 4–1 | Introduction | 4–1 |
| 4–3 | General Description | 4–1 |
| 4–5 | System Components | 4–1 |
| 4–7 | 64K Memory Circuit Board | 4–1 |
| 4–8 | Analog/Digital Circuit Board | 4–1 |
| 4–9 | Input/Output Circuit Board | 4–1 |
| 4–10 | CPU Circuit Board | 4–2 |

| PARAGRAPH | DESCRIPTION | PAGE NO. |
|---|---|---|
| 4–11 | VDM Circuit Board | 4–2 |
| 4–12 | EMI Filter Circuit Board | 4–2 |
| 4–13 | Controller Circuit Board | 4–2 |
| 4–14 | Motherboard | 4–2 |
| 4–15 | System Keyboard and Video Monitor | 4–2 |
| 4–16 | Power Supply | 4–2 |
| 4–17 | System Communication | 4–2 |
| 4–24 | Detailed Description | 4–5 |
| 4–25 | 64K Memory Circuit Board | 4–5 |
| 4–26 | General | 4–5 |
| 4–31 | Operation | 4–5 |
| 4–36 | Analog/Digital Circuit Board | 4–6 |
| 4–37 | General | 4–6 |
| 4–38 | Operation | 4–6 |
| 4–46 | Input/Output Circuit Board | 4–11 |
| 4–47 | General | 4–11 |
| 4–48 | Operation | 4–11 |
| 4–69 | Central Processing Unit Circuit Board (CPU) | 4–15 |
| 4–71 | Operation | 4–17 |
| 4–84 | Video Monitor Display Circuit Board | 4–19 |
| 4–85 | General | 4–19 |
| 4–88 | Operation | 4–19 |
| **SECTION V** | **MVDS MAINTENANCE** | |
| 5–1 | Introduction | 5–1 |
| 5–3 | Safety Considerations | 5–1 |
| 5–6 | Maintenance | 5–1 |
| 5–7 | Preventative | 5–1 |
| 5–9 | Adjustments | 5–1 |
| 5–11 | Analog/Digital Circuit Board Adjustments | 5–1 |
| 5–12 | PA Forward Power, Plate Voltage, and Plate Current Digital Display Calibrate (R43, R67, R94) | 5–1 |
| 5–19 | Analog/Digital Converter Offset Voltage Adjust (R85, R86, R87) | 5–2 |
| 5–20 | Troubleshooting | 5–3 |
| 5–26 | Component Replacement | 5–4 |
| **SECTION VI** | **PARTS LIST** | |
| 6–1 | Introduction | 6–1 |
| **SECTION VII** | **MVDS DRAWINGS** | |
| 7–1 | Introduction | 7–1 |
| **APPENDIX A** | **MVDS MANUFACTURERS DATA** | |
| A–1 | Introduction | A–1 |

# LIST OF ILLUSTRATIONS


| FIGURE | DESCRIPTION | PAGE NO. |
|---|---|---|
| 2–1 | Video Display Module Jumper Programming | 2–2 |
| 2–2 | CPU Circuit Board Switch Programming | 2–2 |
| 2–3 | 64K Memory Circuit Board Jumper Programming | 2–3 |
| 2–4 | Analog/Digital Circuit Board Jumper Programming | 2–3 |
| 2–5 | Input/Output Circuit Board Jumper Programming | 2–4 |
| 2–6 | MVDS Video Monitor Switch Programming | 2–5 |
| 2–7 | Controller Cabinet | 2–6 |
| 2–8 | Typical Logging Device Applications | 2–7 |
| 2–9 | Rear–Panel of Controller Cabinet | 2–9 |
| 3–1 | Keyboard | 3–2 |
| 3–2 | Normal Display Screen | 3–4 |
| 3–3 | Customer Configuration Screen | 3–6 |
| 3–4 | Overload Display | 3–11 |
| 3–5 | Tolerance Highlighting | 3–11 |
| 3–6 | FM–20B, FM–30B and FM–35B Bar Graph Display Screen | 3–13 |
| 3–7 | FM–3.5B, FM–5B/5BS, and FM–10B Bar Graph Display Screen | 3–14 |
| 3–8 | Bar Graph Screen Highlighting | 3–15 |
| 4–1 | MVDS Block Diagram | 4–3 |
| 4–2 | 64K Memory Circuit Board Block Diagram | 4–7 |
| 4–3 | Analog/Digital Circuit Board Block Diagram | 4–9 |
| 4–4 | Input/Output Circuit Simplified Schematic | 4–13 |
| 4–5 | CPU Circuit Board Block Diagram | 4–16 |
| 4–6 | VDM Circuit Board Block Diagram | 4–20 |
| 5–1 | Analog/Digital Circuit Board Controls | 5–2 |


# LIST OF TABLES


| TABLE NO. | DESCRIPTION | PAGE NO. |
|---|---|---|
| 1–1 | System Characteristics | 1–2 |
| 1–2 | Physical Characteristics | 1–3 |
| 3–1 | Keyboard Commands | 3–3 |
| 3–2 | Normal Dislay Screen | 3–5 |
| 3–3 | Customer Configuration Screen | 3–7 |
| 5–1 | MVDS Troubleshooting | 5–3 |
| 6–1 | Replaceable Parts List Index | 6–1 |


This equipment is a Class A (or Class B) digital apparatus which complies with the Radio Interference Regulations, CRC c.1374.

# SECTION I
# GENERAL INFORMATION

## 1–1. INTRODUCTION.

1–2. Information presented by this section provides a general description of the Broadcast Electronics Microprocessor Video Diagnostic System and lists equipment specifications.

## 1–3. EQUIPMENT DESCRIPTION.

1–4. The Microprocessor Video Diagnostic System (MVDS) is a microprocessor based video display system which continuously monitors and displays all major transmitter parameters. The system contains five plug–in circuit boards, a power supply, a filter circuit board, a video monitor, and a system keyboard. All components are located within the controller cabinet and operate independently of the standard transmitter digital controller.

1–5. Transmitter parameter limits are selected by the operator and entered into the MVDS through the system keyboard. Transmitter limits and parameter status information are presented on three video display screens: the customer configuration screen, the normal display screen, and the bar–graph screen.

1–6. The customer configuration screen displays transmitter parameter limit information. Access to the screen is protected by an eight–digit password. Values are entered by the operator which establish the operating parameters for the transmitter. The values are stored in non–volatile memory for protection during a power failure.

1–7. The normal display screen displays the status of the transmitter parameters. Overloads and out–of–limit parameters are displayed in reverse video with a diagnosis of the transmitter condition. With this information, the operator is directed to a specific problem for troubleshooting.

1–8. The bar–graph screen displays selected transmitter parameters in a bar–graph and digital format. Out–of–limit parameters are displayed in reverse video for immediate recognition. The display can be used to tune the transmitter for overall efficiency or to check the transmitter operating parameters quickly.

1–9. A printed copy of the information presented on the normal display screen may be obtained through the MVDS logging system. Transmitter logs may be requested at the keyboard by the operator or provided automatically by the MVDS. A parallel and a serial port are provided for log printers. Logs may be transmitted through a modem or connected to an SCA generator for remote reception.

1–10. The microprocessor within the MVDS provides the transmitter with an additional independent and redundant controller. When the transmitter is operated with the microprocessor, most transmitter control operations as well as the diagnostic and display functions are performed by the MVDS. If the microprocessor is disabled, control will be automatically returned to the transmitter digital controller.

## 1–11. OPTIONS AND ACCESSORIES.

1–12. The following is a list of the available options for the MVDS system.

| MODEL NO. | PART NUMBER | DESCRIPTION |
|---|---|---|
| RC–1 | 909–0122–0XX | OPTIONAL MVDS REMOTE CONTROL SYSTEM. |
| MT–3 | 909–0127–004 | OPTIONAL MULTIPLE TRANSMITTER INTERFACE. |

## 1–13. EQUIPMENT SPECIFICATIONS.

1–14. Refer to Table 1–1 for the system characteristics or Table 1–2 for physical characteristics of the Microprocessor Video Diagnostics System.

**TABLE 1–1. SYSTEM CHARACTERISTICS**

| PARAMETER | DESCRIPTION |
|---|---|
| POWER SUPPLY | Power One model HCCAA–60W–A. Completely independent of transmitter controller. |
| NON–VOLATILE MEMORY | 2 k bytes. Storage of customer configuration screen data. |
| BATTERY SUPPORTED RANDOM ACCESS MEMORY | 50 bytes. Storage of Clock and Overload data. |
| FILTERING | EMI filtering for all required communication signals to/from the logging devices. |
| COMMUNICATION PORTS | One parallel port. Three serial ports with selec table baud rates. |
| EXTERNAL VIDEO CONNECTION AND DISPLAY | One external video connection located on the rear–panel of the controller cabinet. The Monitor can be extended a maximum of 1000 feet using RG59U cable terminated into 75 Ohms. |
| MVDS DISPLAY ACCURACY: | |
| PLATE VOLTAGE | Within 0.5% of full scale. |
| PLATE CURRENT | Within 1.4% of full scale. |
| FORWARD POWER | Within 1.0% of full scale of calibrated power meter. |

## TABLE 1–2. PHYSICAL CHARACTERISTICS

| PARAMETER | DESCRIPTION |
|---|---|
| AMBIENT TEMPERATURE RANGE | +14F to 122F (–10C to +50C). |
| MAXIMUM ALTITUDE: | |
| 50 Hz Models | 0 to 7500 feet above sea level (0 to 2286 meters). |
| 60 Hz Models | 0 to 10,000 feet above sea level (0 to 3048 meters). |
| MAXIMUM HUMIDITY | 95%, Non–Condensing. |
| DIMENSIONS: | |
| WIDTH | 19 Inches (48.26 cm). |
| HEIGHT | 12.2 Inches (30.99 cm). |
| DEPTH | 18.6 Inches (47.24 cm). |
| WEIGHT: | |
| MVDS OPTION | 33 Pounds (14.9 kg). |
| MVDS OPTION WITH CONTROLLER | 54 Pounds (24.3 kg). |
| COOLING AIR REQUIREMENTS | 30 Cubic Feet per minute (0.85 m#/min). |

# SECTION II
# INSTALLATION

## 2–1. INTRODUCTION.

2–2. This section contains information required for the installation of the Broadcast Electronics Microprocessor Video Diagnostics System (MVDS).

## 2–3. UNPACKING.

2–4. The equipment becomes the property of the customer when the equipment is delivered to the carrier. Carefully unpack the monitor, keyboard, and the MVDS circuit boards. Perform a visual inspection to determine that no apparent damage has been incurred during shipment. All shipping materials should be retained until it is determined that the unit has not been damaged. Claims for damaged equipment must be promptly filed with the carrier or the carrier may not accept the claim.

2–5. The contents of the shipment should be as indicated on the packing list. If the contents are incomplete, or if the unit is damaged electrically or mechanically, notify both the carrier and Broadcast Electronics, Inc.

## 2–6. INSTALLATION.

*NOTE* *THE FOLLOWING PROCEDURE, THE MVDS CLOCK BATTERY SWITCH ON THE INPUT/OUTPUT CIRCUIT BOARD MUST BE OPERATED TO ON.*

*NOTE*

### 2–7. MVDS SWITCH AND JUMPER PROGRAMMING CHECK.

2–8. Each MVDS is programmed, operated, and tested at the factory prior to shipping. The following programming check assures the system circuit board jumpers have not become dislodged or the switches changed during shipment.

2–9. Refer to Figures 2–1 through 2–6 and ensure the system jumpers and switches are correctly positioned.

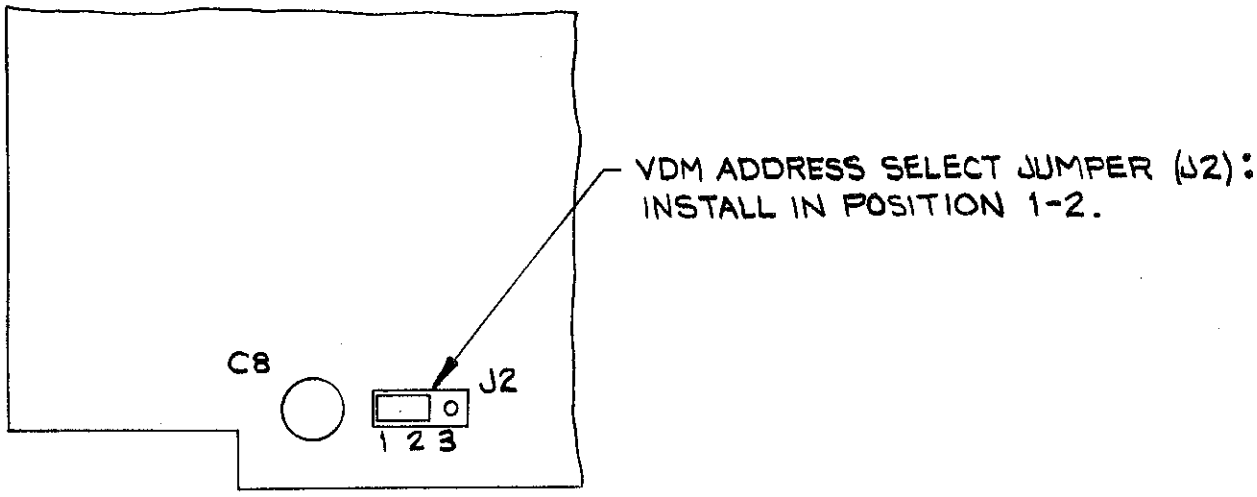
2–10. Refer to PART I, SECTION II of the applicable transmitter manual and ensure the controller circuit board jumpers are correctly positioned.

### 2–11. VIDEO MONITOR AND CIRCUIT BOARD INSTALLATION.

*WARNING* *ENSURE ALL TRANSMITTER PRIMARY POWER IS DISCONNECTED BEFORE PROCEEDING.*

*WARNING*

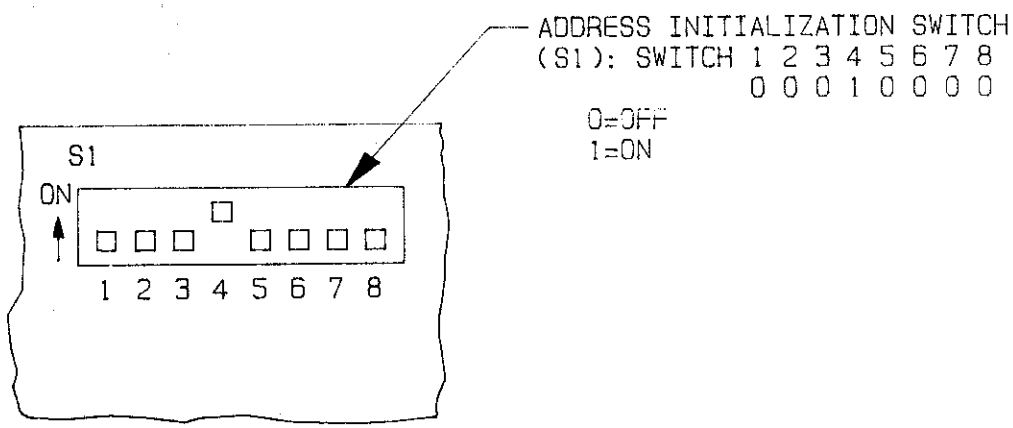
2–12. Ensure all transmitter primary power is disconnected before proceeding.




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597-0036-3

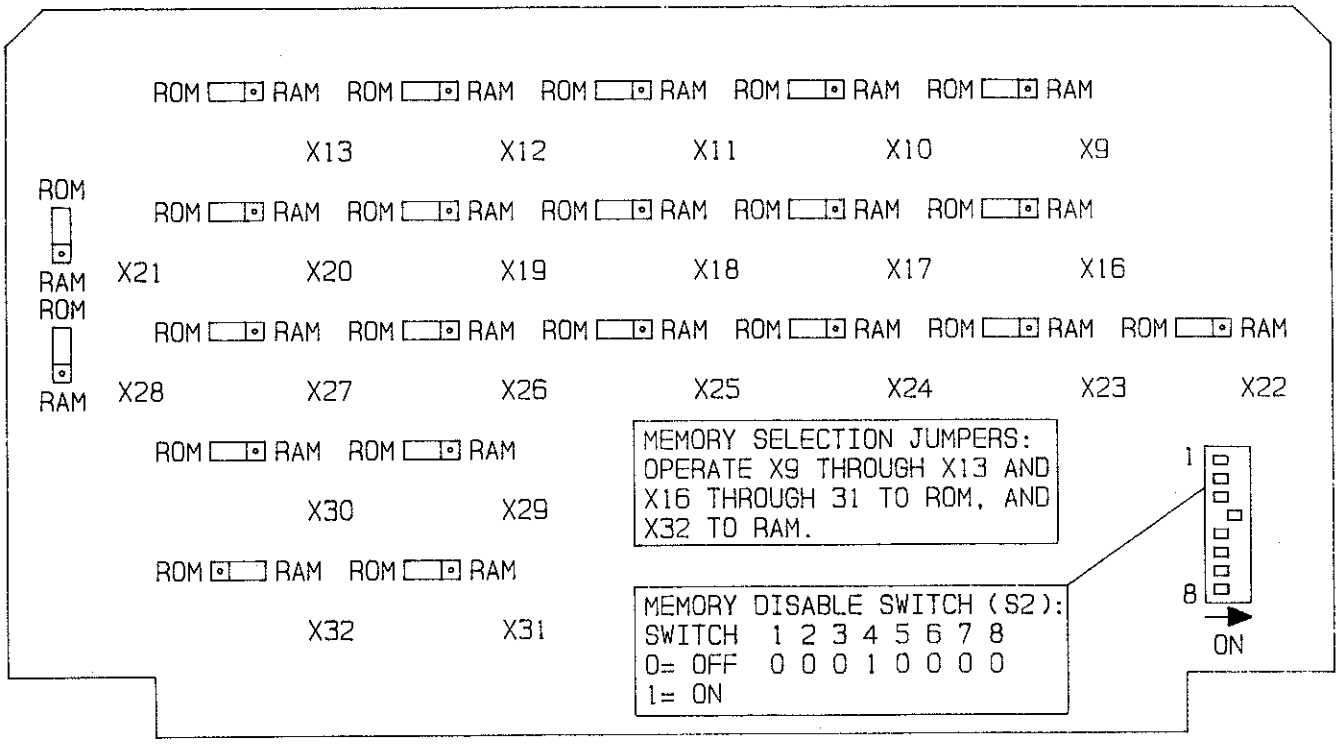
**FIGURE 2-1. VIDEO DISPLAY MODULE JUMPER PROGRAMMING**




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

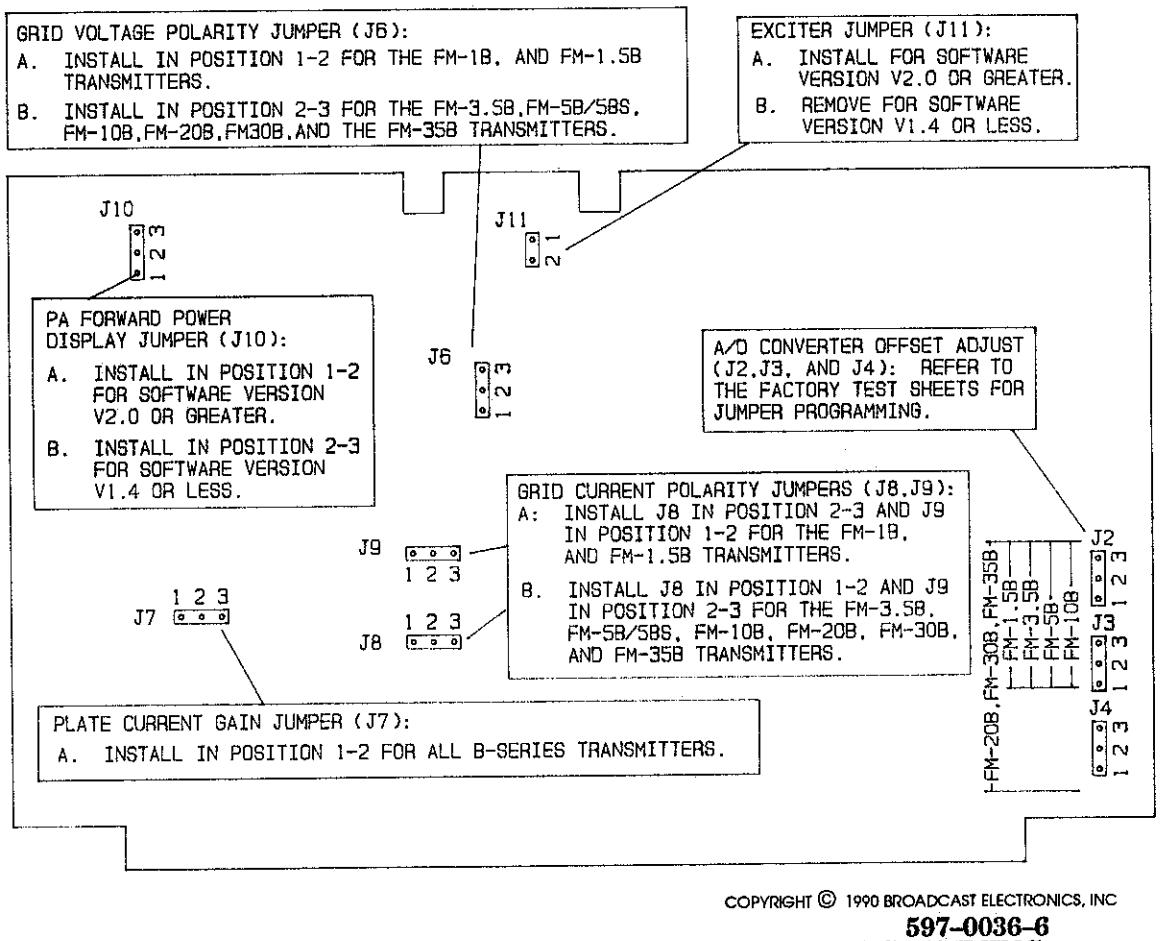
597-0036-4

**FIGURE 2-2. CPU CIRCUIT BOARD SWITCH PROGRAMMING**



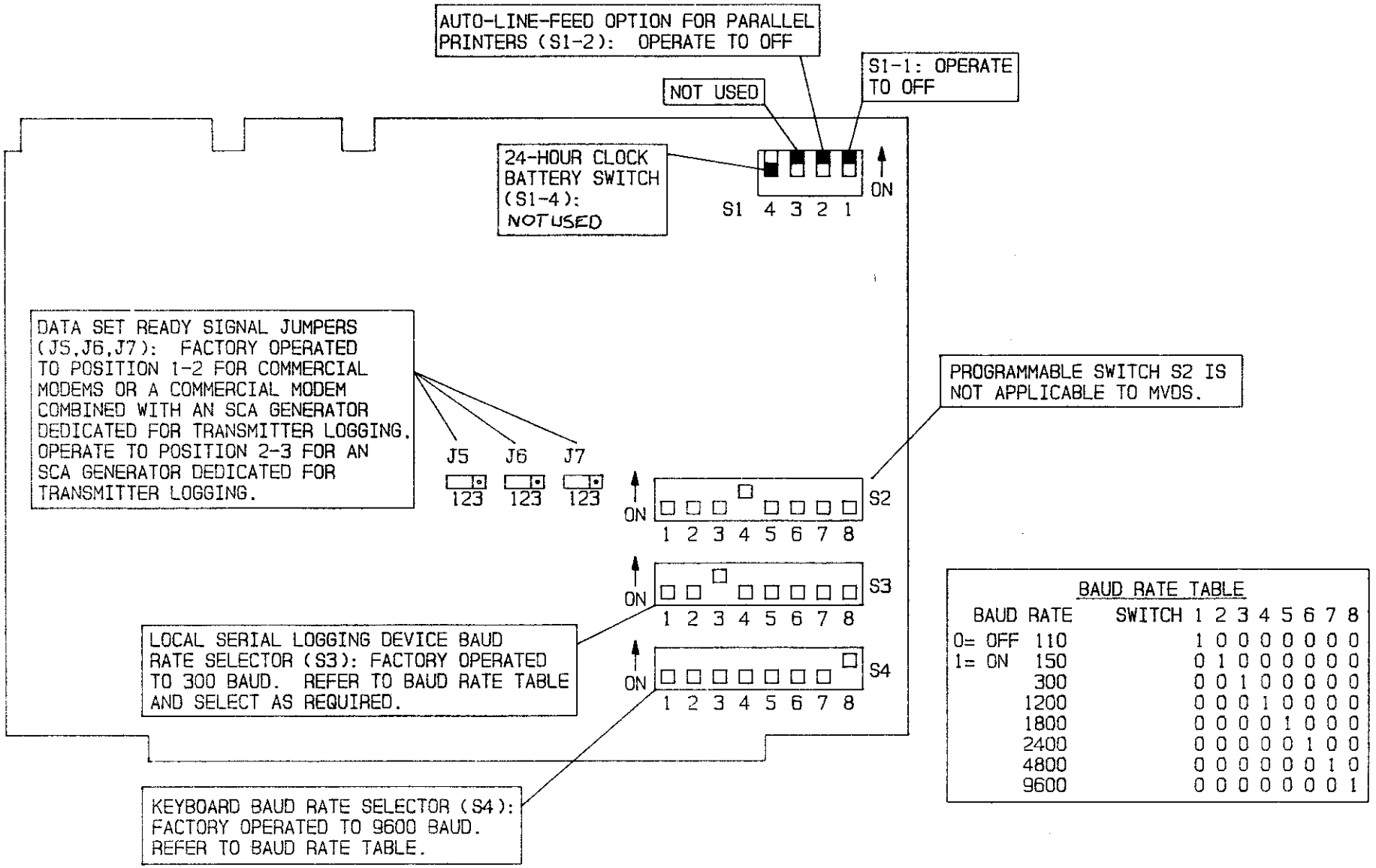

597-0036-5

**FIGURE 2–3. 64K MEMORY CIRCUIT BOARD JUMPER PROGRAMMING**




597-0036-6

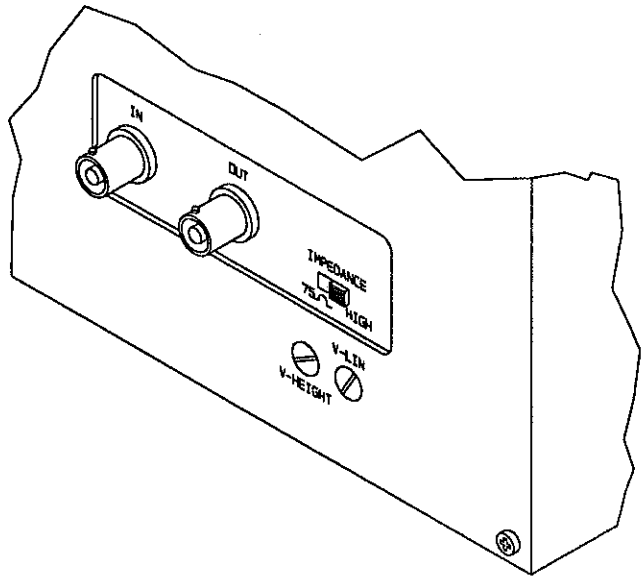
**FIGURE 2–4. ANALOG/DIGITAL CIRCUIT BOARD JUMPER PROGRAMMING**




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597-0036-65

**FIGURE 2–5. INPUT/OUTPUT CIRCUIT BOARD JUMPER PROGRAMMING**




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597-0036-30

**FIGURE 2–6. MVDS VIDEO MONITOR SWITCH PROGRAMMING**

2–13. Refer to Figure 2–7 and install the MVDS video monitor as follows:

A. Open the transmitter controller cabinet doors and connect the video monitor ac line cord to the receptacle which is located at the top of the microprocessor power supply assembly.

B. Connect wire W10 to the monitor VIDEO IN jack.

C. Connect wire W6 to the monitor VIDEO OUT jack.

D. Slide the video monitor into the chassis opening and secure the two turnlock fasteners.

2–14. Refer to Figure 2–7 and install the MVDS circuit boards and connect the cables.

2–15. **COMMUNICATION EQUIPMENT CONNECTIONS.**

2–16. **KEYBOARD.** The MVDS is provided with a system keyboard. Refer to Figure 2–9 and connect the keyboard cable to serial port J6 located on the rear–panel of the controller cabinet.

2–17. **LOGGING DEVICES.** A logging system is incorporated into the MVDS which allows the operator to obtain a printed copy of the transmitter parameters presented on the normal display screen. Different types of customer furnished logging devices may be connected to the MVDS. The following information and Figure 2–8 illustrate typical logging device applications. Cable information is provided in Section VII. The cables may be manufactured locally or purchased from Broadcast Electronics, Inc.

2–18. **Local Serial Or Parallel Printer.** Transmitter logs may be printed at the transmitter site through the use of an inexpensive home computer type parallel printer or a serial printer. Cable information is presented in drawing 949–0110 for the parallel printer and drawing 949–0113 for the serial printer.

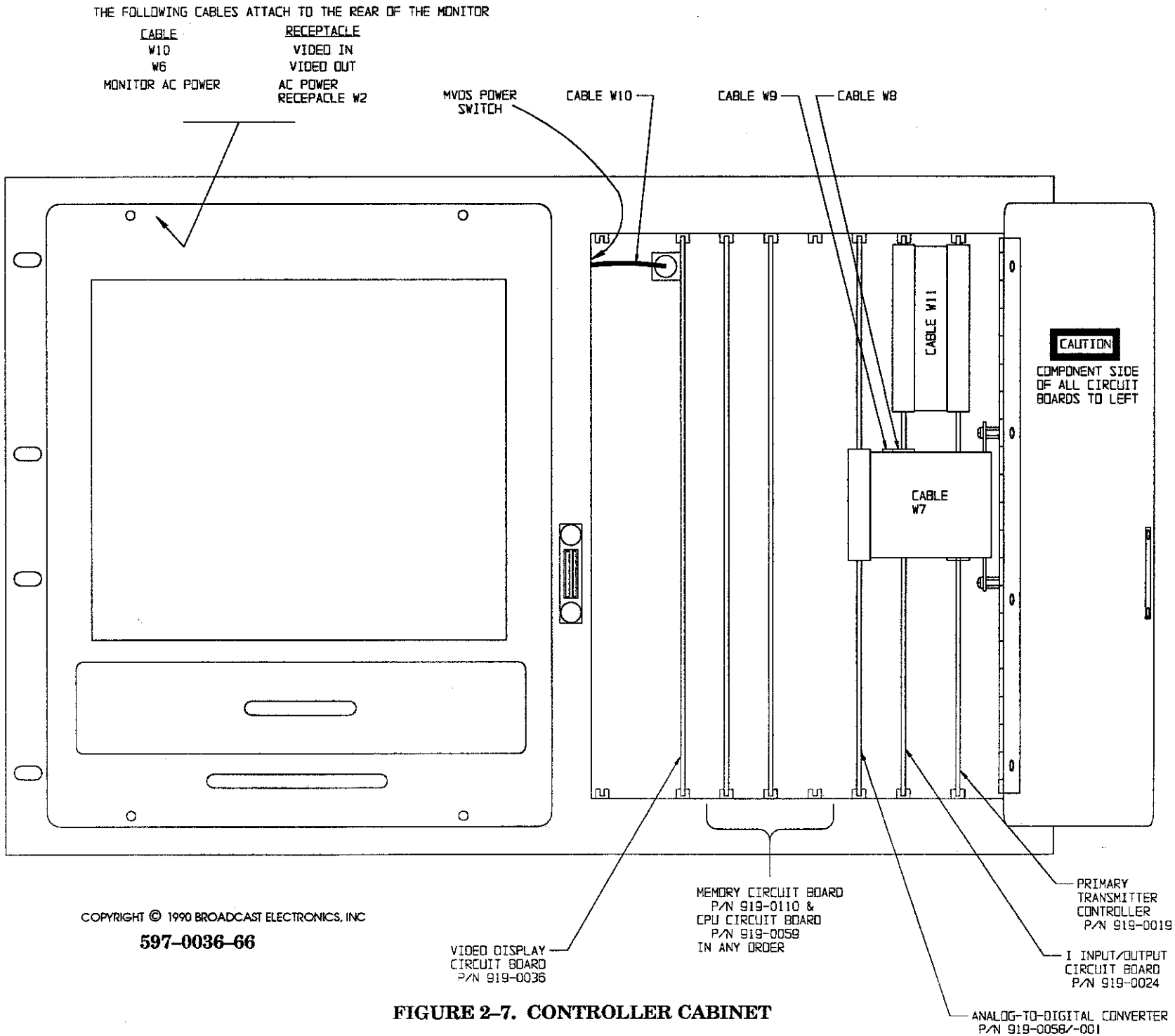



**FIGURE 2–7. CONTROLLER CABINET**

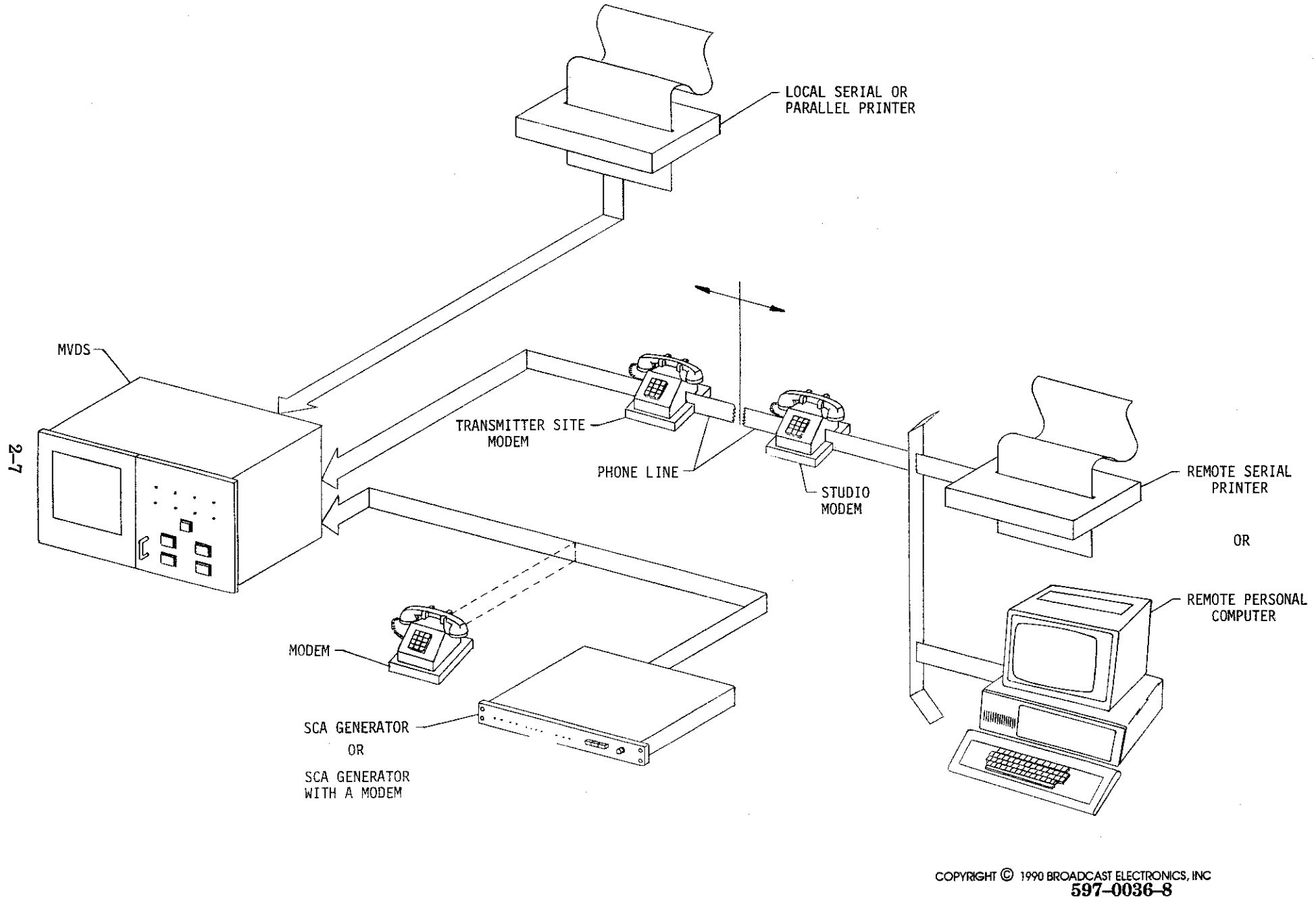



**FIGURE 2–8. TYPICAL LOGGING DEVICE APPLICATIONS**

2–19. **Transmitting Log Information Through A Modem.** Log information may be transmitted through a modem for remote reception by a serial printer or a personal computer. Two modems are required for logging operations: a transmitter site modem and a receiver site modem. Drawing 949–0114 provides cable information for the transmitter site modem.

2–20. In order for the modems to transmit and receive log information, the transmitter site modem and the studio modem must be operated with the following general characteristics.

| TRANSMITTER SITE MODEM | STUDIO MODEM |
|---|---|
| 1. Monitors and recognizes carrier detect. | 1. The same baud rate as the transmitter site modem. |
| 2. Auto–answer (Not required for dedicated line service). | |
| 3. No interpretation of data as commands. | |

2–21. **Transmitting Log Information Through An SCA Generator.** Log information may be transmitted through an SCA generator for remote reception. An SCA generator may be used alone or connected in parallel with a modem to provide an alternate logging method if the transmitter cycles off–the–air. Drawing 949–0111 provides cable information for the SCA generator and drawing 949–0112 provides information for the SCA generator combined with a modem.

2–22. **Logging Device Connections To The MVDS.** Connections for the logging devices are provided on the rear panel of the controller cabinet. The following list describes each connector.

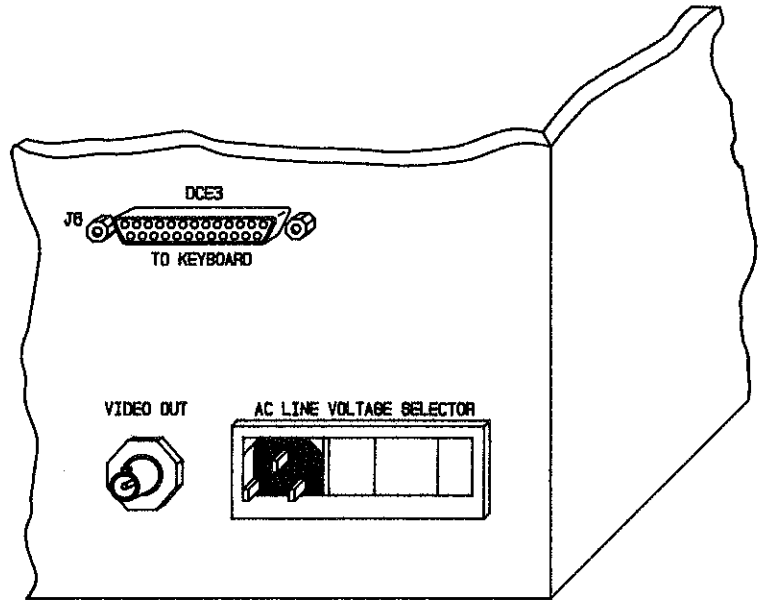
| CONNECTOR | TYPE OF PORT | SPECIFIC USE |
|---|---|---|
| J7 CENTRONICS | Parallel | Log Printer |
| J5 DCE2 | Serial | Log Printer, Modem, SCA Generator, or SCA Generator with a Modem |

2–23. **Baud Rate Selection.** Baud rate selection for devices connected to DCE2 is provided on the input/output circuit board. It is recommended that SCA logging be performed at 1200 baud, and modem logging be performed at 300 or 1200 baud, depending on the type of modem used. Refer to Figure 2–5 and ensure switch S3 is operated to the correct baud rate for the device.

2–24. **CABLE ROUTING.** Cables for the keyboard and the logging devices should be routed through the knock–out provided on the base plate of the transmitter. Inside the transmitter cabinet, route the cables as close to the cabinet frame as possible to avoid mechanical damage and connect the cable to the appropriate connector.

2–25. **EXTERNAL VIDEO OUTPUT.** The MVDS is equipped with an external video output connector which is located on the rear–panel of the controller cabinet. Refer to Figure 2–9 and connect the device to the VIDEO OUT connector if external video is desired.

2–26. **STATUS INPUTS.** Tower lights and external alarm status input circuits can be monitored with MVDS software version V2.0 or greater. If monitoring a status input is desired, remove the appropriate jumper from TB2–34 or TB2–35 on the transmitter remote interface panel. When +5 volts is applied to either input, the monitor will display the associated message. If monitoring the status inputs is not required, ensure terminals TB2–34 and TB2–35 are jumpered to ground.




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

**597–0036–2**

**FIGURE 2–9. REAR–PANEL OF CONTROLLER CABINET**

2–27. To monitor the tower lights, connect a tower light sensing device between terminal strip TB2–35 and ground on the transmitter remote interface panel. To monitor an external alarm, connect an alarm sensing device between terminal strip TB2–34 and ground on the transmitter remote interface panel.

2–28. For transmitters not equipped with TB2–34 and TB2–35 on the remote interface panel, connect the sensing devices as follows. To monitor tower lights, connect a sensing device between transmitter controller rear–panel connector J3–18 and ground. To monitor an external alarm, connect a sensing device between transmitter controller rear–panel connector J3–19 and ground.

2–29. **AC POWER CONNECTION.**

*WARNING* *ENSURE ALL PRIMARY POWER IS DISCONNECTED BEFORE PROCEEDING.*

*WARNING*

2–30. A transmitter controller which is equipped with an MVDS system is programmed for the proper power supply voltage when shipped from the factory. Refer to Figure 2–9 and remove the fuse from the rear–panel fuse–holder. Ensure the fuse is a slow–blow type rated at 2A for 220V operation.

# SECTION III
# OPERATION

## 3–1. INTRODUCTION.

3–2. This section provides initial entry and standard operating procedures for the Broadcast Electronics Microprocessor Video Diagnostics System.

## 3–3. INITIAL OPERATION.

### 3–4. KEYBOARD.

3–5. Initial operation begins with the operation of the keyboard which provides communication between the operator and the MVDS. Refer to Figure 3–1 and Table 3–1 and learn the basic keyboard commands and special key functions.

### 3–6. TURN–ON.

***CAUTION*** ***ENSURE THE TRANSMITTER IS OFF AND ALL CIRCUIT BREAKERS ARE OFF BEFORE PROCEEDING.***

***CAUTION***

***NOTE*** ***ENSURE THE TRANSMITTER IS COMPLETELY INSTALLED AND OPERATING PROPERLY BEFORE PROCEEDING.***

***NOTE***

3–7. If the transmitter is on–the–air, operate the transmitter to OFF and operate all circuit breakers to OFF.

3–8. Operate the following circuit breakers to ON:

| | | |
|---|---|---|
| FM–3.5B/5B | AC POWER | BLOWER |
| FM–10B | CONTROL | DRIVER |
| FM–30B | CONTROL | DRIVER |
| FM–35B | CONTROL | DRIVER |
| FM–20B | CONTROL | |

3–9. Operate the MVDS power switch (located above the monitor) to ON.

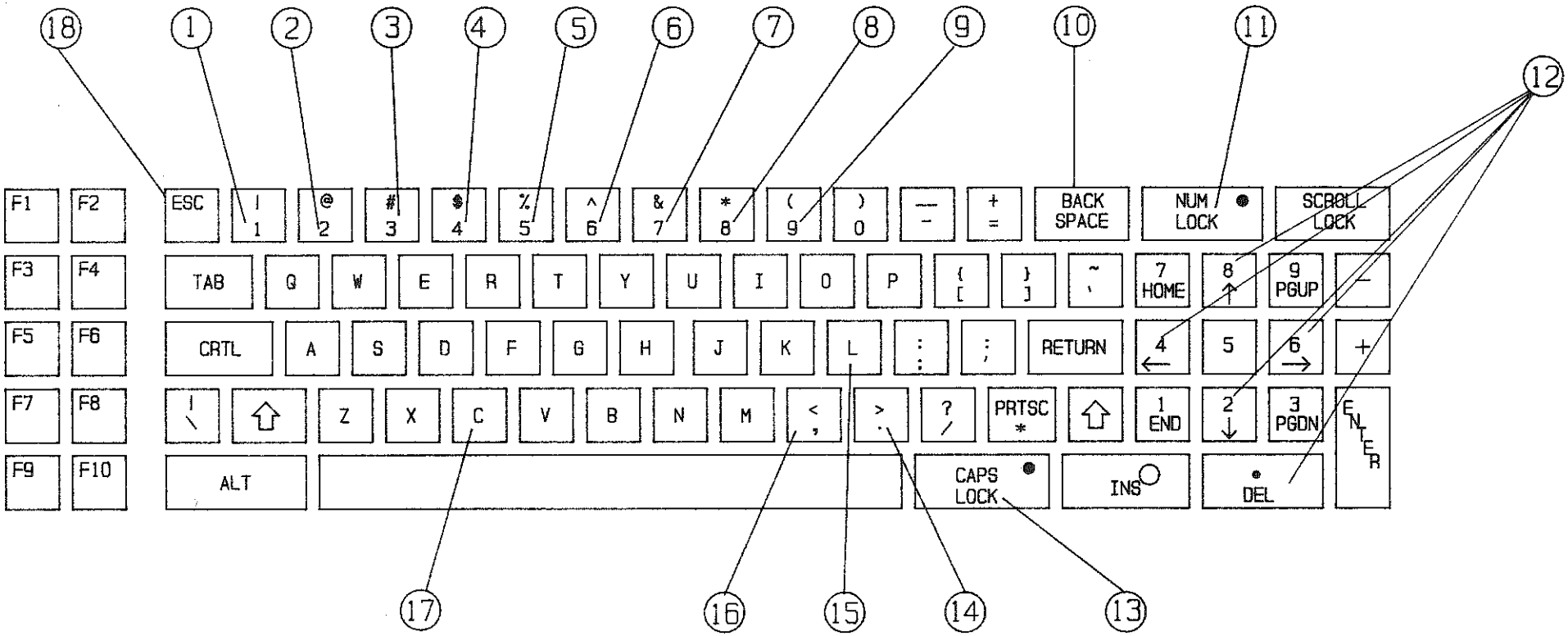
3–10. **NORMAL DISPLAY SCREEN.** With power applied, the normal display screen will appear on the monitor. Refer to Figure 3–2 and Table 3–2 for a description of the display.

3–11. **Clock Set Procedure.** To program the 24–hour clock, proceed as follows:

3–12. Before programming the 24–hour clock, depress the transmitter **OVERLOAD** reset switch to remove the POWER FAILURE warning.

3–13. Depress the CAPS LOCK key for upper case character entry. The **CAPS LOCK** indicator will illuminate.

3–14. Operate the NUM LOCK key to extinguish the **NUM LOCK** indicator.



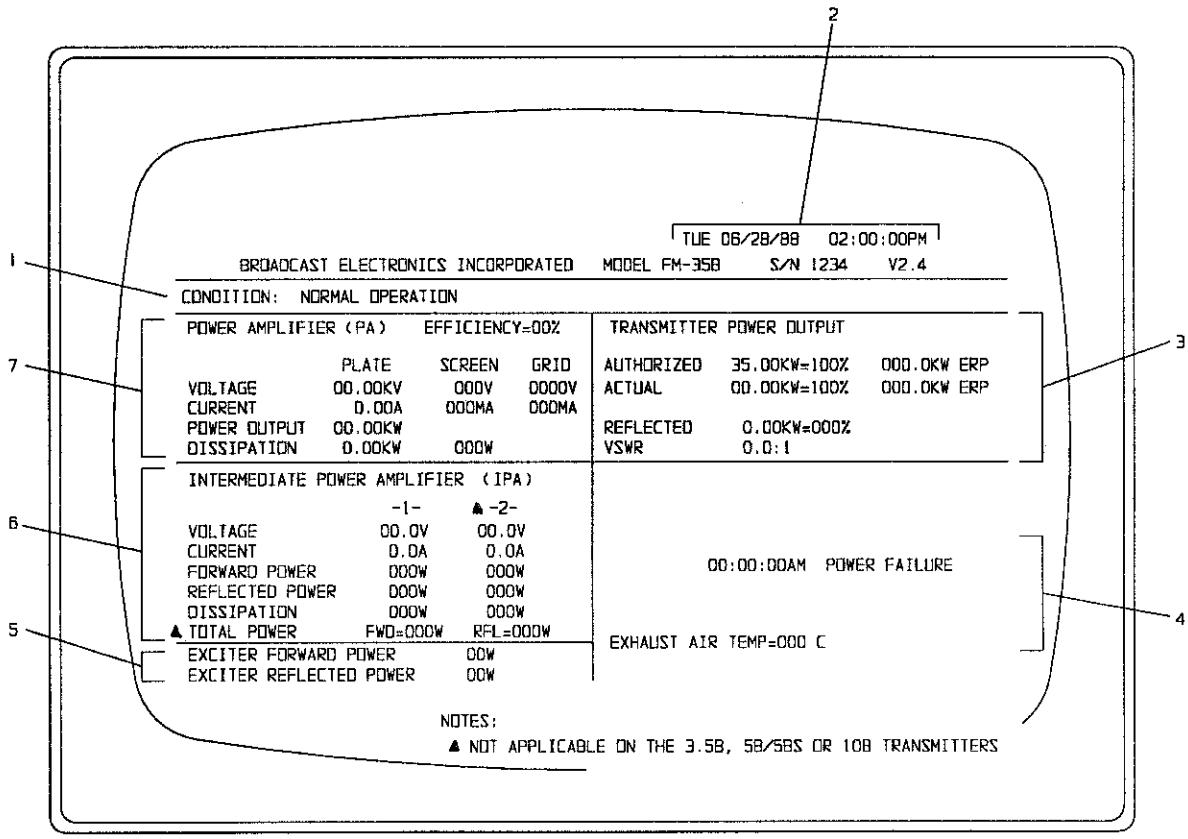

COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597–0036–50

**FIGURE 3–1. KEYBOARD**

## TABLE 3–1. KEYBOARD COMMANDS

| INDEX NUMBER | DESCRIPTION |
|---|---|
| 1 | Advances the day–of–the–week in the CLOCK SET mode. |
| 2 | Advances the month in the CLOCK SET mode and accesses the bar–graph screen. |
| 3 | Advances the day in the CLOCK SET mode and accesses the customer configuration screen. |
| 4 | Advances the year in the CLOCK SET mode. |
| 5 | Advances the hours in the CLOCK SET mode. |
| 6 | Advances the minutes in the CLOCK SET mode. |
| 7 | Advances the seconds in the CLOCK SET mode. |
| 8 | Toggles the 24–hour clock between military time (18:30:00) and normal civilian time (06:30:00PM). |
| 9 | Starts and stops the 24–hour clock. |
| 10 | Cursor backspace. |
| 11 | Toggles the 2, 4, 6, 8, and DEL keys of the numeric keypad between numeric operation (LED illuminated) and cursor operation (LED extinguished). |
| 12 | Enters numeric data when the NUM LOCK LED is illuminated. When the NUM LOCK LED is extinguished, the keys perform cursor operations (left, right, up and down). |
| 13 | Provides upper case character entry. |
| 14 | Cursor advance (depress the ⇑ shift and > ). |
| 15 | Requests a log of the normal display screen when operated during the normal or bar–graph display screen. |
| 16 | Cursor backspace (depress the ⇑ shift and < ). |
| 17 | Accesses the CLOCK SET mode (CLOCK SET is only accessible from the normal display screen). |
| 18 | Terminates the CLOCK SET mode and accesses the normal display screen. |




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

**597-0036-10**

**FIGURE 3-2. NORMAL DISPLAY SCREEN**

3-15. Depress the C key (CLOCK SET will appear on the lower right-hand corner of the screen).

3-16. Depress the DELETE key (resets the 24-hour clock).

3-17. Depress key 1 until the correct day-of-the-week appears on the 24-hour clock.

3-18. Depress key 2 until the correct month appears on the 24-hour clock.

3-19. Depress key 3 until the correct day appears on the 24-hour clock.

3-20. Depress key 4 until the correct year appears on the 24-hour clock.

3-21. Depress key 5 until the correct hour appears on the 24-hour clock.

3-22. Depress key 6 until the correct minutes appear on the 24-hour clock.

3-23. Depress key 7 until the correct seconds appear on the 24-hour clock.

3-24. Depress key 8 to convert the 24-hour clock into military time (example 18:30:00) or depress key 8 again for normal civilian time (example 06:30:00AM).

3-25. Depress key 9 to manually start (or stop) the 24-hour clock.

3-26. Depress the ESCAPE key (CLOCK SET will disappear from the display and the 24-hour clock will automatically start).

TABLE 3–2. NORMAL DISPLAY SCREEN

| INDEX NUMBER | DESCRIPTION |
|---|---|
| 1 | Displays the present condition of the transmitter and the reason for the condition. |
| 2 | Displays the 24–hour clock which is programmed by the operator. The clock will automatically adjust for leap year. |
| 3 | Displays the status of the TRANSMITTER POWER OUTPUT parameters: ACTUAL ERP, REFLECTED power, and VSWR. |
| 4 | Displays all overload conditions in reverse video and the following transmitter and MVDS statuses. |

| Transmitter | MVDS |
|---|---|
| EXHAUST AIR TEMP. | LOG PRINTING |
| APC ON | LOG ENABLED |
| APC PRESET POWER | CLOCK SET |
| REMOTE CONTROL ON | MPU (microprocessor unit) CONTROL |
| | TOWER LIGHTS |
| | EXTERNAL ALARM (in reverse video when activated) |

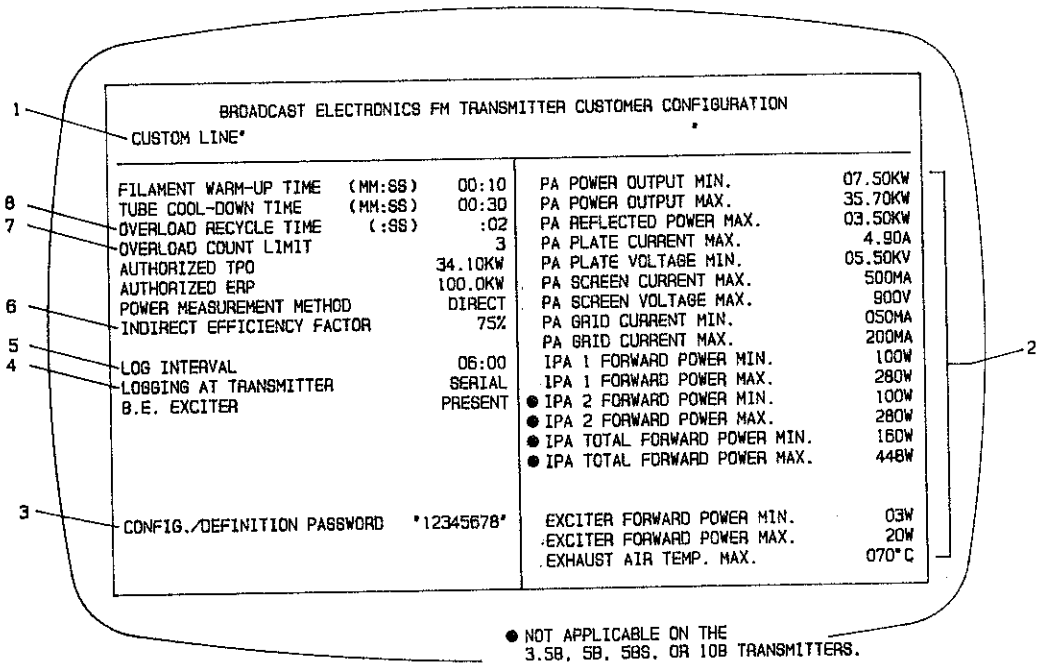
| | |
|---|---|
| 5 | Displays the status of the EXCITER FORWARD and REFLECTED POWER parameters. |
| 6 | Displays the status of the IPA VOLTAGE, CURRENT, FORWARD POWER, REFLECTED POWER, DISSIPATION, and TOTAL POWER parameters. |
| 7 | Displays the status of the PA PLATE, SCREEN, and GRID parameters. |

3–27. **CUSTOMER CONFIGURATION SCREEN.** The next step in initial operation is to access the customer configuration screen which is protected by an eight–digit password. This screen allows the operator to enter maximum and minimum limits of transmitter parameters. The operator must enter limits which are within the factory–set safe operating levels for each model of transmitter. If a limit is entered which is above or below the safe operating level, the cursor will not advance to the next field of entry. To access the customer configuration screen, proceed as follows:

3–28. Depress key 3 (ENTER PASSWORD: " " will appear on the screen).

3–29. Enter 12345678 which is the factory default PASSWORD.

3–30. The customer configuration screen will appear on the monitor. Refer to Figure 3–3 and Table 3–3 for a description of the display.




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597–0036–11

**FIGURE 3–3. CUSTOMER CONFIGURATION SCREEN**

3–31. **Procedure.** To program the customer configuration screen, proceed as follows:

3–32. Enter any desired message on the CUSTOM LINE (40 characters maximum).

3–33. Depress the ⇓ key.

3–34. Enter the FILAMENT WARM–UP TIME. The factory operating limits are:

| | Maximum | Minimum |
|---|---|---|
| All Models | 59:59 | 00:10 |

3–35. Depress the ⇓ key.

3–36. Enter the TUBE COOL–DOWN TIME. The factory operating limits are:

| | Maximum | Minimum |
|---|---|---|
| All Models | 59:59 | 00:30 |

3–37. Depress the ⇓ key.

3–38. Enter the OVERLOAD RECYCLE TIME. The factory operating limits are:

| | Maximum | Minimum |
|---|---|---|
| All Models | 00:59 | 00:01 |

3–39. Depress the ⇓ key.

TABLE 3–3. CUSTOMER CONFIGURATION SCREEN

| INDEX NUMBER | DESCRIPTION |
|---|---|
| 1 | An operator entered message which has a maximum length of 40 characters (example: WBEI–FM 103.3 MHz) and no effect on transmitter parameters. |
| 2 | Operator minimum and maximum limits for transmitter parameters (values displayed on the screen are factory default limits). The operator entered limits must be within the factory–set safe operating levels or the cursor will not advance to the next field of entry. |
| 3 | A customer generated eight character password which authorizes access to the MVDS customer configuration screen. This password will replace factory default password 12345678. |
| 4 | Defines the type of logging printer at the transmitter site. |
| 5 | The length of time between log printouts (example: 00:10 – a log will print every 10 minutes). |
| 6 | The indirect efficiency factor is an efficiency value which is calculated and entered at the factory and displayed on the PA section of the normal display screen (if the indirect power measurement method is selected). The indirect efficiency factor must be updated as required to reflect the changes in transmitter efficiency. |
| 7 | The number of overloads the transmitter will accept before the transmitter will deenergize and must be manually reset. |
| 8 | The length of time the transmitter remains off–the–air after an overload to allow the condition that prompted the overload to dissipate. |

3–40. Enter the OVERLOAD COUNT LIMIT. The factory operating limits are:

| | Maximum | Minimum |
|---|---|---|
| All Models | 9 | 0 |

3–41. Depress the ⇓ key.

3–42. Enter the AUTHORIZED TPO (transmitter power output).

3–43. Depress the ⇓ key.

3–44. Enter the AUTHORIZED ERP.

3–45. Depress the ⇓ key.

3–46. Enter the POWER MEASUREMENT METHOD.

D= DIRECT
I= INDIRECT

3–47. Depress the ⇓ key.

3–48. The INDIRECT EFFICIENCY FACTOR is factory calculated and entered into the display during final testing. The indirect efficiency factor must be updated as required to reflect the changes in transmitter efficiency. If the DIRECT method was selected in the above step, the indirect efficiency factor has no effect on power output calculations and may be disregarded.

3–49. Depress the ⇓ key.

3–50. Enter the LOG INTERVAL. If no periodic logging is required, enter 00:00.

3–51. Depress the ⇓ key.

3–52. Enter the correct responce for logging at the transmitter.

P= PARALLEL
S= SERIAL
D= DISABLED

3–53. Depress the ⇓ key.

3–54. Enter the correct response for BE EXCITER.

P= PRESENT
A= ABSENT

3–55. Depress the ⇓ key.

3–56. Enter the CONFIG./DEFINITION PASSWORD.

3–57. If the config./definition password cannot be recalled in the future, contact Broadcast Electronics Customer Service Department.

3–58. Depress the ⇓ key.

3–59. Enter the PA POWER OUTPUT MIN. The factory minimum limits are:

| FM–3.5B | FM–5B/5BS | FM–10B | FM–20B | FM–30B | FM–35B |
|---|---|---|---|---|---|
| 01.35KW | 02.00KW | 04.00KW | 07.50KW | 07.50KW | 07.50KW |

3–60. Depress the ⇓ key.

3–61. Enter the PA POWER OUTPUT MAX. The factory maximum limits are:

| FM–3.5B | FM–5B/5BS | FM–10B | FM–20B | FM–30B | FM–35B |
|---|---|---|---|---|---|
| 04.00KW | 05.75KW | 11.50KW | 22.00KW | 31.00KW | 36.75KW |

3–62. Depress the ⇓ key.

3–63. Enter the PA REFLECTED POWER MAX. The factory maximum limits are:

| FM–3.5B | FM–5B/5BS | FM–10B | FM–20B | FM–30B | FM–35B |
|---|---|---|---|---|---|
| 00.35KW | 00.40KW | 00.80KW | 01.80KW | 03.00KW | 03.00KW |

3–64. Depress the ⇓ key.

3–65. Enter the PA PLATE CURRENT MAX. The factory maximum limits are:

| FM–3.5B | FM–5B/5BS | FM–10B | FM–20B | FM–30B | FM–35B |
|---|---|---|---|---|---|
| 1.35A | 1.42A | 2.50A | 3.60A | 4.90A | 4.90A |

3–66. Depress the ⇓ key.

3–67. Enter the PA PLATE VOLTAGE MIN. The factory minimum limits are:

| FM–3.5B | FM–5B/5BS | FM–10B | FM–20B | FM–30B | FM–35B |
|---|---|---|---|---|---|
| 03.90KV | 04.80KV | 05.00KV | 06.00KV | 05.50KV | 05.50KV |

3–68. Depress the ⇓ key.

3–69. Enter the PA SCREEN CURRENT MAX ). The factory maximum limits are:

| FM–3.5B | FM–5B/5BS | FM–10B | FM–20B | FM–30B | FM–35B |
|---|---|---|---|---|---|
| 150mA | 150mA | 150mA | 200mA | 500mA | 500mA |

3–70. Depress the ⇓ key.

3–71. Enter the PA SCREEN VOLTAGE MAX. The factory maximum limits are:

| FM–3.5B | FM–5B/5BS | FM–10B | FM–20B | FM–30B | FM–35B |
|---|---|---|---|---|---|
| 750V | 850V | 900V | 999V | 900V | 900V |

3–72. Depress the ⇓ key.

3–73. Enter the PA GRID CURRENT MIN. The factory minimum limits are:

| FM–3.5B | FM–5B/5BS | FM–10B | FM–20B | FM–30B | FM–35B |
|---|---|---|---|---|---|
| 020mA | 020mA | 020mA | 020mA | 025mA | 025mA |

3–74. Depress the ⇓ key.

3–75. Enter the PA GRID CURRENT MAX. The factory maximum limits are:

| FM–3.5B | FM–5B/5BS | FM–10B | FM–20B | FM–30B | FM–35B |
|---|---|---|---|---|---|
| 060mA | 060mA | 100mA | 150mA | 200mA | 200mA |

3–76. Depress the ⇓ key.

3–77. Enter the IPA 1 FORWARD POWER MIN. The factory minimum limits are:

| FM–3.5B | FM–5B/5BS | FM–10B | FM–20B | FM–30B | FM–35B |
|---|---|---|---|---|---|
| 075W | 075W | 075W | 075W | 100W | 100W |

3–78. Depress the ⇓ key.

3–79. Enter the IPA 1 FORWARD POWER MAX. The factory maximum limits are:

| FM–3.5B | FM–5B/5BS | FM–10B | FM–20B | FM–30B | FM–35B |
|---|---|---|---|---|---|
| 220W | 250W | 250W | 250W | 280W | 280W |

3–80. Depress the ⇓ key.

3–81. Enter the IPA 2 FORWARD POWER MIN (FM–20B, FM–30B, and FM–35B only). The factory minimum limit is:

| FM–20B | FM–30B | FM–35B |
|---|---|---|
| 75W | 100W | 100W |

3–82. Depress the ⇓ key.

3–83. Enter the IPA 2 FORWARD POWER MAX (FM–20B, FM–30B, and FM–35B only). The factory minimum limit is:

| FM–20B | FM–30B | FM–35B |
|---|---|---|
| 250W | 280W | 280W |

3–82. Depress the ⇓ key.

3–85. Enter the IPA TOTAL FORWARD POWER MIN (FM–20B, FM–30B, and FM–35B only). The factory minimum limit is:

| FM–20B | FM–30B | FM–35B |
|---|---|---|
| 130W | 160W | 160W |

3–86. Depress the ⇓ key.

3–87. Enter the IPA TOTAL FORWARD POWER MAX (FM–20B, FM–30B, and FM–35B only). The factory maximum limit is:

| FM–20B | FM–30B | FM–35B |
|---|---|---|
| 448W | 448W | 448W |

3–88. Depress the ⇓ key.

3–89. Enter the EXCITER FORWARD POWER MIN. The factory minimum limits are:

| FM–3.5B | FM–5B/5BS | FM–10B | FM–20B | FM–30B | FM–35B |
|---|---|---|---|---|---|
| 05W | 05W | 05W | 10W | 03W | 03W |

3–90. Depress the ⇓ key.

3–91. Enter the EXCITER FORWARD POWER MAX. The factory maximum limits are:

| FM–3.5B | FM–5B/5BS | FM–10B | FM–20B | FM–30B | FM–35B |
|---|---|---|---|---|---|
| 25W | 30W | 40W | 50W | 20W | 20W |

3–92. Depress the ⇓ key.

3–93. Enter the EXHAUST AIR TEMP. MAX (FM–3.5B, FM–5B/5BS, FM–10B, FM–20B, FM–30B, and FM–35B only). The factory maximum limits are:

| FM–3.5B | FM–5B/5BS | FM–10B | FM–20B | FM–30B | FM–35B |
|---|---|---|---|---|---|
| 75°C | 75°C | 75°C | 95°C | 95°C | 95°C |

## 3–94. TRANSMITTER OPERATION WITH MVDS.

3–95. After the customer configuration screen has been properly programmed, the last step is to operate the transmitter with the MVDS. The status of the transmitter parameters will be displayed on the normal display screen and the bar–graph screen.

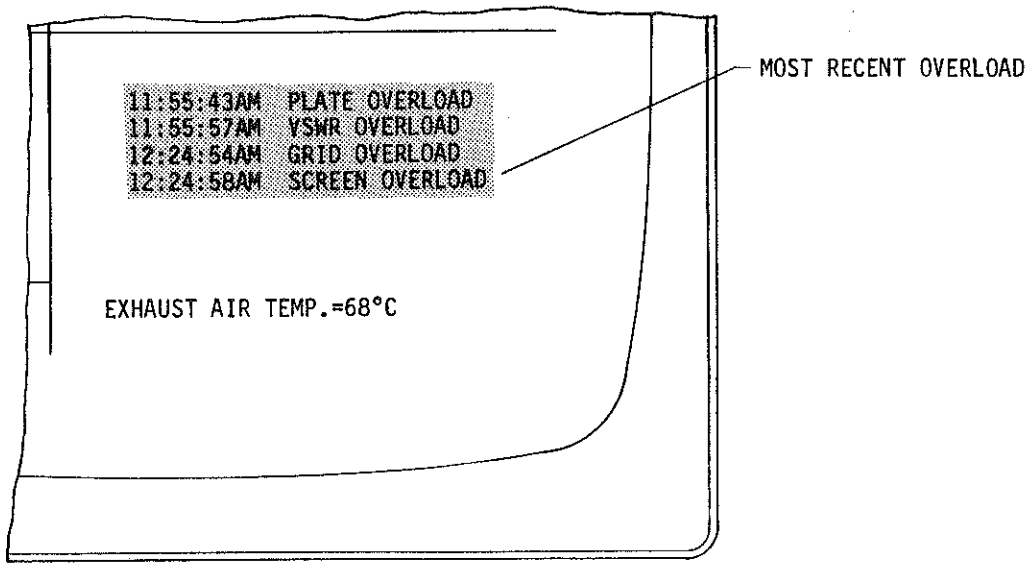
### 3–96. OPERATION OF THE NORMAL DISPLAY SCREEN.

3–97. Access the normal display screen by depressing the ESCAPE key (the normal display screen will appear on the monitor). The operator can access the normal display screen at any time by depressing the ESCAPE key.

3–98. Operate the transmitter at the normal RF power output. The normal display screen will display the status of the transmitter parameters. After the transmitter has cycled–on, a Transmitter On Log of the normal display screen will be printed by the MVDS (if the logging system has been enabled).

3–99. Observe the normal display screen values and the Transmitter On Log. Due to the accuracy of the MVDS, use the MVDS normal display screen as the transmitter primary metering system. Use the transmitter analog meters as a secondary metering system as required.

3–100. **OVERLOADS.** Four transmitter parameters are monitored for overloads by the transmitter controller and the MVDS: control grid bias current, screen current, PA VSWR, and plate current. If a single or a series of overloads occur: 1) the transmitter will cycle off–the–air, 2) the type of overload(s) will be displayed in the lower right–hand corner of the normal display screen with the most recent displayed at the bottom (refer to Figure 3–4), and an OVERLOAD LOG will be printed by the MVDS. If the overload clears, the transmitter will cycle on–the–air and the overload display will remain until the **OVERLOAD** reset switch is depressed.

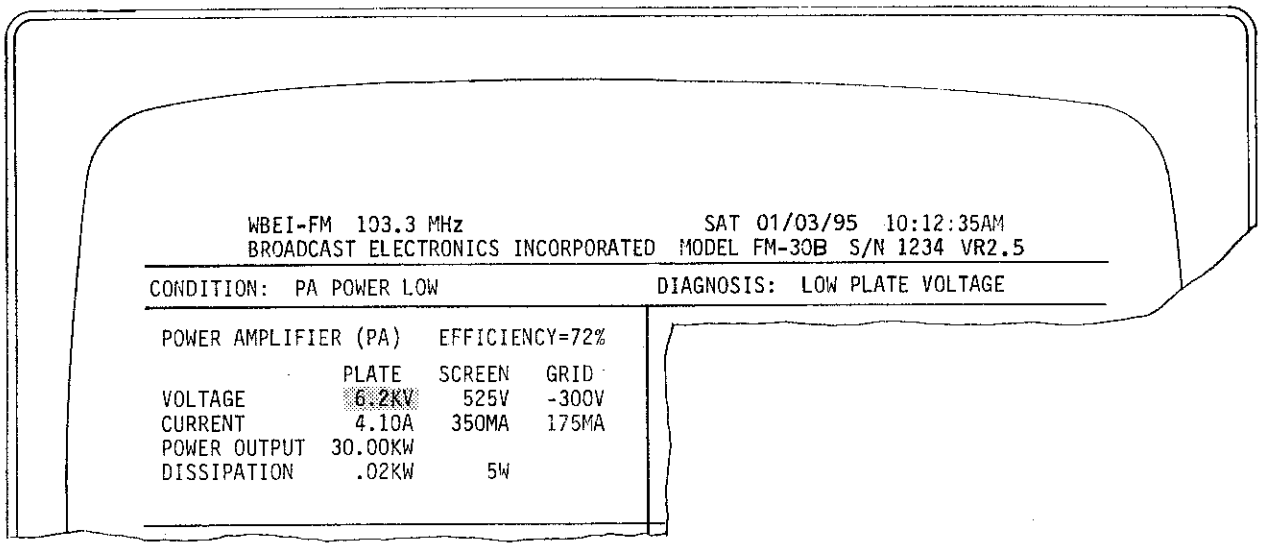



COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597–0036–12

**FIGURE 3–4. OVERLOAD DISPLAY**

3–101. **TOLERANCE HIGHLIGHTING.** If one of the transmitter parameters exceeds the limits of the customer configuration screen (example: low plate voltage), the value of the out–of–limit parameter will be highlighted (displayed in reverse video) on the normal display screen (refer to Figure 3–5). The CONDITION line will display the status of the transmitter (example: PA POWER LOW) and the DIAGNOSIS line will display the reason for the condition (example: LOW PLATE VOLTAGE).




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597–0036–13

**FIGURE 3–5. TOLERANCE HIGHLIGHTING**

3–102. **NON–VOLATILE MEMORY MONITORING.** Software within the MVDS is designed to monitor the status of the non–volatile memory. In the event of non–volatile memory failure, the following message will appear in reverse video on the normal display screen above the CONDITION/DIAGNOSIS line.

"***REPLACE NONVOLATILE MEMORY, X2***"

3–103. **OPERATION OF THE BAR GRAPH SCREEN.**

3–104. The second operating display screen is the bar–graph screen. The bar–graph screen displays the transmitter parameters in bar–graph form which changes with the status of the transmitter. The display is especially valuable in tuning the transmitter for overall maximum efficiency and checking the basic transmitter operating parameters quickly.

3–105. **PROCEDURE.** To access and observe the operation of the bar–graph screen, proceed as follows:

3–106. With the monitor displaying the normal display screen, depress ⇓ key. The bar–graph screen will appear on the monitor.

3–107. Refer to the following illustrations for a description of the bar–graph display.

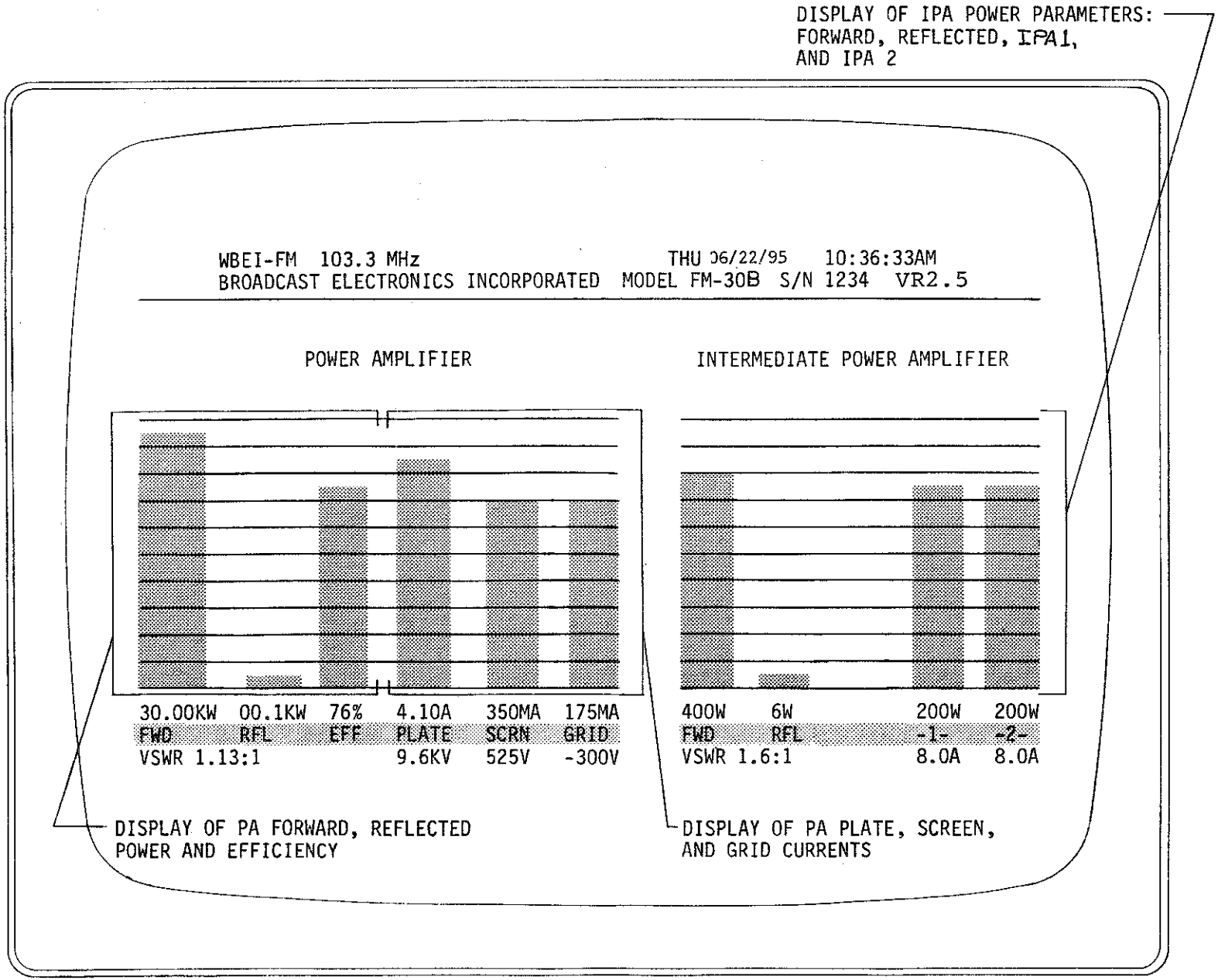
**FIGURE 3–6**

FM–20B
FM–30B
FM–35B

**FIGURE 3–7**

FM–3.5B FM–5B/5BS
FM–10B

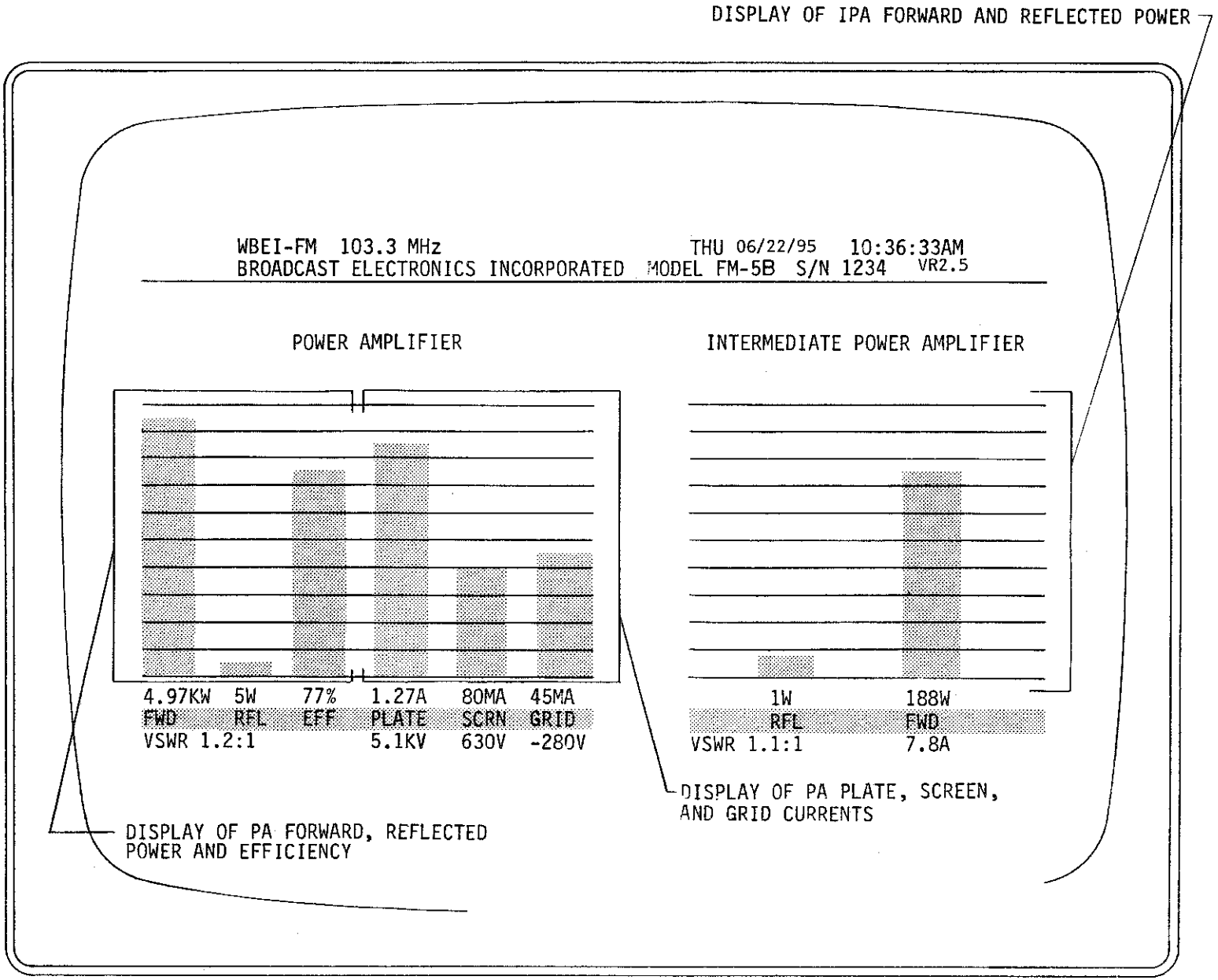
3–108. With the transmitter in operation, the bar–graphs will display a normal pattern of the transmitter parameters. If one of the displayed parameters exceeds the limits of the customer configuration screen (example: grid current), the parameter will be highlighted (refer to Figure 3–8).




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

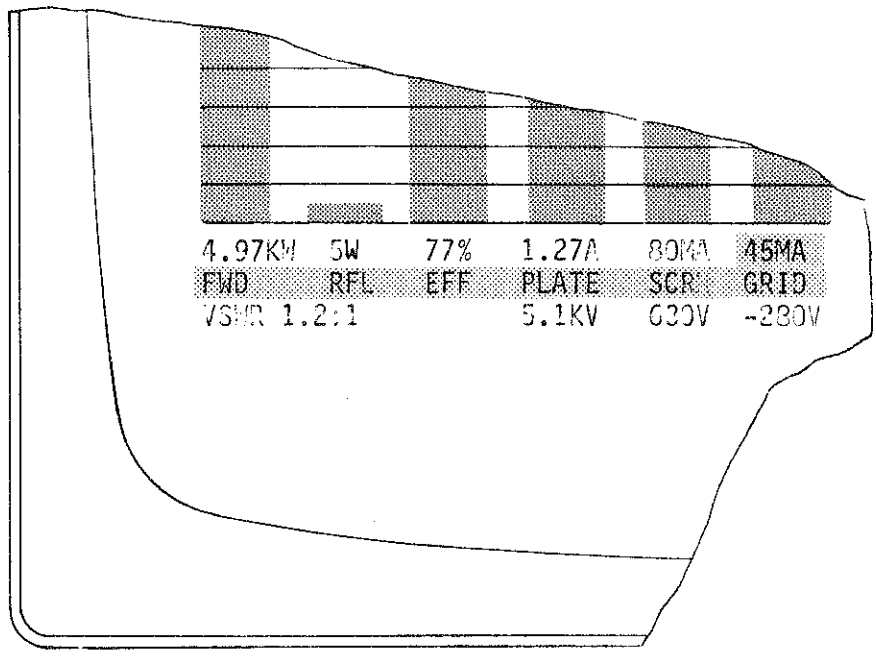
597-0036-14

**FIGURE 3-6. FM-20B, FM-30B, AND FM-35B BAR GRAPH DISPLAY SCREEN**




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC
597–0036–15

**FIGURE 3–7. FM–3.5B, FM–5B/FM–5BS, AND FM–10B BAR GRAPH DISPLAY SCREEN**




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597-0036-16

**FIGURE 3-8. BAR GRAPH SCREEN HIGHLIGHTING**

3-109. **MPU/DIGITAL CONTROLLER CONTROL.**

3-110. With the MVDS option, the transmitter is equipped with two redundant and independent controllers: the transmitter digital controller and the MPU (microprocessor unit) controller which is incorporated into the MVDS. Both monitor transmitter parameters and completely control transmitter operations.

3-111. To operate the transmitter with the digital controller, operate switch S2 on the controller circuit board to CONT. With the digital controller, the filament warm-up time, tube cool-down time, overload recycle time, and the overload count limit are determined by the digital circuitry on the controller circuit board. The digital controller will control the transmitter operation with the MVDS displaying and diagnosing the transmitter parameters.

3-112. To operate the transmitter with MPU control, operate switch S2 on the controller circuit board to MICRO (MPU CONTROL will appear in the lower right-hand corner of the screen). With MPU CONTROL, the filament warm-up time, tube cool-down time, overload recycle time, and the overload count limit are determined by the values entered in the customer configuration screen. The microprocessor unit of the MVDS system will monitor and control transmitter operation and also display and diagnose the transmitter parameters. The controller circuit board will be by-passed until the microprocessor unit is disabled, then control will automatically be returned to the controller circuit board.

3-113. **TRANSMITTER LOGS.**

3-114. When a transmitter log is required, a copy of the normal display screen will be printed by the logging device. Logs may be requested by the operator at any time during the normal or bar-graph display screens (depress the L key) or provided automatically by the MVDS. The following list describes the conditions for an automatic log to occur:

1. A transmitter overload or AC power failure.
2. Operating the transmitter to ON.
3. Operating the transmitter to OFF.
4. An external alarm condition which deenergizes the transmitter to OFF.
5. An interval log which is determined by the customer configuration screen.

## 3–115. TRANSMITTER OPERATION WITHOUT MVDS.

3–116. Due to the dual controller design, the transmitter may be operated without MVDS if required. To operate the transmitter without MVDS, proceed as follows:

A. Operate the controller circuit board **CONT/MICRO** switch to **CONT**.

B. Operate the **MVDS ON/OFF** switch to **OFF**. Control of the transmitter will be returned to the Digital Controller.

*NOTE*

*NOTE*

***WHEN MVDS IS DISABLED, ALL LOCAL AND REMOTE METER INDICATIONS WILL BE INACCURATE. TO CORRECT THE METER INDICATIONS, REMOVE CABLE W7 FROM THE ANALOG–TO–DIGITAL CONVERTER CIRCUIT BOARD.***

# SECTION IV
# THEORY OF OPERATION

## 4–1. INTRODUCTION.

4–2. This section provides the principles of operation for the Broadcast Electronics MVDS. An overall system description is presented first, followed by a detailed description of each circuit board.

## 4–3. GENERAL DESCRIPTION.

4–4. Refer to Figure 4–1 as required for the following discussion.

### 4–5. SYSTEM COMPONENTS.

4–6. The Broadcast Electronics MVDS is a video diagnostic system which is constructed of solid–state circuitry for maximum reliability. The system consists of the following items:

A. Circuit Boards:

1. 64K Memory Circuit Board
2. Analog/Digital Circuit Board
3. Input/Output Circuit Board
4. Central Processing Unit (CPU) Circuit Board
5. Video Display Module (VDM) Circuit Board
6. EMI Filter Circuit Board
* 7. Controller Circuit Board
8. Motherboard

* Supplied with the standard transmitter controller

B. System Keyboard

C. Video Monitor

D. Power Supply

4–7. **64K MEMORY CIRCUIT BOARD.** The 64K memory circuit board provides all the read only memory (ROM) and the random access memory (RAM) for the MVDS system. The ROM is implemented through EPROMS (erasable programmable read only memory) which provide a permanent memory storage location for the system software. The RAM provides the microprocessor with temporary memory storage.

4–8. **ANALOG/DIGITAL CIRCUIT BOARD.** The analog/digital circuit board converts analog transmitter samples to digital codes through CMOS analog–to–digital integrated circuits. The digital codes are stored within the analog–to–digital converter built–in memory and accessed by the microprocessor when required.

4–9. **INPUT/OUTPUT CIRCUIT BOARD.** The input/output circuit board provides data and control communication between the microprocessor and the keyboard, the controller circuit board, and the logging devices. Parallel input and output ports are provided for the controller circuit board. Parallel and serial ports are provided for logging devices with one serial port dedicated to the system keyboard.

4–10. **CPU CIRCUIT BOARD.** The CPU circuit board is the main control element for the MVDS. The CPU contains a Z–80 microprocessor which executes the system software. The CPU accesses and routes data into and out of the system circuit boards.

4–11. **VDM CIRCUIT BOARD.** The VDM is a Z–80 based microprocessor circuit board that accepts data and commands from the CPU. In response to CPU commands and data, the VDM generates the composite video and synchronization pulses required by the video monitor.

4–12. **EMI FILTER CIRCUIT BOARD.** The EMI filter circuit board processes all keyboard and peripherial device inputs and outputs to minimize susceptibility to electromagnetic interference.

4–13. **CONTROLLER CIRCUIT BOARD** (Supplied with the standard Transmitter Controller). When the microprocessor is in control of the transmitter (MPU CONTROL), the controller circuit board provides the MVDS with transmitter indicator and switch status information. Also, control lines are routed through the controller circuit board which allows the microprocessor to operate the switch indicators, LED display, and control relays when required.

4–14. **MOTHERBOARD.** A communication network between the MVDS circuit boards is implemented through the motherboard. The motherboard interconnects the CPU, the 64K memory circuit board, the VDM circuit board, the analog/digital circuit board, and the input/output circuit board.

4–15. **SYSTEM KEYBOARD AND VIDEO MONITOR.** The keyboard and the video monitor provide communication between the operator and the MVDS. The operator communicates to the MVDS through keyboard commands which are processed by the microprocessor. The MVDS communicates to the operator through transmitter parameter displays on the video monitor.

4–16. **POWER SUPPLY.** The power supply provides all MVDS operating voltages and is completely independent of the standard transmitter controller power supply for greater reliability.

4–17. **SYSTEM COMMUNICATION.**

4–18. The MVDS operates under the direction of a Z–80 based microprocessor which is located on the CPU circuit board. The microprocessor responds to a set of instructions from a computer program which is stored in ROM on the 64K circuit board. Each instruction in the program has a specific location and a unique address within the memory. The microprocessor operates by: 1) accessing an instruction from the computer program, 2) processing the instruction, 3) routing data to or from the appropriate device.

4–19. Communication for microprocessor operation is provided by an S–100 bus which is implemented on the motherboard. The S–100 bus contains three communication buses: the address bus, the data bus, and the control bus.

4–20. The address bus transmits a 16–bit binary code from the CPU which identifies a specific device and memory location. The CPU can address the 64K memory circuit board, analog/digital circuit board, VDM circuit board, or the input/output circuit board.

4–21. The data bus, which works with the address bus, carries information or data. The data bus is divided into two parts, Data In and Data Out. Data In is information entering the CPU from a location identified by the address. Data Out is information from the CPU to a location identified by the address.

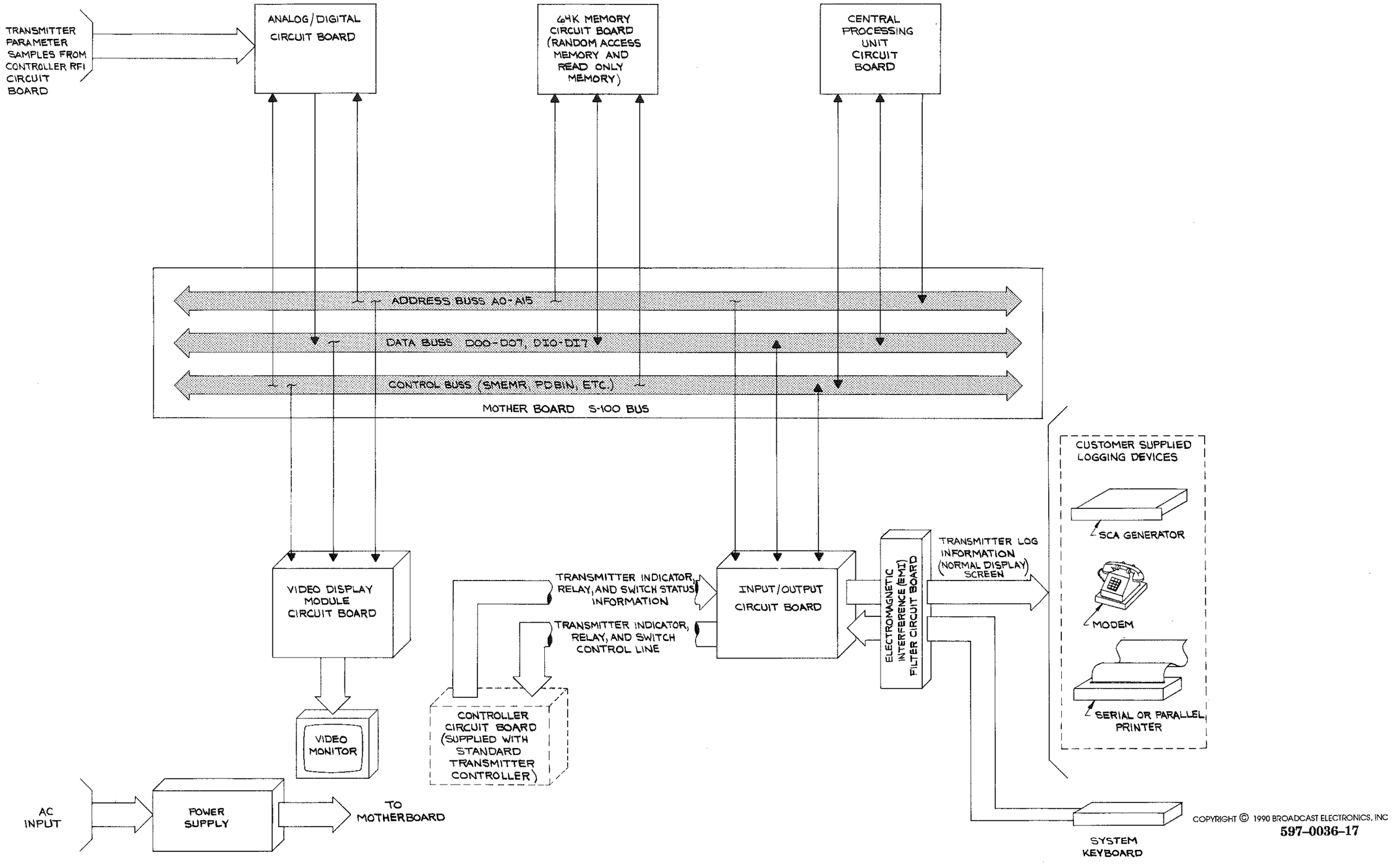



**FIGURE 4–1. MVDS BLOCK DIAGRAM**

4–22. The control bus carries control signals between the CPU and the MVDS circuit boards. Examples of these signals are the Read strobe and the Write strobe. The Read strobe indicates the CPU is in a mode to accept data that is present on the Data In bus. The Write strobe indicates the CPU is in a mode to transmit data on the Data Out bus. Both signals require a simultaneous address with active information on a data bus.

4–23. The microprocessor communicates with the controller circuit board, keyboard, and the logging devices via the input/output circuit board. Keyboard and controller circuit board information are accessed from the input/output circuit board by the microprocessor when required. Log and transmitter control information from the microprocessor is applied to the peripherial devices and controller circuit board through ports on the input/output circuit board.

## 4–24. DETAILED DESCRIPTION.

### 4–25. 64K MEMORY CIRCUIT BOARD.

4–26. **GENERAL.** The 64K memory circuit board provides both read only memory (ROM) and random access memory (RAM) for the MVDS system (refer to Figure 4–2). ROM, as the name implies, can only be read by the microprocessor. RAM is a type of memory that can be written into, changed, and read by the microprocessor.

4–27. The ROM is implemented through EPROMs which store 2 K bytes (eight bits equals one byte) of information. The EPROMs provide a permanent memory storage location for the MVDS control program. The control program directs the actions of the microprocessor and is electrically programmed into the EPROMs. Once programmed, the EPROM can only be erased by ultra–violet light. A sticker is placed over the window of the EPROM to prevent accidental erasing.

4–28. The RAM functions as temporary memory storage for the microprocessor. Two types of RAM are located on the 64K memory circuit board: volatile and non–volatile.

4–29. The volatile RAM is implemented through RAM integrated circuit X1 which stores 2 K bytes of information and provides the microprocessor with temporary data storage. This type of RAM is not battery supported and the stored data will not be retained when power is deenergized.

4–30. The non–volatile RAM is implemented through E²PROM X2 which stores 2 K bytes of information and provides a memory location for the customer configuration screen data. This special type of RAM is not externally battery supported, however the stored information will be retained when power is deenergized. Therefore, the customer configuration screen data will not need to be re–entered after a power failure.

***NOTE*** ***DI (DATA IN) REFERS TO DATA INPUT TO THE MICROPROCESSOR AND DO (DATA OUT) REFERS TO DATA OUTPUT BY THE MICROPROCESSOR.***

***NOTE***

4–31. **OPERATION.** All inputs and outputs (data in bus, data out bus, and address bus) from the 64K memory circuit board are buffered by non–inverting tri–state bus drivers (refer to schematic 919–0110). The tri–state drivers are active only when the control signal is a logical LOW state. U14 buffers address lines A0 through A7 and U15 buffers A8 through A15. U16 buffers data out lines DO0 through DO7 and U17 buffers data input lines DI0 through DI7.

4–32. When the microprocessor requests or writes data from the memory circuit board, the particular memory location is selected with address lines A0 through A10 and the particular RAM or ROM integrated circuit is selected with address lines A11 through A15. Address lines A11 through A15 are routed to address decoders U2, U4, U6, and U7. The decoders output a LOW which enables the proper memory device. Memory location address lines A0 through A10 are routed directly from the buffers to each memory device for internal decoding by each RAM or ROM integrated circuit.

4–33. **Address Disable Switches.** Switches S2–1 through S2–4 are used to disable the data in bus (data routed to the microprocessor) when an address for memory locations on EPROMs X29, X30, X31, and X32 is assigned to a memory device which is located on another MVDS circuit board. When one of the switches is closed and one of the EPROMs (X29, X30, X31, X32) is selected by U7, a LOW is applied to one of the inputs of U20A. U20A outputs a HIGH through inverter U21D to NAND gate U20B. U20B outputs a HIGH which disables the data in bus driver.

4–34. **Writing Data Into Memory.** When the microprocessor is required to write data into RAM integrated circuits X1 or X2, the integrated circuit address will be decoded by U2 and the memory location address will be applied through address lines A0 through A10. The MWRITE signal from the microprocessor will go HIGH, indicating the microprocessor is ready to write data into a memory location. U21 inverts the MWRITE signal and applies a LOW to data output driver U16 which allows data to be written into memory.

4–35. **Reading Data From Memory.** When the microprocessor requests data from RAM or ROM, the memory location and integrated circuit address will be decoded by a combination of internal and external logic. U20B functions as a read gate and NANDS the processor data bus in signal (PDBIN), the status memory read signal (SMEMR), and the output of U20A (address disable switches). The SMEMR and the PDBIN signals the processor is ready to read data from memory and the timing is correct to route data onto the motherboard data in bus. When the inputs to U20B go HIGH, a LOW is output to the data in bus driver (U17), allowing the microprocessor to read data from memory.

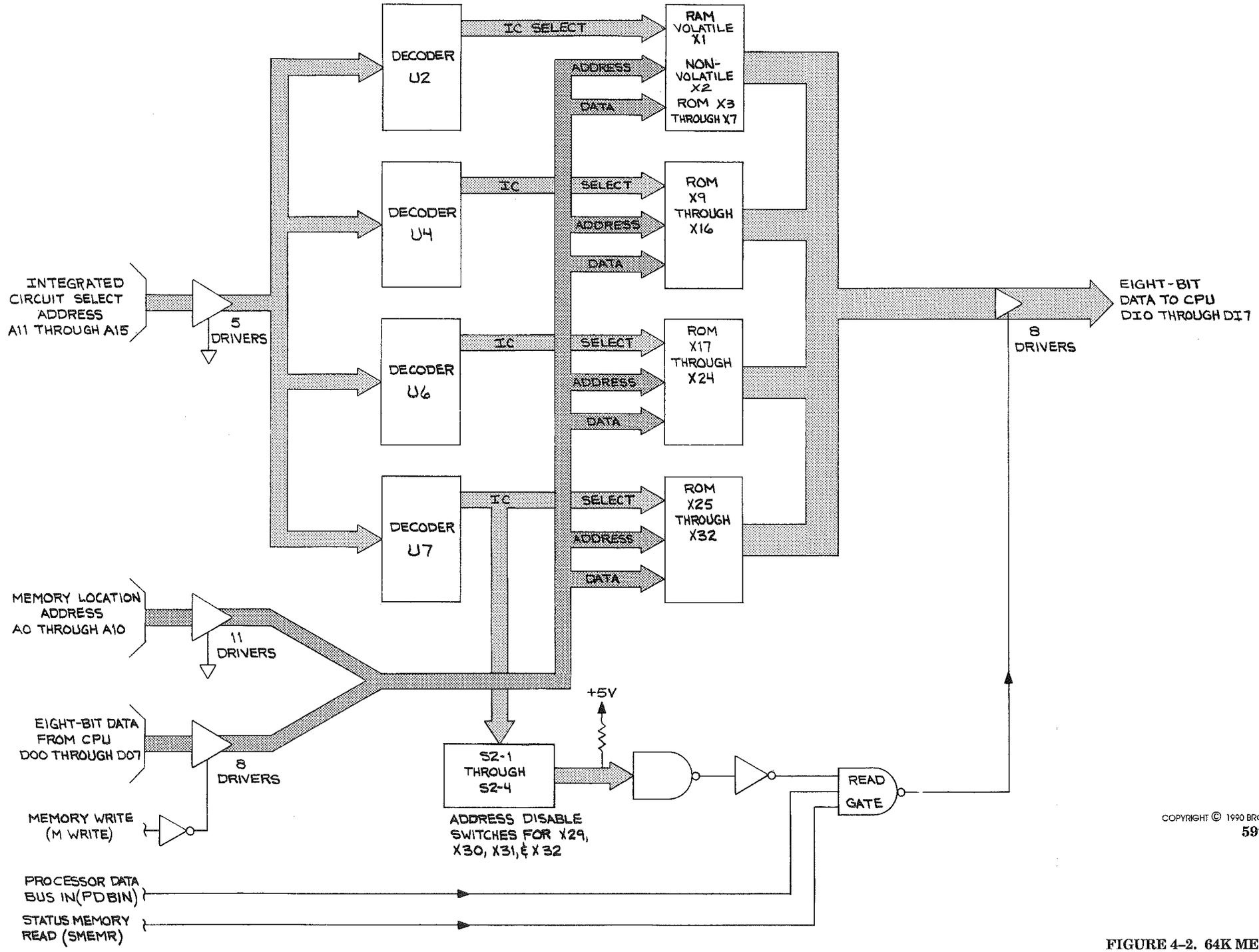
4–36. **ANALOG/DIGITAL CIRCUIT BOARD.**

4–37. **GENERAL.** The analog/digital circuit board provides digital transmitter parameter values for the video display (refer to Figure 4–3). Analog transmitter parameters are converted to eight–bit codes through CMOS analog–to–digital integrated circuits. The digital codes are stored in the analog–to–digital converter RAM memory. Access to the memory is provided by the address bus. If the memory is not addressed every 10.2 seconds, an automatic reset signal will be applied to the microprocessor.

4–38. **OPERATION.** Transmitter parameter samples from the controller RFI filter circuit board are applied through an RC filter and protection diodes. The filtered sample is applied through an amplifier stage to the input of the analog–to–digital converter.

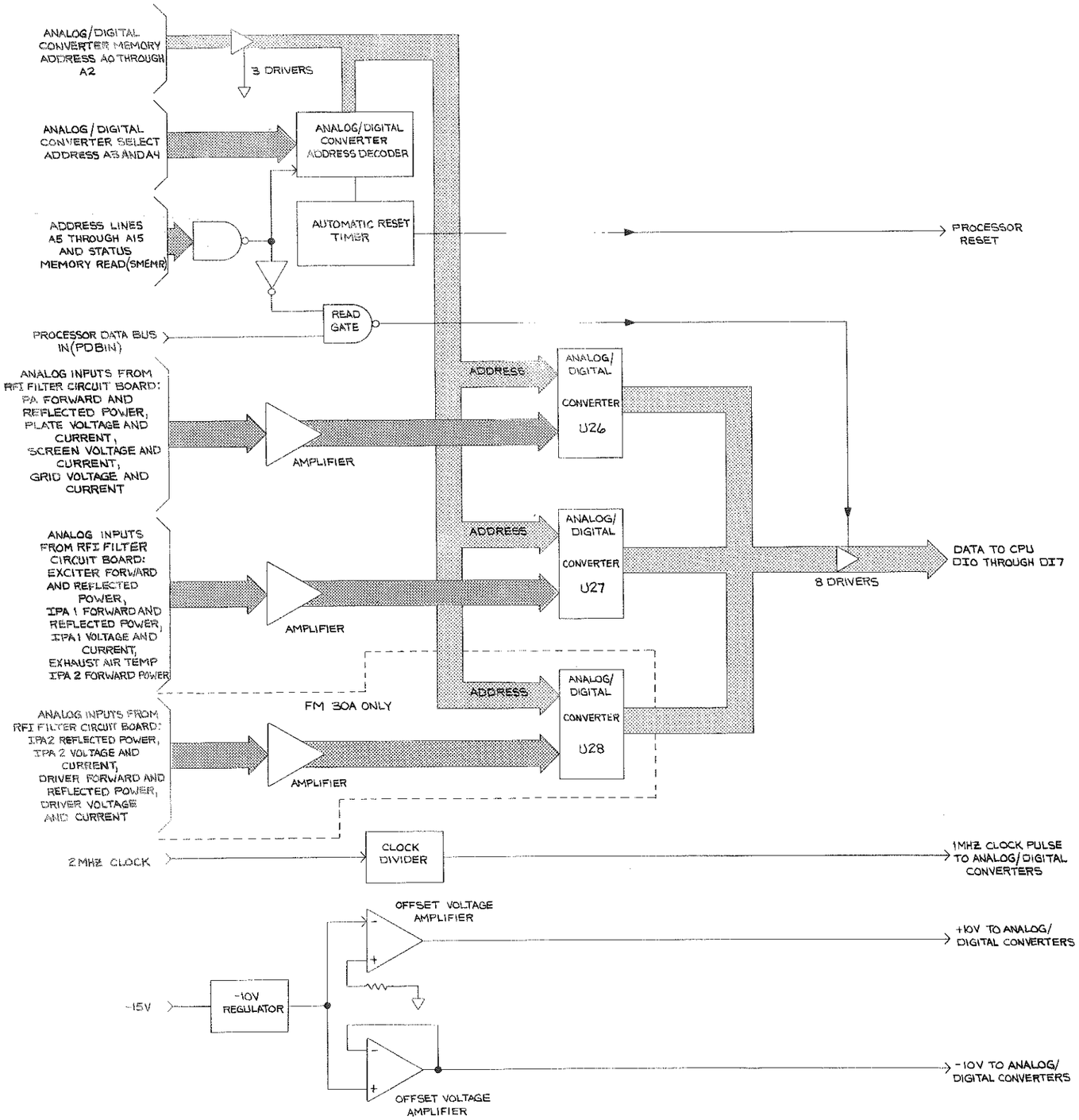
4–39. **Analog–To–Digital Converter and Support Circuitry.** The analog–to–digital converter is a data acquisition system which consists of an analog–to–digital converter, an 8 channel multiplexer, an 8 X 8 RAM (storage for 8 eight–bit words), tri–state data drivers, address latches, and control logic. The converter accepts eight analog inputs and sequentially converts each input into an eight–bit binary code. The eight binary codes are then stored in the 8 X 8 RAM. The tri–state data drivers, control logic, and the address latches control the flow of data to the data bus.

4–40. Timing is provided by a 1 MHz clock pulse from U24A. Calibration of the analog–to–digital converter is provided by dc offset voltage. Precision –10V reference U16 establishes a voltage to offset voltage amplifiers U14A and U14B. The non–inverted –10V dc output of U14A and the inverted +10V dc output of U14B are applied to all analog– to–digital converters through potentiometers and jumpers. This calibration is performed at the factory and is not considered a field adjustment.




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC
597-0036-18

**FIGURE 4–2. 64K MEMORY CIRCUIT BOARD BLOCK DIAGRAM**




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

**597-0036-25**

**FIGURE 4-3. ANALOG/DIGITAL CIRCUIT BOARD BLOCK DIAGRAM**

4–41. **Addressing The Memory.** When the microprocessor requests data from the analog–to–digital memory, the memory location address is applied through address lines A0 through A2 and buffer U21 to each of the analog–to–digital converters. The three lines have eight combinations of logical states which the converter decodes and selects one of the eight memory locations.

4–42. Address line A5 will go LOW and be inverted by NAND gate U18A. Address line A8 will also go LOW and be inverted by U17A and NANDed at U18B with a HIGH from A7. Address lines A9 through A15 will go HIGH and be NANDed at U20 with a HIGH from U17B. U20 will output a LOW which is inverted HIGH by U17C. The HIGH from U17C is NANDed at U19A with a HIGH from the status memory read (SMEMR) signal, a HIGH from line A6, and a HIGH from U18A.

4–43. The analog–to–digital converter will be selected by address lines A3 and A4. Address lines A3 and A4 and a LOW from U19A are routed to converter address decoder U23. U23 decodes the BCD (binary coded decimal) address and outputs a LOW to enable the proper analog–to–digital converter.

4–44. **Automatic Microprocessor Reset.** As long as the microprocessor routes an active address to decoder U23, the decoder will periodically apply a LOW to automatic reset timer U25. This pulse prevents the reset timer from biasing transistor Q1 on. If the decoder does not receive an active address, a continuous HIGH will be applied to the reset timer. After 10.2 seconds, the timer will output a HIGH which biases Q1 on. This pulls the reset line LOW and resets the microprocessor.

4–45. **Reading The Data.** During the addressing sequence, the processor data bus in (PDBIN) signal will go HIGH, indicating timing is correct for data transfer. The HIGH from PDBIN is NANDed with a HIGH from the inverted output of U19A at read gate U18C. U18C will output a LOW to line driver U22, allowing the microprocessor to read data from the addressed memory location.

4–46. **INPUT/OUTPUT CIRCUIT BOARD.**

4–47. **GENERAL.** The input/output circuit board provides data and control communication between the microprocessor and the keyboard, the controller circuit board, and the logging devices. The input/output circuit board houses seven communication ports, address decoding logic, read and write circuitry, a controller circuit board monitor circuit, the 24–Hour clock, and the MPU (microprocessor unit) control request circuit.

4–48. **OPERATION.** Communication ports U11, U12, and U13 (refer to Figure 4–4) communicate with the keyboard and serial logging devices. The serial ports are referred to as universal asynchronous receiver/transmitters (UART). The UARTs contain four types of internal circuits: data exchange, control, status, and operation support.

4–49. The data exchange circuitry receives and transmits data between the microprocessor and the external devices. The control circuitry communicates microprocessor commands to the UART while the status circuitry communicates UART and external device logic conditions back to the microprocessor. The operation support circuitry provides internal clock information which allows the UART to operate at an identical baud rate as the external device.

4–50. The microprocessor addresses the UART in two different ways. The microprocessor can check the status of the UART for data present (example: keyboard information that is entered into U11) or enable the UART to route data to the peripherial device.

4–51. Parallel ports U7, U8, and U9 communicate transmitter indicator status and control information which is routed through the controller circuit board. Parallel port U1 (Centronics) communicates with a home computer type parallel printer.

4–52. The parallel ports contain internal information registers and control circuitry. Information routed to a parallel port is stored in four internal registers. The control circuitry directs the flow of the information to and from the registers. Information is accessed by the microprocessor by addressing the correct port and information register.

4–53. **Addressing.** Address decoding is performed by U10, U18, and U20. The address is applied through lines A0 through A7. An address is routed to the decoding logic through bidirectional bus lines DB0 through DB7 when the processor synchronization (PSYNC) line is pulsed HIGH. The PSYNC is inverted LOW by U31A which enables address buffer U32. U23A inverts the PSYNC line again and provides a clock pulse for the address latches.

4–54. The microprocessor can address several devices on the input/output circuit board. The following list describes the address lines for each device.

| DEVICE | ADDRESS DESCRIPTION |
|---|---|
| Serial Port | Line A0 selects the data/status. Lines A2 and A3 select the particular serial port. |
| Parallel Port | Lines A0 and A1 select the information register. Lines A2 through A4 select the particular parallel port. |
| 24–Hour System Clock | A logical combination of lines A0 through A5. |
| MPU Control Request Circuit | A logical combination of lines A0 through A6. |

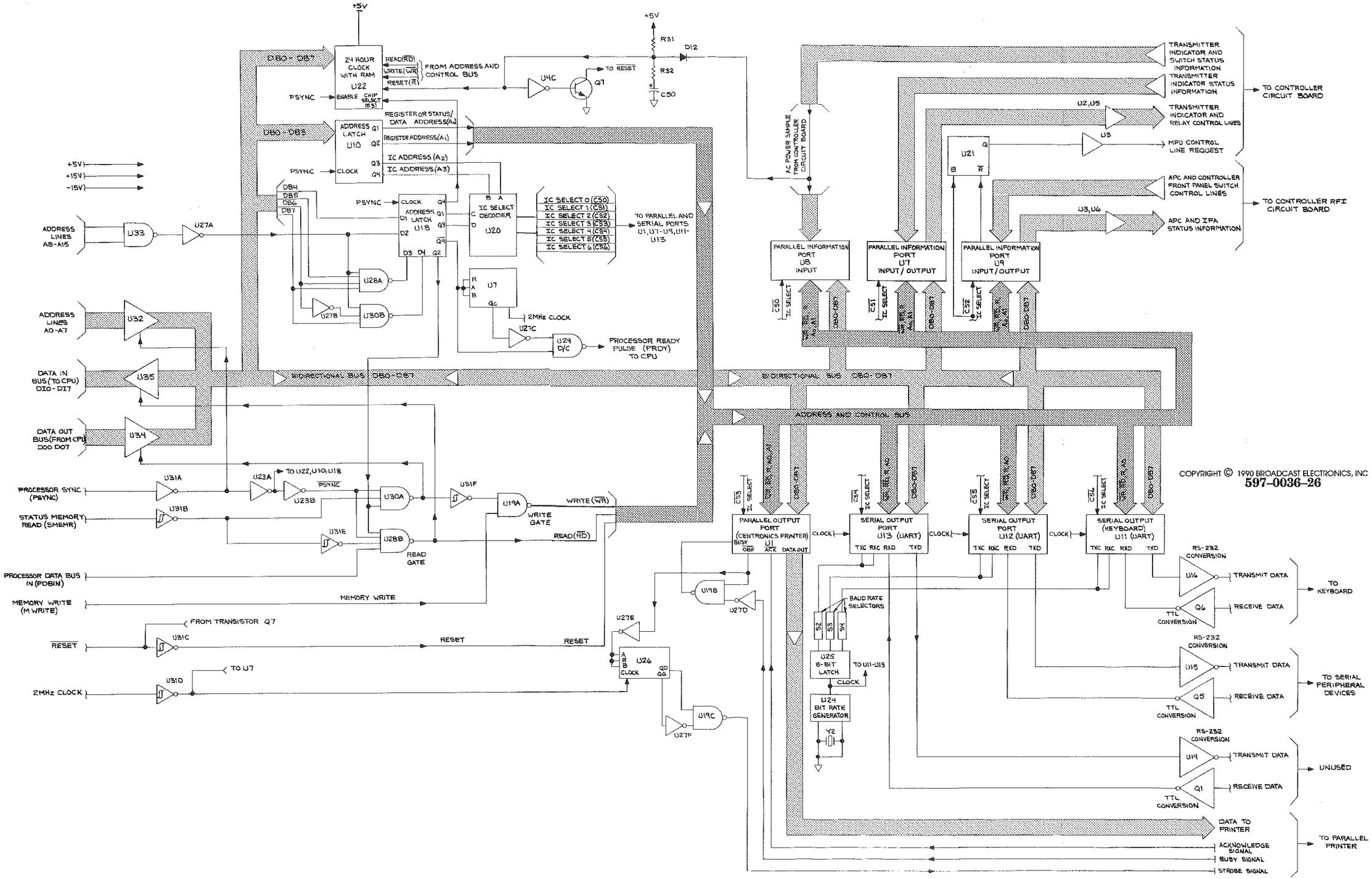
4–55. When the microprocessor routes an address to the decoding logic, the states of lines DB0 through DB3 will be latched into U10. Address lines A8 through A15 will go HIGH and be NANDed at U33. The output of U33 will go LOW and be inverted by U27A. Line DB4 and a HIGH from inverter U27A are routed to U18. Lines DB5 through DB7 are partially decoded at U28A and U30B, and routed to latch U18.

4–56. Latch U10 will output: 1) the proper register enable for the parallel ports or the status/data mode for the serial devices, 2) one–half of the communication port address to U20. U18 outputs the other one–half of the communication port address to decoder U20. U20 decodes the BCD (binary coded decimal) address and applies a LOW to enable the proper communication device.

4–57. **Write Logic.** When the microprocessor is required to write data to one of the communication ports, the microprocessor synchronization (PSYNC) line will pulse HIGH, allowing the address of the communication port to be decoded. The PSYNC will return to a LOW state and be applied through a series of inverters as a HIGH to U30A.

4–58. U30A NANDs the PSYNC signal, the status memory read signal (SMEMR), and the Q2 output of U18. The SMEMR will be LOW and inverted HIGH by U31B. The Q2 output of U18 will go HIGH, allowing U30A to output a LOW to inverter U31F and data–out bus driver U34. The memory write (MWRITE) line will go HIGH and be NANDed at U19A with a HIGH from inverter U31F. U19A will output a LOW to enable the write function of the correct communication device.

4–59. **Read Logic.** U28B functions as a read gate and NANDs the processor synchronization (PSYNC) pulse, the status memory read signal (SMEMR), the processor data bus in (PDBIN) signal, and the Q2 output of U18. When the microprocessor is required to read data from a communication port, the PSYNC line will pulse HIGH, allowing the address to be decoded. The PSYNC will return to a LOW state and be applied through a series of inverters as a HIGH to U28B. The SMEMR signal, the PDBIN signal, and the Q2 output of U18 will go HIGH indicating the microprocessor is ready to route data onto the data–in bus. U28B will output a LOW which enables the read function of the communication port and data–in bus driver U35.




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC
597-0036-26

**FIGURE 4–4. INPUT/OUTPUT CIRCUIT BOARD SIMPLIFIED SCHEMATIC**

4–60. **UART Output Interface Circuitry.** In order for the UART to transmit or receive data from an external device, the data must be converted to the correct voltage levels. Amplifiers U14, U15, and U16 convert the transmit data to RS–232 levels. Transistors Q1, Q5, and Q6 convert the RS–232 receive data from the external devices back to TTL levels for UART operation.

4–61. **Parallel Printer Port (Centronics) Control Logic.** The Centronics control logic on the input/output circuit board provides a start pulse and a wait state for the printer. When Centronics port U1 is required to route data to the printer, U1 will output a LOW at $\overline{\text{OBF}}$ (output buffer full) to shift register U26. U26 will output a signal to NAND gate U19C which outputs a start pulse to the printer.

4–62. While printing data, the printer will output a busy signal to inverter U27D. U27D outputs a LOW which is NANDed with a LOW from the OBF at U19B. U19B routes a HIGH to the busy input of Centronics port U1 which operates the port into a wait state.

4–63. **Controller Circuit Board Monitor Circuit.** An ac power sample from the controller circuit board is applied to parallel information port U8. If power to the controller circuit board is disabled, a ground is applied to D12 which pulls R31 and the reset line to U22 LOW. The LOW is inverted by U4C and biases on transistor Q7. Q7 pulls the reset line LOW which resets the microprocessor and all the communication ports. When power is returned, the +5V charges through R31 and C50 which applies a 0.5 second reset pulse to the microprocessor. The reset pulse allows the communication ports to stabilize data before the microprocessor resumes operation.

4–64. **24–Hour Clock.** The 24–Hour clock is generated on integrated circuit U22. Integrated circuit U22 contains a complete clock and calendar system, address decoding logic, clock/calendar RAM, and general purpose RAM.

4–65. U22 operates by continuously generating clock and calendar data. The data is converted to a parallel format and stored in the clock/calendar RAM.

4–66. The microprocessor addresses U22 through lines DB0 through DB6. The address is decoded through a combination of internal logic and external decoding logic U33, U30B, and latch U18. U18 supplies a HIGH which enables U22 and a LOW (at $\overline{\text{Q4}}$) to shift register U17 and NAND gate U29. U29 outputs the processor ready pulse (PRDY) to the microprocessor. The PRDY pulse instructs the microprocessor to wait before accessing the memory location.

4–67. The microprocessor accesses the clock and calendar data by applying the correct address to the decoding logic. Once the address is decoded, a LOW from read gate U28B will enable the read function of U22, allowing the data to be routed on the bidirectional bus. The microprocessor also writes overload and time data into the general purpose RAM. The write function is enabled when the proper address is decoded and a LOW is applied from write gate U19A.

4–68. **MPU Control Request Circuit.** In order for the MVDS to control the transmitter (MPU Control), the microprocessor must receive control from the controller circuit board. The microprocessor gains control of the transmitter by continuously addressing and enabling (applying a LOW) parallel port U9 and the correct information register. Port U9 routes a HIGH to the active–LOW reset of U21. U21 outputs a HIGH to the logic on the controller circuit board. The logic transfers control to the microprocessor if the switch on the controller circuit board is operated to the MICRO position.

## 4–69. CENTRAL PROCESSING UNIT CIRCUIT BOARD (CPU).

4–70. The CPU circuit board is the central communications and decision making element in the MVDS. At the core of the CPU circuit board is the Z–80A microprocessor chip. All the remaining circuitry on the circuit board aids in routing data, supports operation of the microprocessor chip, and interfaces the circuitry to the S100 bus system (see Figure 4–5).

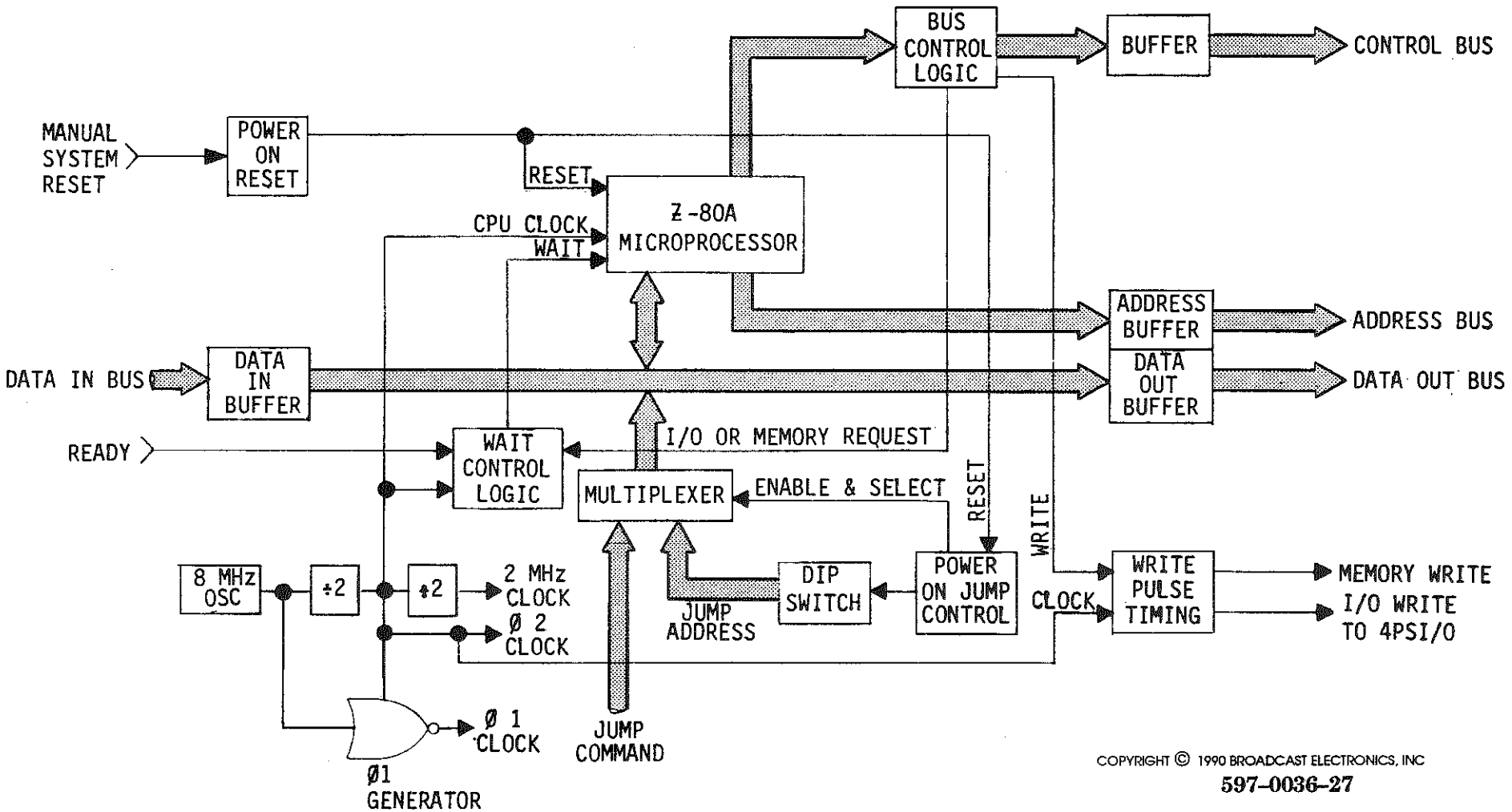



**FIGURE 4–5. CPU CIRCUIT BOARD BLOCK DIAGRAM**

4–71. **OPERATION.** The Z–80A microprocessor has four output signals that indicate what the microprocessor is doing at any instant (refer to Schematic 919–0059). These four outputs are used to synchronize external logic to steer data as required by the microprocessor. These outputs are: 1) input or output request ($\overline{IORQ}$), 2) memory request ($\overline{MREQ}$), 3) write ($\overline{WR}$), and 4) read ($\overline{RD}$). These signals are gated together according to the following combinations to form the indication functions:

A. SOUT (status output) = ($\overline{WR}$)($\overline{IORQ}$)*. Indicates that the processor is outputting data to a port (S–100 bus pin No. 45). During this type of instruction execution, data is output on the data out bus, the port address is output on the address bus, and the processor write pulse ($\overline{PWR}$) provides timing to the external logic.

B. SINP (status input) = ($\overline{RD}$)($\overline{IORQ}$). Indicates that the processor is accepting data from a port (S–100 bus pin No. 46). During this type of instruction execution, data is input on the data in bus while the address is output on the address bus. The processor data bus in signal (PDBIN) provides timing to the external logic.

C. SMEMR (status memory read) = ($\overline{RD}$)($\overline{MREQ}$). Indicates that the processor is reading data from memory (S–100 bus pin No. 47). During this operation, the address of the data desired is output from the microprocessor on the address bus, and the data is read in on the data input bus. The processor data bus in signal (PDBIN) provides timing to the external memory element.

   There are many operations in which the microprocessor reads data from memory, and this operation is by far the most frequent. As all instructions for the microprocessor are stored in memory, each instruction must be read, one at a time, as each instruction is executed. The first operation of each instruction cycle is to read a specific instruction from memory. The microprocessor may also read data from memory during the execution of an instruction, depending on the instruction itself.

D. MWRITE (memory write) = ($\overline{PWR}$)($\overline{MREQ}$). Indicates that the microprocessor is writing data to memory (S–100 bus pin No. 68). During this operation, data is output on the data out bus, and the address in memory where the data is to be stored is output on the address bus.

* **NOTE:** The expression ($\overline{WR}$)($\overline{IORQ}$) indicates a logical ANDing of $\overline{WR}$ and $\overline{IORQ}$.

4–72. **Power–On Jump.** The power–on jump instruction causes an automatic jump to a switch–specified address upon power on or reset. The logic for this feature is composed of integrated circuits U13, U14, U21, and switch S1. Integrated circuit U13 is a quad, edge–triggered, type–D latch which is used as a three–bit shift register. U13 is clocked by the output of a quad NAND gate section of U6. When U13 is reset by the power–on reset logic, it causes a series of three bytes (8 bits X 3) of information to be placed on the CPU circuit board data bus in response to the first three read cycles that the CPU executes.

4–73. The first three read cycles after a reset to the microprocessor are the instruction fetch cycles for the first instruction to be executed. Integrated circuits U14 and U21 are multiplexer chips with inverting tri–state outputs. During each of the first three read cycles, these multiplexers put data onto the CPU circuit board data bus. This information consists of the inverse of either the A or B inputs to U14 and U21, depending on the position of switches S1A through S1H.

4–74. The reset pulse begins the power–on jump by resetting both the microprocessor chip and all states of U13. This causes all Q outputs to go LOW and all $\overline{Q}$ outputs to go HIGH. Because each successive read cycle will clock a HIGH into the next stage, three read pulses will cause all the stages to have a HIGH on their Q output and a LOW on the Q output.

4–75. The first microprocessor read cycle will read the complement of the A inputs to U14 and U21 into the microprocessor. This is a jump command. At the end of the first read cycle, the first stage of U12 will change states, changing the select input to each multiplexer.

4–76. The second microprocessor read cycle will read all LOW states into the microprocessor as all B inputs are HIGH. The position of switches S1A through S1H does not affect this second word because the $\overline{Q}$ output of the second stage is HIGH. At the end of the second read cycle, $\overline{Q}$ of the second stage is clocked LOW.

4–77. The third microprocessor read cycle will read the high–order byte (8 bits) of the jump command into the microprocessor. On bits where the switch input is open, a HIGH will be input to the multiplexer and a LOW will be placed on the CPU circuit board data bus. On bits where the switch input is closed, a LOW will be input to the multiplexer and a HIGH will be placed on the CPU circuit board data bus. At the end of the third read cycle, the last stage of U13 changes stages. This causes the automatic power–on jump (AUTOJ) cycle to be terminated. Program execution will now begin at the new address.

4–78. **Write Pulse Timing.** The processor write pulse ($\overline{PWR}$) provides timing to external logic for outputting data. The circuit operates as follows: Quad type–D latch U4 is connected as a three–bit shift register. When a write pulse from the microprocessor occurs, the pulse is shifted into the first section of U4 and causes the Q output to go LOW. Two clock pulses later, the Q output of the third stage of U4 will go high and terminate the $\overline{PWR}$ pulse. This forms a $\overline{PWR}$ pulse 0.5 microseconds long, occurring within the period of the microprocessor write pulse.

4–79. **Wait Logic.** U8, U1 and Y1 form a 4 MHz clock circuit which acts as a frequency reference for the microprocessor chip (U12). This circuitry also forms the basis of the wait logic which allows the microprocessor to operate at a rate faster than the rate at which the input/output logic and memory circuits operate.

4–80. For an internally generated wait, the $\overline{Q}$ output of the first stage of quad type–D edge–triggered latch U2 is connected to the D input. In this configuration, it divides the clock frequency by 2. This 2 MHz signal, along with the 4 MHz signal, are routed to the S–100 bus to synchronization for the other system circuit boards.

4–81. The second and third sections of U2 are connected as a two–bit shift register. With Q of the second section gated with $\overline{Q}$ of the third section, a pulse generator is formed. A LOW–going pulse, one clock period wide is generated each time the D input of the second section goes HIGH. The D input is the result of the function D = $(\overline{MREQ})(\overline{IORQ})$. Each time the microprocessor executes a cycle that involves access to memory, an input port, or an output port, one clock period pulse is generated at the output of U3. Thispulse is applied to inverter U5 to form a negative–going pulse ($\overline{WAIT}$) at the input of the microprocessor.

4–82. Through this mechanism, one wait state is automatically inserted into the microprocessor timing for each memory access and each input/output access. This wait state allows the microprocessor to operate at 4 MHz with memory access and input/output timing operating at 2 MHz. This increases the system performance without the additional cost of higher speed memory and input/output logic.

4–83. The external ready inputs can also place the microprocessor into a wait condition for as long as the input signal remains present. The two external ready inputs are external equipment ready (XRDY) and processor ready (PRDY). Both signals are gated together by U3 and synchronized with the CPU clock by the fourth stage of U2. The output from U5 is then gated with the automatic wait state pulse and applied through U5 to the microprocessor. A LOW on either of the circuit board inputs will place the microprocessor in the wait mode for the duration of the LOW input.

## 4–84. VIDEO MONITOR DISPLAY CIRCUIT BOARD.

4–85. **GENERAL.** The video display module (VDM) is a fully self–contained microprocessor–based display terminal board that accepts ASCII data and commands from the CPU circuit board (refer to Figure 4–6). The VDM stores the data and generates both composite video and separate TTL levels for horizontal sync, vertical sync, and video output. The VDM is interfaced through the S–100 bus to the main processor CPU. A port informs the CPU when the VDM is ready to receive data.

4–86. The VDM utilizes a Z–80A microprocessor to perform the logic functions such as data storage, line feed, carriage return, cursor addressing, and scrolling. It also utilizes a CRT 5027 CRT controller integrated circuit to provide the scanning necessary for character display and provides timing to generate vertical and horizontal synchronization pulses and blanking. The VDM supplies both composite signals to the CRT and separate TTL level synchronization and timing.

4–87. A 8K X 8 EPROM memory stores the microprocessor program and a second 8K X 8 EPROM functions as a character generator to control the individual dots that form the characters on the CRT display. Additional memory includes a 2K X 8 RAM which is accessed by the microprocessor as required during program execution.

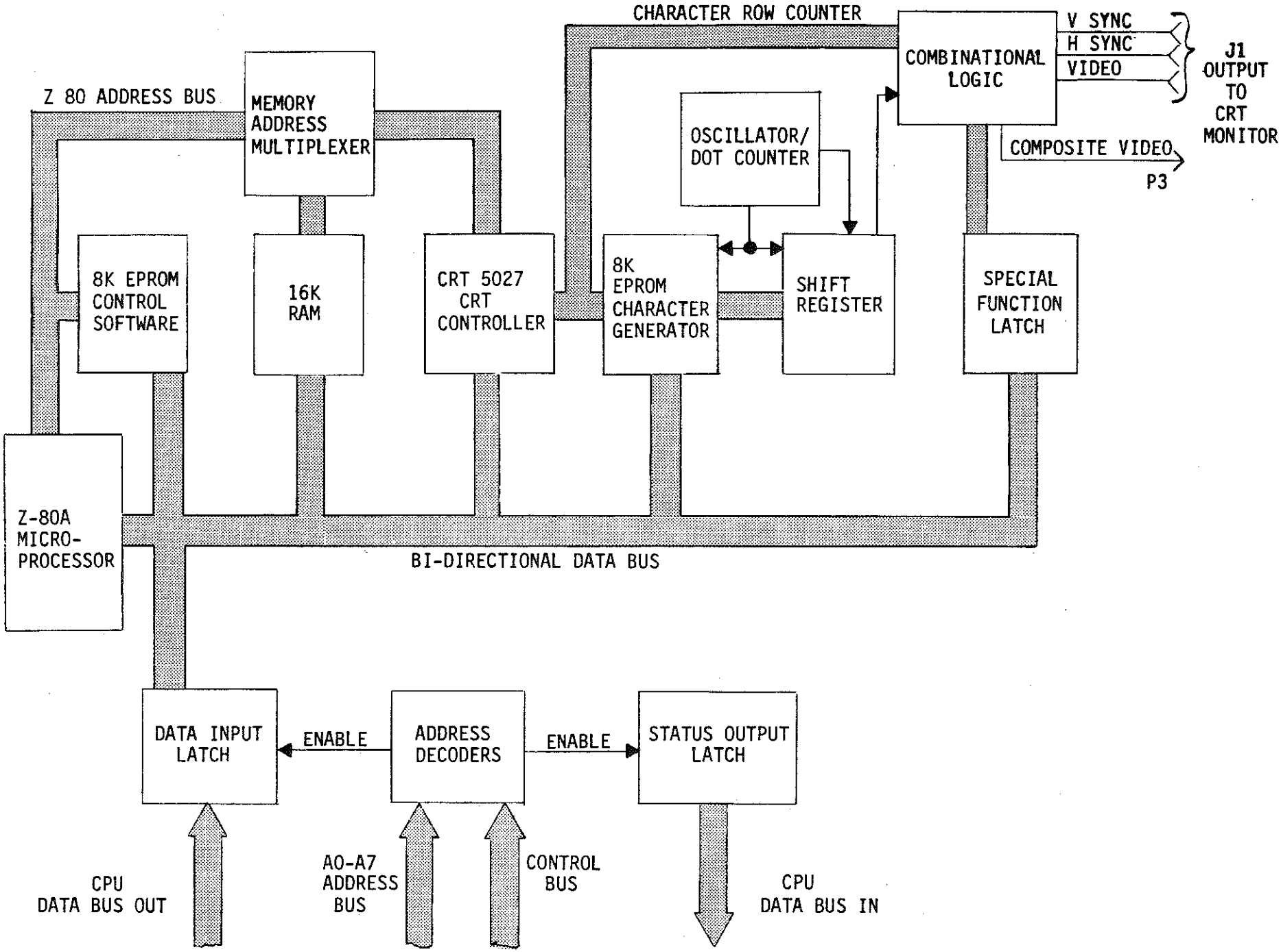
4–88. **OPERATION.** Information from the microprocessor to the VDM is written to hexadecimal address port address F9 (refer to Schematic 919–0036). The port address is decoded by U21, U22, U31, and U32. The decoded port address is gated with the status out (SOUT) signal and the processor write ($\overline{\text{PWR}}$) signal from the CPU to U21 which generates strobes to U20 and U30. U21 also gates the status input (SINP) signal and the processor data–bus–in (PDBIN) signal inputs with the port number to enable tri–state line driver U19.

4–89. Data on the microprocessor data out bus is latched into U30 by the strobe from U21 and U20 generates an interrupt to the Z–80A (U11) in response to its strobe. In addition, U20 controls the status sent back to the microprocessor through U19 when hexadecimal port address F8 is read by the microprocessor. The port number is decoded by the same port decoding circuitry as the port address.

4–90. In response to the interrupt request generated by U20, the microprocessor chip (U11) inputs the data stored in latch U30 and analyzes the data. U11 can then store the data into the 16k RAM (U24, U25, U26, and U27) if required.

4–91. Integrated circuits U8, U10, U18, U34, and portions of U22 and U23 form a memory address multiplexer. Under control of U11, the microprocessor can address the RAM through the multiplexer, or CRT controller U9 can address the RAM.

4–92. Two gates of U14 and Y1 are connected as a crystal stabilized oscillator which generates a 14.43098 MHz reference frequency. This frequency is a "dot clock" which generates timing for CRT controller U9. In addition, U12 and U14 form a divide–by–nine counter which outputs a "character clock". These two clocks determine that each character position will be 9 dot positions wide.




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597-0036-28

**FIGURE 4-6. VDM CIRCUIT BOARD BLOCK DIAGRAM**

4–93. The character clock output of U12 is routed to the dot counter carry input of U9. In addition, the dot counter carry signal is inverted and used to load data into U6, U13, and U29. U13 is a shift register that is loaded with parallel data from the character generator for each line of each character. It receives its first eight dots from character generator U28. The ninth dot will always be the same as the first because the H output and the serial input are connected together. The $\overline{H}$ output is pre–processed dot video as the shift register is clocked at the dot clock rate.

4–94. CRT controller chip U9 addresses RAM through the address multiplexer to scan across and down the screen as the sweep proceeds. Lines H0 through H6 address the horizontal characters, or the low order portion of RAM address. Output lines DR0 through DR4 address the vertical row, or the high order portion of RAM address.

4–95. The row address information is used as the low order portion of the address input for character generator U28. The high order portion of the address for the character generator is the lower seven bits of the word from RAM. The CRT controller chip address lines, the RAM, and the character clock latch the RAM data into U29. Therefore, the character generator U28 which then yields the dot pattern. This dot pattern is then loaded into shift register U13 and is shifted out as dot video.

4–96. CRT controller U9 also provides blanking, composite sync, vertical sync, and horizontal sync as outputs. The composite sync is gated in U36 and applied to latch U33 to generate a bus request–not ($\overline{BUSRQ}$) signal. Under normal conditions, the microprocessor (U11) will insert a HIGH in latch U33. This HIGH allows the microprocessor to access the data bus and the RAM only during sync pulse formation. In response to the $\overline{BUSRQ}$ input, U11 will output a bus acknowledge ($\overline{BUSAK}$) signal.

4–97. $\overline{BUSAK}$ signals the RAM address multiplexer that the microprocessor has suspended processing and has allowed CRT controller U9 to access the RAM address bus and the data bus to read information from RAM. When the composite sync pulse is output, the $\overline{BUSRQ}$ and therefore the $\overline{BUSAK}$ goes away, and the microprocessor is again allowed to access RAM.

4–98. Therefore, the microprocessor operates only during the low–going composite sync pulses, or when U11 writes a LOW into D7 of latch U33. With a LOW in U33, the latch output is gated with composite sync so that the microprocessor operation can not be suspended. The only time this occurs is when the microprocessor has a great deal of processing to perform. A clear screen function is an example of when a great deal of processing is required as all RAM must be cleared.

4–99. Integrated circuits U15 and U20 form a five–bit, divide–by–32 counter which operates from vertical sync. This counter generates an approximate 2 Hz signal which is used to generate a special effect when desired.

4–100. The highest order memory bit of the RAM data (D7) is used as an enhancement flag. This bit is loaded into U6 at the same time that U13 is loaded with dot information. The output of U6 indicates to the remaining logic circuitry which characters are to be enhanced. An example of enhanced characters are the reverse video characters that display the out–of–limit transmitter parameters. Active enhancement modes are controlled by the microprocessor which controls the output of latch U33. The following list details the meaning of each data bit.

| DATA BIT | LATCH Q | EFFECT |
|---|---|---|
| 4 | 7 | Controls the gate to the $\overline{\text{BUSRQ}}$ input of the microprocessor. |
| 4 | 2 | Underlines the enhanced characters (unused). |
| 3 | 5 | Causes all video to be blanked. |
| 2 | 6 | Causes all enhanced characters to appear in reverse video. |

4–101. The dot video is then inverted by U2, and depending upon the inputs to U3, the dot video may be inverted again. U3 is an exclusive OR gate which functions as a selective inverter. If pin 12 is LOW, the input will be output in a non–inverted condition. If pin 12 is HIGH, the input will in inverted.

4–102. The dot video from U3 is routed through another gate of U4 in which the video is gated with vertical sync which blanks the video during the vertical interval. The video is also gated with the blanking output of CRT controller U9 which blanks the video during the blanking portion of the horizontal sweep. The video is also gated with a third blanking signal through inverter U2 from U16. This signal gates together the enhancement flag from U6 and the blinking enhancement bit from U33. As the underline enhancement mode is not used in the MVDS, the fourth input to U16 is inactive.

4–103. Integrated circuit U17 gates together two different sets of conditions that can cause video reversal (used as a special effect to intensify or highlight a portion of the display screen). The first set of conditions generates the blinking underline cursor. U17 does this by gating together the blinking signal from U15, the cursor position from CRT controller U9, and the row 9 conditions. When all these conditions occur, the output of U17 will go HIGH, causing the video to be reversed in row 9 of the character designated by U9 as the cursor position.

4–104. The second set of conditions that generates reversed video involves the enhanced fields controlled by the microprocessor. When the enhancement flag is set and reverse video enhancement is selected, the output of U17 will go HIGH, causing the video reversal. Again, because underline enhancement is not used in the MVDS, the third input to U17 is not active.

4–105. The output circuit consists of transistor Q1 which mixes the composite sync from U9 with dot video from U4 to generate a 75 Ohm composite video output (video plus sync).

# SECTION V
# MVDS MAINTENANCE

## 5–1. INTRODUCTION.

5–2. This section provides maintenance information for the Broadcast Electronics MVDS.

## 5–3. SAFETY CONSIDERATIONS.

5–4. Low voltages are used throughout the MVDS circuit boards, however maintenance with power energized is always considered hazardous and caution should be observed. All high voltages used within the controller cabinet have been shielded, however do not touch any component within the controller cabinet with power energized. Good judgement, care, and common sense must be practiced to prevent accidents. The procedures contained in this section should be performed only by experienced and trained personnel.

5–5. If any MVDS maintenance requires removal of the controller cabinet or troubleshooting within the transmitter, refer to the applicable transmitter manual for safety and maintenance procedures. Never open the transmitter unless all primary power is disconnected.

## 5–6. MAINTENANCE.

***CAUTION*** ***INADVERTENT CONTACT BETWEEN ADJACENT COMPONENTS OR CIRCUIT BOARDS WITH TEST EQUIPMENT CAN CAUSE SERIOUS DAMAGE TO THE MVDS.***

***CAUTION***

### 5–7. PREVENTATIVE.

5–8. The preventative maintenance philosophy consists of regularly inspecting the MVDS for improperly seated circuit boards and semiconductors, and components damaged by overheating. Also, clean the circuit boards as required to prevent future failures.

### 5–9. ADJUSTMENTS.

***WARNING*** ***NEVER OPEN THE TRANSMITTER UNLESS ALL PRIMARY POWER IS DISCONNECTED.***

***WARNING***

5–10. The following text provides procedures to adjust all controls associated with the MVDS. The controls are located on the analog to digital circuit board. Adjustment procedures for the analog/digital circuit board are presented in the following text.

### 5–11. ANALOG/DIGITAL CIRCUIT BOARD ADJUSTMENTS.

5–12. **PA FORWARD POWER, PLATE VOLTAGE, AND PLATE CURRENT DIGITAL DISPLAY CALIBRATE (R43, R67, R94).** To calibrate the values of PA FORWARD POWER, PLATE VOLTAGE, and PLATE CURRENT displayed on the normal display screen to the transmitter analog meters, refer to the following procedure.

5–13. **Required Equipment.** The following equipment is required to adjust the PA FWD PWR, PLATE E, and PLATE I digital display calibrate controls (R43, R67, R94).

A. Insulated adjustment tool, flat–tip (BE P/N 407–0083).

5–14. **Procedure.** To adjust the controls, proceed as follows:

*NOTE* *ENSURE THE TRANSMITTER FORWARD POWER, PLATE VOLTAGE, AND PLATE CURRENT METERS*

*NOTE* *ARE CORRECTLY CALIBRATED BEFORE PROCEEDING.*

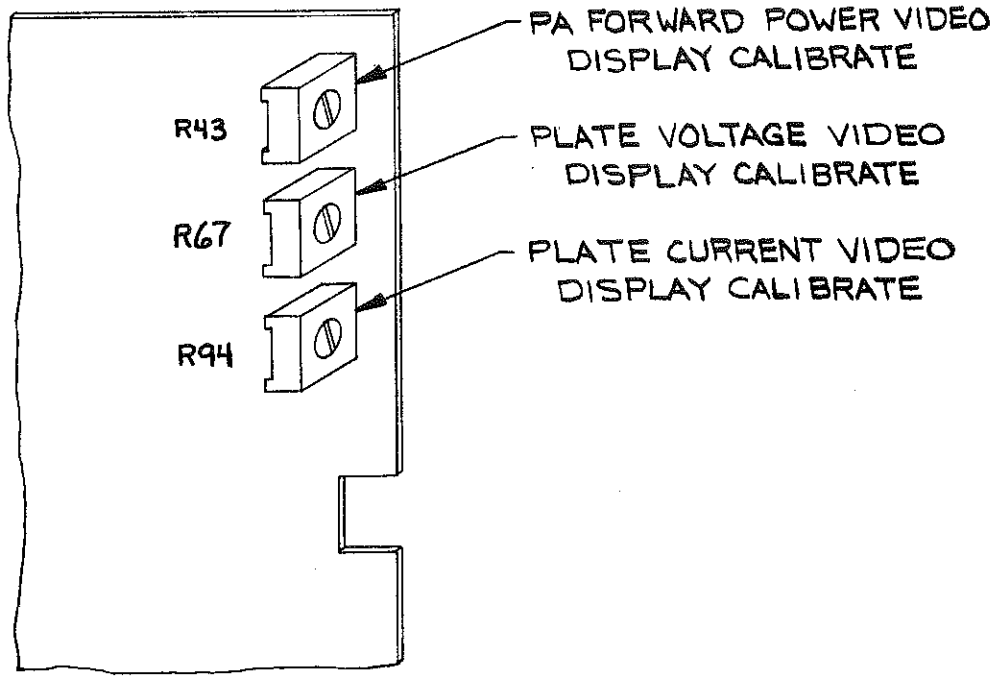
5–15. Apply power and operate the transmitter at the normal RF power.

5–16. Observe the transmitter OUTPUT POWER meter and the PA OUTPUT value displayed on the normal display screen.

5–17. Refer to Figure 5–1 and adjust R43 until the digital value displayed on the normal display screen is equal to the indication on the meter.

5–18. Repeat the R43 procedure for PLATE VOLTAGE and PLATE CURRENT, adjusting R67 and R94 until the value on the normal display screen is equal to the indication on the respective meter.

5–19. **ANALOG/DIGITAL CONVERTER OFFSET VOLTAGE ADJUST (R85, R86, R87).** Potentiometers R85, R86, and R87 adjust the analog/digital converter offset voltage. Due to the critical function of the offset voltage controls, field adjustment is not recommended. If adjustment is required, the analog/digital circuit board must be returned to the factory for calibration.




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC
597–0036–20

FIGURE 5–1. ANALOG/DIGITAL CIRCUIT BOARD CONTROLS

## 5–20. TROUBLESHOOTING.

5–21. Troubleshooting within the controller circuit board cage is not considered hazardous due to the low voltages and currents involved. All high voltages used within the controller cabinet have been shielded, however do not touch any component within the controller cabinet with power energized.

5–22. If any MVDS maintenance requires removal of the controller cabinet or troubleshooting within the transmitter, refer to the applicable transmitter manual for safety and maintenance procedures. Never open the transmitter unless all primary power is disconnected.

***NOTE***

***NOTE***

***WHEN MVDS IS DISABLED, ALL LOCAL AND REMOTE METER INDICATIONS WILL BE INACCURATE. TO CORRECT THE METER INDICATIONS, REMOVE CABLE W7 FROM THE ANALOG–TO–DIGITAL CONVERTER CIRCUIT BOARD.***

5–23. An extender circuit board with a reset switch is provided to assist troubleshooting. The reset switch clears all the digital circuitry which allows the system to generate new data. When the extender circuit board is not used, it must be inserted in the far left receptacle in the controller circuit board cage.

5–24. The troubleshooting philosophy for the MVDS consists of isolating a problem to a specific circuit board. The problem may be isolated by referencing the following warnings and Table 5–1 which lists specific symptoms and items to check.

**TABLE 5–1. MVDS TROUBLESHOOTING**

| SYMPTOM | ITEMS TO CHECK |
|---|---|
| Missing Video Display | Power supply, video monitor, video cables W6 and W10, and the VDM circuit board. |
| An Entire Highlighted Screen With Missing Video Display | Cable W11. |
| Flashing Video Display | CPU circuit board switch programming, micro–processor, 64K memory circuit board. |
| Unstable Data Values On Video Display | Cable W7, analog/digital circuit board. |
| Inoperative Keyboard | +5V keyboard supply at pin 11 on the EMI filter circuit board, keyboard cable, cable W8, input/output circuit board. |
| Disabled Logging | Correct log interface and status of logging system on the customer configuration screen, cable W8, cables to the logging devices, input/output circuit board. |

*WARNING*

*WARNING*

***NEVER OPEN THE TRANSMITTER UNLESS ALL POWER IS DISCONNECTED. USE THE GROUNDING STICKS PROVIDED TO ENSURE ALL COMPONENTS ARE DISCHARGED BEFORE ATTEMPTING ANY MAINTENANCE.***

*WARNING*

*WARNING*

***REMOVE ALL JEWELRY BEFORE TROUBLESHOOTING.***

*WARNING*

*WARNING*

***REMOVE ALL POWER BEFORE INSERTING OR REMOVING PRINTED CIRCUIT BOARDS OR REPLACING ANY COMPONENTS.***

*CAUTION*

*CAUTION*

***WHEN REPLACING A COMPONENT MOUNTED ON A HEATSINK, ENSURE A THIN FILM OF A ZINC–BASED HEATSINK COMPOUND IS USED (BE P/N 700–0028) TO ASSURE GOOD HEAT DISSIPATION.***

*CAUTION*

*CAUTION*

***INADVERTENT CONTACT BETWEEN ADJACENT COMPONENTS OR CIRCUIT BOARDS WITH TEST EQUIPMENT CAN CAUSE SERIOUS DAMAGE TO THE MVDS.***

*NOTE*

*NOTE*

***IF AN ANALOG/DIGITAL CONVERTER FAILS, THE ANALOG/DIGITAL CIRCUIT BOARD MUST BE RETURNED TO THE FACTORY FOR REPAIR.***

5–25. Once the trouble is isolated and power is totally deenergized, it is suggested that the exact problem be located with resistance checks using the schematic diagrams and the theory of operation. The faulty component may be repaired locally or the entire device may be returned to Broadcast Electronics, Inc. for repair or replacement.

5–26. **COMPONENT REPLACEMENT.** Refer to Section V of the applicable transmitter manual for the component replacement procedure.

# SECTION VI
# PARTS LIST

## 6–1. INTRODUCTION.

6–2. This section provides descriptions and part numbers of parts and assemblies required for maintenance of the Broadcast Electronics MVDS. Each table entry in this section is indexed by the reference designators of the applicable schematic diagram.

6–3. Table 6–1 indexes all tables listing assemblies and subassemblies having replaceable parts, the table number listing the parts, and the page number of the applicable table.

**TABLE 6–1. REPLACEABLE PARTS LIST INDEX**


| TABLE NO. | DESCRIPTION | PART NO. | PAGE |
|---|---|---|---|
| 6–2 | MICROPROCESSOR VIDEO DIAGNOSTICS SYSTEM | 909–0091–XXX | 6–2 |
| 6–3 | ASSEMBLY, MICROPROCESSOR VIDEO DIAGNOSTICS SYSTEM OPTION | 959–0298–001 | 6–2 |
| 6–4 | MICROPROCESSOR MOTHERBOARD ASSEMBLY | 919–0023 | 6–2 |
| 6–5 | VIDEO DISPLAY MODULE CIRCUIT BOARD ASSEMBLY | 919–0036 | 6–2 |
| 6–6 | INPUT FILTER CIRCUIT BOARD ASSEMBLY | 919–0057 | 6–4 |
| 6–7 | ANALOG/DIGITAL CIRCUIT BOARD ASSEMBLY | 919–0058/ –001 | 6–5 |
| 6–8 | CENTRAL PROCESSOR UNIT CIRCUIT BOARD ASSEMBLY | 919–0059 | 6–8 |
| 6–9 | INPUT/OUTPUT CIRCUIT BOARD ASSEMBLY | 919–0024 | 6–9 |
| 6–10 | 64K MEMORY CIRCUIT BOARD ASSEMBLY | 919–0110 | 6–11 |
| 6–11 | CABLE ASSEMBLY, FM MICROPROCESSOR | 949–0191–001 | 6–12 |
| 6–12 | ASSEMBLY, EXHAUST AIR TEMPERATURE SENSOR | 919–0082 | 6–12 |
| 6–13 | SOFTWARE KIT, MVDS VDM, 60 Hz | 979–0113 | 6–13 |
| 6–14 | SOFTWARE KIT, MVDS VDM, 50 Hz | 979–0112 | 6–13 |
| 6–15 | SOFTWARE KIT, FM–30B | 979–0091–014 | 6–13 |
| 6–16 | SOFTWARE KIT, FM–3.5B | 979–0091–024 | 6–13 |
| 6–17 | SOFTWARE KIT, FM–5B | 979–0091–034 | 6–13 |
| 6–18 | SOFTWARE KIT, FM10B | 979–0091–054 | 6–14 |
| 6–19 | SOFTWARE KIT, FM–35B | 979–0091–064 | 6–14 |
| 6–20 | SOFTWARE KIT, FM–20B | 979–0091–074 | 6–14 |

## TABLE 6–2. MICROPROCESSOR VIDEO DIAGNOSTICS SYSTEM – 909–0091–XXX

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| —— | Assembly, Microprocessor Video Diagnostics System | 959–0298–001 | 1 |
| —— | Assembly, Exhaust Air Temperature Sensor | 919–0082 | 1 |
| | **DELETE** | | |
| —— | Assembly, Transmitter Controller | 959–0298–002 | 1 |

## TABLE 6–3. ASSEMBLY, MICROPROCESSOR VIDEO DIAGNOSTICS SYSTEM OPTION – 959–0298–001

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| —— | Pin Connector | 417–0036 | 5 |
| —— | Power Supply MVDS System, HCAA–60W–A:<br>AC Input: 200/120/220/230–240 Vac, 47–63 Hz<br>DC Output: +5V @ 6A, +15V @ 1A, –15V @ 1A | 540–0001 | 1 |
| —— | Fuse, AGC, 2 Ampere, Slow–Blow | 334–0200 | 2 |
| —— | Connector, 15–Pin | 418–2379 | 1 |
| —— | Receptacle, 2 Pole Insert | 417–1507 | 1 |
| —— | Microprocessor Motherboard Assembly | 919–0023 | 1 |
| —— | Video Display Module Circuit Board Assembly | 919–0036 | 1 |
| —— | Input Filter Circuit Board Assembly | 919–0057 | 1 |
| —— | Analog/Digital Circuit Board Assembly | 919–0058 | 1 |
| —— | Central Processor Unit Circuit Board Assembly | 919–0059 | 1 |
| —— | Input/Output Circuit Board Assembly | 919–0024 | 1 |
| —— | 64K Memory Circuit Board Assembly | 919–0110 | 1 |
| —— | Keyboard, Serial No: ASCII | 808–4003 | 1 |
| —— | Assembly, Monitor | 809–7020 | 1 |
| —— | Cable Assembly, FM Microprocessor | 949–0191–001 | 1 |
| —— | Cable Assembly, Controller (Refer to Transmitter Manual) | 959–0294 | 1 |
| —— | Assembly, Basic Controller (Refer to Transmitter Manual) | 959–0298 | 1 |
| —— | Software Kit, MVDS | 979–0091–XXX | 1 |

## TABLE 6–4. MICROPROCESSOR MOTHERBOARD ASSEMBLY – 919–0023

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| J2 THRU J7 | Connector, 100–Pin | 418–5001 | 6 |
| —— | Connector, 6–Pin | 417–0677 | 1 |
| —— | Blank Circuit Board | 519–0023 | 1 |

## TABLE 6–5. VIDEO DISPLAY MODULE CIRCUIT BOARD ASSEMBLY – 919–0036
**(Sheet 1 of 3)**

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| C1 THRU C6, C9 THRU C13 | Capacitor, Ceramic Monolithic, 0.1 uF ±20%, 100V | 003–1054 | 11 |
| C14 | Capacitor, Electrolytic, 10 uF ±20%, 25V, Tantalum | 063–1074 | 1 |
| C15 THRU C18 | Capacitor, Ceramic Monolithic, 0.1 uF ±20%, 100V | 003–1054 | 4 |
| C19,C20 | Capacitor, Electrolytic, 10 uF ±20%, 25V, Tantalum | 063–1074 | 2 |
| C23 | Capacitor, Ceramic Monolithic, 0.1 uF ±20%, 100V | 003–1054 | 1 |
| C24 | Capacitor, Electrolytic, 10 uF ±20%, 25V, Tantalum | 063–1074 | 1 |
| C25 | Capacitor, Ceramic, 10 pF ±10%, 1 kV | 001–1014 | 1 |

## TABLE 6–5. VIDEO DISPLAY MODULE CIRCUIT BOARD ASSEMBLY – 919–0036
(Sheet 2 of 3)

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| C26 | Capacitor, Mica, 1000 pF ±5%, 500W Vdc | 041–1032 | 1 |
| CR2 | Diode, 1N4148, Silicon, 75V, 0.3 Amperes | 203–4148 | 1 |
| J2 | Header, 3–Pin | 417–0003 | 1 |
| J3 | Connector, BNC, 90° Angle | 417–0037 | 1 |
| P2 | Jumper, Programmable | 340–0004 | 1 |
| Q1 | Transistor, 2N3904, Silicon, NPN, TO–92 Case | 211–3904 | 1 |
| R1,R2 | Resistor, 2.2 k Ohm ±5%, 1/4W | 100–2243 | 2 |
| R3 | Resistor, 100 Ohm ±5%, 1/4W | 100–1033 | 1 |
| R4 | Resistor, 2.2 k Ohm ±5%, 1/4W | 100–2243 | 1 |
| R5 | Resistor, 1.5 k Ohm ±5%, 1/4W | 100–1543 | 1 |
| R6 THRU R8 | Resistor, 560 Ohm ±5%, 1/4W | 100–5633 | 3 |
| R10 THRU R12 | Resistor, 2.2 k Ohm ±5%, 1/4W | 100–2243 | 3 |
| R13 | Resistor, 22 k Ohm ±5%, 1/4W | 100–2253 | 1 |
| R14 | Resistor, 4.7 k Ohm ±5%, 1/4W | 100–4743 | 1 |
| R15 | Resistor, 2.2 k Ohm ±5%, 1/4W | 100–2243 | 1 |
| R16 | Resistor, 75 Ohm ±1%, 1/4W | 103–7502 | 1 |
| RP1 | Resistor Network, AB210A103, 10 k Ohm, Single–In–Line Package, 10–Pin | 226–1050 | 1 |
| U2 | Integrated Circuit, SN74LS04N, Schottky Hex Inverter, 14–Pin DIP | 228–2404 | 1 |
| U3 | Integrated Circuit, SN74LS86N, Quad 2–Input XOR, Schottky, 14–Pin | 228–2486 | 1 |
| U4 | Integrated Circuit, SN7425N, Dual 4–Input, NOR Gate, 14–Pin DIP | 228–0009 | 1 |
| U6 | Integrated Circuit, 74LS74N, Dual D–Type Flip–FLOP, 14–Pin | 228–0074 | 1 |
| U8 | Integrated Circuit, SN74LS157N, Schottky Quad 2–Line to 1–Line Data Selector, 16–Pin DIP | 228–0007 | 1 |
| U9 | Integrated Circuit, CRT5027, Timing and Control, 40–Pin DIP | 228–0013 | 1 |
| U10 | Integrated Circuit, SN74LS157N, Schottky Quad 2–Line to 1–Line Data Selector, 16–Pin DIP | 228–0007 | 1 |
| U11 | Integrated Circuit, Z80A, 40–Pin DIP | 229–3880 | 1 |
| U12 | Integrated Circuit, SN74163N, 4–Bit Synchronous Counter, 16–Pin DIP | 228–0011 | 1 |
| U13 | Integrated Circuit, SN74LS165N, Schottky 8–Bit Shift Register, 16–Pin DIP | 228–0004 | 1 |
| U14 | Integrated Circuit, SN74SO4N, Schottky Hex Inverter, 14–Pin | 228–0008 | 1 |
| U15 | Integrated Circuit, SN74LS93N, Schottky 4–Bit Counter, 14–Pin DIP | 228–0010 | 1 |
| U16 | Integrated Circuit, SN74LS20N, Dual 4–Input, Schottky, 14–Pin DIP | 228–2420 | 1 |
| U17 | Integrated Circuit, SN74LS10N, 3–Input NAND Gate, Schottky, 14–Pin DIP | 228–2410 | 1 |
| U18 | Integrated Circuit, SN74LS157N, Schottky Quad 2–Line to 1–Line Data Selector, 16–Pin DIP | 228–0007 | 1 |
| U19 | Integrated Circuit, SN74LS368N, Hex Bus Driver Schottky, 16–Pin DIP | 228–0002 | 1 |
| U20 | Integrated Circuit, 74LS74N, Dual D–Type Flip–Flop, 14–Pin | 228–0074 | 1 |
| U21 | Integrated Circuit, SN74LS155N, Schottky Decoder–Demulti–plexer, 16–Pin DIP | 228–0006 | 1 |
| U22 | Integrated Circuit, SN74LS04N, Schottky Hex Inverter, 14–Pin DIP | 228–2404 | 1 |
| U23 | Integrated Circuit, SN74LS00N, Quad NAND Gate, Schottky, 14–Pin DIP | 228–2400 | 1 |
| U24 THRU U27 | Integrated Circuit, MM2114, 1024 X 4–Bit Static RAM, 18–Pin DIP | 228–0012 | 4 |

## TABLE 6–5. VIDEO DISPLAY MODULE CIRCUIT BOARD ASSEMBLY – 919–0036
(Sheet 3 of 3)

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| U29 | Integrated Circuit, SN74LS273N, Octal D–Type Latch, Schottky, 20–Pin DIP | 228–0003 | 1 |
| U30 | Integrated Circuit, SN74LS373N, Octal D–Type Latch, Schottky, 20–Pin DIP | 228–0001 | 1 |
| U31 | Integrated Circuit, SN74LS14N, Hex Schmitt–Trigger Inverter, 14–Pin DIP | 228–2414 | 1 |
| U32 | Integrated Circuit, SN74LS20N, Dual 4–Input, Schottky, 14–Pin DIP | 228–2420 | 1 |
| U33 | Integrated Circuit, SN74LS273N, Octal D–Type Latch, Schottky, 20–Pin DIP | 228–0003 | 1 |
| U34 | Integrated Circuit, SN74LS157N, Schottky Quad 2–Line to 1–Line Data Selector, 16–Pin DIP | 228–0007 | 1 |
| U35 | Integrated Circuit, SN74LS139N, Schottky Dual 2–Line to 4–Line Decoder, 16–Pin DIP | 228–0005 | 1 |
| U36 | Integrated Circuit, SN74LS00N, Quad NAND Gate, Schottky, 14–Pin DIP | 228–2400 | 1 |
| VR1 | Voltage Regulator, MC7812CK, 12V, 1.5 Ampere | 227–7812 | 1 |
| XU2 THRU XU6 | Receptacle, 14–Pin DIP | 417–1404 | 5 |
| XU7 | Receptacle, 28–Pin DIP | 417–2804 | 1 |
| XU8 | Receptacle, 16–Pin DIP | 417–1604 | 1 |
| XU9 | Receptacle, 40–Pin DIP | 417–4005 | 1 |
| XU10 | Receptacle, 16–Pin DIP | 417–1604 | 1 |
| XU11 | Receptacle, 40–Pin DIP | 417–4005 | 1 |
| XU12,XU13 | Receptacle, 16–Pin DIP | 417–1604 | 2 |
| XU14 THRU XU17 | Receptacle, 14–Pin DIP | 417–1404 | 4 |
| XU18,XU19 | Receptacle, 16–Pin DIP | 417–1604 | 2 |
| XU20 | Receptacle, 14–Pin DIP | 417–1404 | 1 |
| XU21 | Receptacle, 16–Pin DIP | 417–1604 | 1 |
| XU22,XU23 | Receptacle, 14–Pin DIP | 417–1404 | 2 |
| XU24 THRU XU27 | Receptacle, 18–Pin DIP | 417–1804 | 4 |
| XU28 | Receptacle, 28–Pin DIP | 417–2804 | 1 |
| XU29,XU30 | Receptacle, 20–Pin DIP | 417–2004 | 2 |
| XU31,XU32 | Receptacle, 14–Pin DIP | 417–1404 | 2 |
| XU33 | Receptacle, 20–Pin DIP | 417–2004 | 1 |
| XU34,XU35 | Receptacle, 16–Pin DIP | 417–1604 | 2 |
| XU36 | Receptacle, 14–Pin DIP | 417–1404 | 1 |
| Y1 | Crystal, 14.43098 MHz ±0.05% @ 20 to 50°C, AT Cut, NE18A Case | 390–0005 | 1 |
| —— | Kit, MVDS Software | 979–0113 | 1 |
| —— | Blank Circuit Board | 518–6351 | 1 |

## TABLE 6–6. INPUT FILTER CIRCUIT BOARD ASSEMBLY – 919–0057
(Sheet 1 of 2)

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| C1 THRU C20 | Capacitor, Mica, 390 pF ±5%, 100V | 042–3922 | 20 |
| C21 | Capacitor, Electrolytic, 10 uF, 16V | 013–1074 | 1 |
| C22 THRU C28 | Capacitor, Mica, 390 pF ±5%, 100V | 042–3922 | 7 |
| C29 | Capacitor, Mylar Film, 0.1 uF, 100V | 030–1053 | 1 |
| C30 THRU C60 | Capacitor, Mica, 390 pF ±5%, 100V | 042–3922 | 31 |

## TABLE 6–6. INPUT FILTER CIRCUIT BOARD ASSEMBLY – 919–0057
## (Sheet 2 of 2)

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| D1 | Diode, 1N4005, Silicon, 600V @ 1 Ampere | 203–4005 | 1 |
| J1 THRU J4 | Connector, 25–Pin | 417–2500 | 4 |
| J8 | Header, 2–Pin, 90° Angle | 417–0075 | 1 |
| L1 THRU L28 | Choke, RF: 4.7 uH, 430 mA<br>DC Resistance: 0.55 Ohms<br>Resonant Frequency: 115 MHz | 360–0022 | 28 |
| —— | Integrated Circuit, MC1805CT, Voltage Regulator, 5V @ 1.0 Ampere, TO–220 Case | 227–7805 | 1 |
| —— | Plug, Keying AMP 206509–1 | 417–0090 | 4 |
| —— | Blank Circuit Board | 519–0057 | 1 |

## TABLE 6–7. ANALOG/DIGITAL CIRCUIT BOARD ASSEMBLIES
## FM–3.5B, FM–5B/5BS, FM–10B – 919–0058,
## FM–20B, FM–30B, FM–35B – 919–0058–001 (Sheet 1 of 3)

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| C1 THRU C16 | Capacitor, Electrolytic, 10 uF, 35V | 023–1076 | 16 |
| C24 | Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V | 003–1054 | 1 |
| C25 | Capacitor, Electrolytic, 100 uF ±10%, 25V | 023–1085 | 1 |
| C26 THRU C28 | Capacitor, Electrolytic, 4.7 uF, 35V | 024–4764 | 3 |
| C29 THRU C39 | Capacitor, Mylar Film, .01 uF ±10%, 100V | 031–1043 | 11 |
| C45 | Capacitor, Electrolytic, 47 uF, 35V | 020–4770 | 1 |
| C46 | Capacitor, Electrolytic, 100 uF ±10%, 16V | 020–1082 | 1 |
| C47 | Capacitor, Electrolytic, 47 uF, 35V | 020–4770 | 1 |
| C48 THRU C56 | Capacitor, Mylar Film, .01 uF ±10%, 100V | 031–1043 | 9 |
| D1 THRU D16, D24 THRU D39 | Diode, 1N4148, Silicon, 75V, 0.3 Ampere | 203–4148 | 32 |
| J2,J3,J6 THRU J10 | Header, 3–Pin | 417–0003 | 7 |
| J11 | Header, 2–Pin | 417–4004 | 1 |
| P2,P3,P6 THRU P11 | Jumper, Programmable | 340–0004 | 8 |
| Q1 | Transistor, 2N3904, Silicon, NPN, TO–92 Case | 211–3904 | 1 |
| R1 THRU R16 | Resistor, 10 k Ohm ±1%, 1/4W | 100–1051 | 16 |
| R24 | Resistor, 1.21 k Ohm ±1%, 1/4W | 103–1214 | 1 |
| R25,R26 | Resistor, 10 k Ohm ±1%, 1/4W | 100–1051 | 2 |
| R27 | Resistor, 23.2 k Ohm ±1%, 1/4W | 103–2325 | 1 |
| R31 | Resistor, 8.66 k Ohm ±1%, 1/4W | 100–8641 | 1 |
| R32 THRU R34 | Resistor, 10 k Ohm ±1%, 1/4W | 100–1051 | 3 |
| R35 | Resistor, 1 Meg Ohm ±1%, 1/4W | 103–1007 | 1 |
| R36 | Resistor, 10 k Ohm ±1%, 1/4W | 100–1051 | 1 |
| R37 | Resistor, 210 k Ohm ±1%, 1/4W | 103–2106 | 1 |
| R41 | Resistor, 10 k Ohm ±1%, 1/4W | 100–1051 | 1 |
| R42 | Resistor, 4.99 k Ohm ±1%, 1/4W | 100–5041 | 1 |
| R43 | Potentiometer, 2 k Ohm ±10%, 1/2W | 178–2044 | 1 |

## TABLE 6–7. ANALOG/DIGITAL CIRCUIT BOARD ASSEMBLIES FM–3.5B, FM–5B/5BS, FM–10B – 919–0058, FM–20B, FM–30B, FM–35B – 919–0058–001 (Sheet 2 of 3)

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| R45,R46 | Resistor, 10 k Ohm ±1%, 1/4W | 100–1051 | 2 |
| R47 | Resistor, 12.7 k Ohm ±1%, 1/4W | 103–1275 | 1 |
| R48,R53 | Resistor, 10 k Ohm ±1%, 1/4W | 100–1051 | 2 |
| R54 | Resistor, 9.09 k Ohm ±1%, 1/4W | 103–9041 | 1 |
| R55 | Resistor, 10 k Ohm ±1%, 1/4W | 100–1051 | 1 |
| R56 | Resistor, 8.25 k Ohm ±1%, 1/4W | 103–8254 | 1 |
| R57,R58, R60,R61,R62 | Resistor, 10 k Ohm ±1%, 1/4W | 100–1051 | 5 |
| R67 | Potentiometer, 1 k Ohm ±10%, 1/2W | 178–1043 | 1 |
| R68 | Resistor, 9.31 k Ohm ±1%, 1/4W | 103–9314 | 1 |
| R69 | Resistor, 6650 Ohm ±1%, 1/4W | 103–6641 | 1 |
| R70 | Resistor, 9.09 k Ohm ±1%, 1/4W | 103–9041 | 1 |
| R71 | Resistor, 6650 Ohm ±1%, 1/4W | 103–6641 | 1 |
| R72 | Resistor, 10 k Ohm ±1%, 1/4W | 100–1051 | 1 |
| R73 | Resistor, 12.7 k Ohm ±1%, 1/4W | 103–1275 | 1 |
| R74 | Resistor, 4.7 k Ohm ±5%, 1/4W | 100–4743 | 1 |
| R75 | Resistor, 130 k Ohm ±1%, 1/4W | 103–1306 | 1 |
| R77 | Resistor, 100 k Ohm ±1%, 1/4W | 103–1062 | 1 |
| R78 | Resistor, 20 k Ohm ±1%, 1/4W | 103–2051 | 1 |
| R79 | Resistor, 8.25 k Ohm ±1%, 1/4W | 103–8254 | 1 |
| R80,R81 | Resistor, 10 k Ohm ±1%, 1/4W | 100–1051 | 2 |
| R82 | Resistor, 8.25 k Ohm ±1%, 1/4W | 103–8254 | 1 |
| R84 | Resistor, 4.7 k Ohm ±5%, 1/4W | 100–4743 | 1 |
| R85,R86 | Potentiometer, 100 Ohm ±10%, 1/2W | 177–1034 | 2 |
| R88 | Resistor, 220 k Ohm ±5%, 1/4W | 100–2263 | 1 |
| R89 | Resistor, 20 k Ohm ±1%, 1/4W | 103–2051 | 1 |
| R90 | Resistor, 100 k Ohm ±1%, 1/4W | 103–1062 | 1 |
| R91 | Resistor, 4.7 k Ohm ±5%, 1/4W | 100–4743 | 1 |
| R92 | Resistor, 100 Ohm ±5%, 1/4W | 100–1033 | 1 |
| R93 | Resistor, 10 k Ohm ±5%, 1/4W | 100–1053 | 1 |
| R95,R96 | Resistor, 1 Meg Ohm ±1%, 1/4W | 103–1007 | 2 |
| R97 | Resistor, 6650 Ohm ±1%, 1/4W | 103–6641 | 1 |
| R98 | Resistor, 56.2 k Ohm ±1%, 1/4W | 103–5651 | 1 |
| U1 THRU U10,U14 | Integrated Circuit, TL072CP, Dual Operational Amplifier, 8–Pin DIP | 221–0072 | 11 |
| U16 | Integrated Circuit, AD581KH, Negative 10V Precision Regulator, TO–5 Case | 220–0581 | 1 |
| U17 | Integrated Circuit, SN74LS04N, Low–Power Schottky Hex Inverter, 14–Pin DIP | 228–2404 | 1 |
| U18 | Integrated Circuit, SN74LS00N, Low–Power Quad NAND Gate, 14–Pin DIP | 228–2400 | 1 |
| U19 | Integrated Circuit, SN74LS20N, Schottky Dual 4–Input NAND Gate, 14–Pin DIP | 228–2420 | 1 |
| U20 | Integrated Circuit, SN74LS30N, Schottky 8–Input NAND Gate, 14–Pin DIP | 228–2430 | 1 |
| U21,U22 | Integrated Circuit, SN74LS244N, Octal Tri–State Bus Driver, 20–Pin DIP | 228–2244 | 2 |
| U23 | Integrated Circuit, SN74LS42N, BCD–To–Decimal Decoder, 16–Pin DIP | 228–2442 | 1 |
| U24 | Integrated Circuit, 74LS74N, Dual D–Type Flip–Flop, 14–Pin DIP | 228–0074 | 1 |
| U25 | Integrated Circuit, 74LS123, Schottky Dual Monostable Multivibrator, 16–Pin DIP | 220–2123 | 1 |

## TABLE 6–7. ANALOG/DIGITAL CIRCUIT BOARD ASSEMBLIES FM–3.5B, FM–5B/5BS, FM–10B – 919–0058, FM–20B, FM–30B, FM–35B – 919–0058–001 (Sheet 3 of 3)

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| U26,U27 | Integrated Circuit, AD7581LN, 8–Channel A–D Converter, CMOS, 28–Pin DIP | 220–7581 | 2 |
| XU1 THRU XU10,XU14 | Socket, 8–Pin DIP | 417–0804 | 11 |
| XU17 THRU XU20 | Socket, 14–Pin DIP | 417–1404 | 4 |
| XU21,XU22 | Socket, 20–Pin DIP | 417–2004 | 2 |
| XU23 | Socket, 16–Pin DIP | 417–1604 | 1 |
| XU24 | Socket, 14–Pin DIP | 417–1404 | 1 |
| XU25 | Socket, 16–Pin DIP | 417–1604 | 1 |
| XU26,XU27 | Socket, 28–Pin DIP | 417–2804 | 2 |
| —— | Pad, Transistor Mounting, TO–18 Case | 409–0121 | 1 |
| —— | Blank Circuit Board | 519–0058 | 1 |
| | **ADDITIONAL PARTS FOR ANALOG/DIGITAL CIRCUIT BOARD ASSEMBLY – 919–0058** | | |
| R44 | Resistor, 102 k Ohm ±1%, 1/4W | 103–1026 | 1 |
| R47 | Resistor, 12.7 k Ohm ±1%, 1/4W | 103–1275 | 1 |
| R59 | Resistor, 10 k Ohm ±1%, 1/4W | 100–1051 | 1 |
| R73 | Resistor, 12.7 k Ohm ±1%, 1/4W | 103–1275 | 1 |
| R76 | Resistor, 20 k Ohm ±1%, 1/4W | 103–2051 | 1 |
| R94 | Potentiometer, 5 k Ohm ±10%, 1/2W | 178–5043 | 1 |
| | **ADDITIONAL PARTS FOR ANALOG/DIGITAL CIRCUIT BOARD ASSEMBLY – 919–0058–001** | | |
| C17 THRU C23 | Capacitor, Electrolytic, 10 uF, 35V | 023–1076 | 7 |
| C40 THRU C44 | Capacitor, Mylar, 0.01 uF ±10%, 100V | 031–1043 | 5 |
| D17 THRU D23,D40 THRU D46 | Diode, 1N4148, Silicon, 75V @ 0.3 Ampere | 203–4148 | 14 |
| J4 | Header, 3–Pin | 417–0003 | 1 |
| P4 | Jumper, Programmable | 340–0004 | 1 |
| R17 THRU R23,R28 THRU R30, R38,R39,R40 | Resistor, 10 k Ohm ±1%, 1/4W | 100–1051 | 13 |
| R44 | Resistor, 97.6 k Ohm ±1%, 1/4W | 100–9751 | 1 |
| R47 | Resistor, 12.7 k Ohm ±1%, 1/4W | 103–1275 | 1 |
| R49 THRU R52 | Resistor, 10 k Ohm ±1%, 1/4W | 100–1051 | 4 |
| R59 | Resistor, 24.9 k Ohm ±1%, 1/4W | 103–2495 | 1 |
| R63 THRU R66 | Resistor, 10 k Ohm ±1%, 1/4W | 100–1051 | 4 |
| R73 | Resistor, 12.7 k Ohm ±1%, 1/4W | 103–1275 | 1 |
| R76 | Resistor, 40.2 k Ohm ±1%, 1/4W | 103–4025 | 1 |
| R83 | Resistor, 8.25 k Ohm ±1%, 1/4W | 103–8254 | 1 |
| R87 | Potentiometer, 100 Ohm ±10%, 1/2W | 177–1034 | 1 |
| R94 | Potentiometer, 10 k Ohm ±10%, 1/2W | 178–1054 | 1 |
| U11 THRU U13,U15 | Integrated Circuit, TLO72CP, Dual Operational Amplifier, 8–Pin DIP | 221–0072 | 4 |

**ADDITIONAL PARTS FOR ANALOG/DIGITAL CIRCUIT BOARD ASSEMBLY – 919–0058–001 (Cont'd.)**

| | | | |
|---|---|---|---|
| U28 | Integrated Circuit, AD7581LN, 8–Channel A–D Converter, CMOS, 28–Pin DIP | 220–7581 | 1 |
| XU11 THRU XU13, XU15 | Socket, 8–Pin DIP | 417–0804 | 4 |
| XU28 | Socket, 28–Pin DIP | 417–2804 | 1 |

**TABLE 6–8. CENTRAL PROCESSOR UNIT CIRCUIT BOARD ASSEMBLY – 919–0059 (Sheet 1 of 2)**

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| C1 | Capacitor, Ceramic Disc, 10 pF ±10%, 1 kV | 001–1014 | 1 |
| C2 | Capacitor, Mica, 1000 pF ±5%, 500V | 041–1032 | 1 |
| C3,C4 | Capacitor, Electrolytic, 100 uF, 40V | 014–1084 | 2 |
| C5 THRU C22 | Capacitor, Ceramic, 0.1 uF +80 –20, 10V | 000–1055 | 18 |
| C23 | Capacitor, Mica, 33 pF ±5%, 500V | 042–3322 | 1 |
| D1 | Diode, 1N4148, Silicon, 75V, 0.3 Ampere | 203–4148 | 1 |
| Q1 | Transistor, 2N3906, PNP, Silicon, TO–92 Case | 210–3906 | 1 |
| R1,R2 | Resistor, 560 Ohm ±5%, 1/4W | 100–5633 | 2 |
| R3 | Resistor, 22 k Ohm ±5%, 1/4W | 100–2253 | 1 |
| R4 | Resistor, 100 Ohm ±5%, 1/4W | 100–1033 | 1 |
| R5,R14,R23 | Resistor Network, AB210A103, 10 k Ohm, Single–In–Line Package, 10–Pin | 226–1050 | 3 |
| R32 THRU R34 | Resistor, 1 k Ohm ±5%, 1/4W | 100–1043 | 3 |
| R35 | Resistor, 220 Ohm ±5%, 1/4W | 100–2233 | 1 |
| R36 | Resistor, 6.2 K Ohm ±5%, 1/4W | 100–1243 | 1 |
| S1 | Switch Assembly, SPST, 8–Position DIP | 340–0003 | 1 |
| U1,U2 | Integrated Circuit, SN74LS175N, Hex/Quad, Flip–Flop, 16–Pin DIP | 228–2175 | 2 |
| U3 | Integrated Circuit, SN74LS00N, Quad NAND Gate, 14–Pin DIP | 228–2400 | 1 |
| U4 | Integrated Circuit, SN74LS175N, Hex/Quad, Fkip–Flop, 16–Pin DIP | 228–2175 | 1 |
| U5 | Integrated Circuit, SN74LS04N, Hex Inverter, 14–Pin DIP | 228–2404 | 1 |
| U6 | Integrated Circuit, SN74LS00N, Quad NAND Gate, 14–Pin DIP | 228–2400 | 1 |
| U7 | Integrated Circuit, SN74LS02N, Quad NOR Gate, 14–Pin DIP | 228–2402 | 1 |
| U8 | Integrated Circuit, SN74LS04N, Hex Inverter, 14–Pin DIP | 228–2404 | 1 |
| U9 | Integrated Circuit, SN74LS244, Octal Tri–State Bus Driver, 20–Pin | 228–2244 | 1 |
| U10 | Integrated Circuit, SN74LS02N, Quad NOR Gate, 14–Pin DIP | 228–2402 | 1 |
| U11 | Integrated Circuit, SN74LS244, Octal Tri–State Bus Driver, | 228–2244 | 1 |
| U12 | Integrated Circuit, Z–80A, Central Processor Unit, 40–Pin DIP | 229–3880 | 1 |
| U13 | Integrated Circuit, SN74LS175N, Hex/Quad, Flip–Flop, 16–Pin DIP | 228–2175 | 1 |
| U14 | Integrated Circuit, SN74LS258, Quad 2–Input Multiplexer with Inverted Tri–State Outputs, 16–Pin | 228–2258 | 1 |
| U15 | Integrated Circuit, SN74LS14N, Hex Schottky Schmitt–Trigger Inverter, 14–Pin DIP | 228–2414 | 1 |
| U16 THRU U20 | Integrated Circuit, SN74LS244, Octal Tri–State Bus Driver, 20–Pin | 228–2244 | 5 |
| U21 | Integrated Circuit, SN74LS258, Quad 2–Input Multiplexer with Inverted Tri–State Outputs, 16–Pin | 228–2258 | 1 |
| XU1,XU2 | Receptacle, 16–Pin DIP | 417–1604 | 2 |
| XU3 | Receptacle, 14–Pin DIP | 417–1404 | 1 |
| XU4 | Receptacle, 16–Pin DIP | 417–1604 | 1 |
| XU5 THRU XU8 | Receptacle, 14–Pin DIP | 417–1404 | 4 |

## TABLE 6–8. CENTRAL PROCESSOR UNIT CIRCUIT BOARD ASSEMBLY – 919–0059
(Sheet 2 of 2)

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| XU9 | Receptacle, 20–Pin DIP | 417–2004 | 1 |
| XU10 | Receptacle, 14–Pin DIP | 417–1404 | 1 |
| XU11 | Receptacle, 20–Pin DIP | 417–2004 | 1 |
| XU12 | Receptacle, 40–Pin DIP | 417–4005 | 1 |
| XU13,XU14 | Receptacle, 16–Pin DIP | 417–1604 | 2 |
| XU15 | Receptacle, 14–Pin DIP | 417–1404 | 1 |
| XU16 THRU XU20 | Receptacle, 20–Pin DIP | 417–2004 | 5 |
| XU21 | Receptacle, 16–Pin DIP | 417–1604 | 1 |
| Y1 | Crystal, 8 MHz ±0.05% from +205C to +505C, A/T Cut, NE18A Case | 390–0018 | 1 |
| —— | Blank Circuit Board | 514–6300 | 1 |

## TABLE 6–9. INPUT/OUTPUT CIRCUIT BOARD ASSEMBLY – 919–0024
(Sheet 1 of 3)

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| C1 | Capacitor, Ceramic, 0.1 uF ±20%, 50V | 003–1054 | 1 |
| C3 THRU C6 | Capacitor, Ceramic, 0.1 uF ±20%, 50V | 003–1054 | 4 |
| C8 THRU C31 | Capacitor, Ceramic, 0.1 uF ±20%, 50V | 003–1054 | 24 |
| C32 | Capacitor, Tantalum, 47 uF ±20%, 6V | 061–4774 | 1 |
| C34,C35 | Capacitor, Ceramic, 0.1 uF ±20%, 50V | 003–1054 | 2 |
| C36,C37 | Capacitor, Ceramic Monolithic, 56 pF ±10%, 200V | 001–5613 | 2 |
| C38 THRU C48 | Capacitor, Ceramic, 0.1 uF ±20%, 50V | 003–1054 | 11 |
| C49 | Capacitor, Electrolytic, 10 uF, 35V | 023–1076 | 1 |
| C50 | Capacitor, Electrolytic, 1 uF, 50V | 024–1064 | 1 |
| C51 | Capacitor, Ceramic Disc, 100 pF, 100V | 002–1024 | 1 |
| D2 THRU D9 D12 THRU D17 | Diode, 1N4148, Silicon, Signal Switching, 75V @ 300 mA Maximum | 203–4148 | 14 |
| J5 THRU J7 | Header, 3–Pin | 417–0003 | 3 |
| P4 | Socket, 16–Pin | 417–1604 | 1 |
| P5 THRU P7 | Jumper, Programmable | 340–0004 | 3 |
| Q1 THRU Q7 | Transistor, 2N3904, Silicon, NPN, TO–92 Case | 211–3904 | 7 |
| R2,R3 | Resistor, 10 k Ohm ±5%, 1/4W | 100–1053 | 2 |
| R4 THRU R10 | Resistor, 4.7 k Ohm ±5%, 1/4W | 100–4743 | 7 |
| R14,R15 | Resistor, 1 k Ohm ±5%, 1/4W | 100–1043 | 2 |
| R17 | Resistor, 4.7 k Ohm ±5%, 1/4W | 100–4743 | 1 |
| R18 | Resistor, 10 k Ohm ±5%, 1/4W | 100–1053 | 1 |
| R19 THRU R23 | Resistor, 4.7 k Ohm ±5%, 1/4W | 100–4743 | 5 |
| R24 | Resistor, 68 k Ohm ±5%, 1/4W | 100–6853 | 1 |
| R25 THRU R27 | Resistor, 4.7 k Ohm ±5%, 1/4W | 100–4743 | 3 |
| R29 | Resistor, 10 k Ohm ±5%, 1/4W | 100–1053 | 1 |
| R30 | Resistor, 10 Meg Ohm ±5%, 1/4W | 100–1083 | 1 |
| R31 | Resistor, 470 k Ohm ±5%, 1/4W | 100–4763 | 1 |
| R32,R33 | Resistor, 100 Ohm ±5%, 1/4W | 100–1033 | 2 |
| R34 | Resistor, 4.7 k Ohm ±5%, 1/4W | 100–4743 | 1 |
| R35 | Resistor, 2.2 k Ohm ±5%, 1/4W | 100–2243 | 1 |

## TABLE 6–9. INPUT/OUTPUT CIRCUIT BOARD ASSEMBLY – 919–0024
(Sheet 2 of 3)

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| RN1 THRU RN3 | Resistor Network, 8–22 k Ohm 1/4W Resistors, 16–Pin DIP | 226–2250 | 3 |
| RN4 THRU RN6 | Resistor Network, AB210A103, 10 k Ohm, Single–In–Line Package, 10–Pin | 226–1050 | 3 |
| RN7 | Resistor Network, 8–22 k Ohm 1/4W Resistors, 16–Pin DIP | 226–2250 | 1 |
| RN8 | Resistor Network, AB210A103, 10 k Ohm, Single–In–Line Package, 10–Pin | 226–1050 | 1 |
| RN9 | Resistor Network, 8–22 k Ohm 1/4W Resistors, 16–Pin DIP | 226–2250 | 1 |
| RN10 | Resistor Network, AB210A103, 10 k Ohm, Single–In–Line Package, 10–Pin | 226–1050 | 1 |
| RN11 | Resistor Network, AB410A471, 9–470 Ohm 1/4W Resistors, Single–In–Line Package, 10–Pin | 226–0470 | 1 |
| S1 | Switch, 4–SPST, Side Adjust, 8–Pin DIP | 340–0013 | 1 |
| S2 THRU S4 | Switch, 8–SPST, 16–Pin DIP | 340–0003 | 3 |
| U1 | Integrated Circuit, 8255A, Programmable Peripheral Interface, 24 Parallel Input/Output Lines, 40–Pin DIP | 229–8255 | 1 |
| U2,U3 | Integrated Circuit, 14505, Hex Level Shifter, TTL to CMOS, 16–Pin DIP | 228–4504 | 2 |
| U4 | Integrated Circuit, CD4069CN, Hex Inverter, CMOS, 14–Pin DIP | 228–4069 | 1 |
| U5,U6 | Integrated Circuit, 14505, Hex Level Shifter, TTL to CMOS, 16–Pin DIP | 228–4504 | 2 |
| U7 THRU U9 | Integrated Circuit, 8255A, Programmable Peripheral Interface, 24 Parallel Input/Output Lines, 40–Pin DIP | 229–8255 | 3 |
| U10 | Integrated Circuit, SN7475N, 4–Bit Bistable Latch, 16–Pin DIP | 228–7475 | 1 |
| U11 THRU U13 | Integrated Circuit, 8251A, Universal Synchronous/Asynchronous Receiver/Transmitter (USART), NMOS, 28–Pin DIP | 229–8251 | 3 |
| U14 THRU U16 | Integrated Circuit, RC741DN, Operational Amplifier, 8–Pin DIP | 221–7410 | 3 |
| U17 | Integrated Circuit, SN74LS164N, 8–Bit Parallel Output Shift Register, TTL, 14–Pin DIP | 228–2164 | 1 |
| U18 | Integrated Circuit, SN7475N, 4–Bit Bistable Latch, 16–Pin DIP | 228–7475 | 1 |
| U19 | Integrated Circuit, SN74LS00N, Schottky Quad NAND Gate, 14–Pin DIP | 228–2400 | 1 |
| U20 | Integrated Circuit, SN74LS42N, Dual D–Type Flip–Flop, 14–Pin DIP | 228–2442 | 1 |
| U21 | Integrated Circuit, SN74LS123, Schottky Dual Monostable Multivibrator, 16–Pin DIP | 220–2123 | 1 |
| U22 | Integrated Circuit, DS1287, Real Time Clock with Built–In RAM and Battery Backup, 24–Pin DIP | 229–1287 | 1 |
| U23 | Integrated Circuit, 74LS04N, Low–Power Schottky Hex Inverter, 14–Pin DIP | 228–2404 | 1 |
| U24 | Integrated Circuit, F4702PC, Bit Rate Generator, CMOS, 16–Pin DIP | 228–8702 | 1 |
| U25 | Integrated Circuit, 93L34PC, 8–Bit Addressable Latch, 16–Pin DIP | 228–1034 | 1 |
| U26 | Integrated Circuit, SN74LS164N, 8–Bit Parallel Output Shift Register, TTL, 14–Pin DIP | 228–2164 | 1 |
| U27 | Integrated Circuit, SN74LS04N, Low–Power Schottky Hex Inverter, 14–Pin DIP | 228–2404 | 1 |
| U28 | Integrated Circuit, SN74LS20N, Schottky Dual 4–Input NAND Gate, 14–Pin DIP | 228–2420 | 1 |
| U29 | Integrated Circuit, SN74LS03N, Schottky NAND Gate with Open Collectors, 14–Pin DIP | 228–2403 | 1 |
| U30 | Integrated Circuit, SN74LS10N, Schottky Triple 3–Input NAND Gate, 14–Pin DIP | 228–2410 | 1 |
| U31 | Integrated Circuit, SN74LS14N, Schottky Hex Schmitt Trigger, 14–Pin DIP | 228–2414 | 1 |
| U32 | Integrated Circuit, SN74LS244N, Octal Tri–State Bus Driver, 20–Pin DIP | 228–2244 | 1 |

## TABLE 6–9. INPUT/OUTPUT CIRCUIT BOARD ASSEMBLY – 919–0024
(Sheet 3 of 3)

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| U33 | Integrated Circuit, SN74LS30N, Schottky 8–Input NAND Gate, TTL, 14–Pin DIP | 228–2430 | 1 |
| U34,U35 | Integrated Circuit, SN74LS244N, Octal Tri–State Bus Driver, 20–Pin DIP | 228–2244 | 1 |
| XU1 | Socket, 40–Pin DIP | 417–4005 | 1 |
| XU2,XU3 | Socket, 16–Pin DIP | 417–1604 | 2 |
| XU4 | Socket, 14–Pin DIP | 417–1404 | 1 |
| XU5,XU6 | Socket, 16–Pin DIP | 417–1604 | 2 |
| XU7 THRU XU9 | Socket, 40–Pin DIP | 417–4005 | 3 |
| XU10 | Socket, 16–Pin DIP | 417–1604 | 1 |
| XU11 THRU XU13 | Socket, 28–Pin | 417–2804 | 3 |
| XU14 THRU XU16 | Socket, 8–Pin DIP | 417–0804 | 3 |
| XU17 | Socket, 14–Pin DIP | 417–1404 | 1 |
| XU18 | Socket, 16–Pin DIP | 417–1604 | 1 |
| XU19 | Socket, 14–Pin DIP | 417–1404 | 1 |
| XU20,XU21 | Socket, 16–Pin DIP | 417–1604 | 2 |
| XU22 | Socket, 24–Pin DIP | 417–2404 | 1 |
| XU23 | Socket, 14–Pin DIP | 417–1404 | 1 |
| XU24,XU25 | Socket, 16–Pin DIP | 417–1604 | 2 |
| XU26 THRU XU31 | Socket, 14–Pin DIP | 417–1404 | 6 |
| XU32 | Socket, 20–Pin DIP | 417–2004 | 1 |
| XU33 | Socket, 14–Pin DIP | 417–1404 | 1 |
| XU34,XU35 | Socket, 20–Pin DIP | 417–2004 | 2 |
| Y2 | Oscillator, Integrated Circuit, CO–238T, Turntable 10 MHz, 14–Pin DIP | 390–0002 | 1 |
| —— | Resistor, 2.2 k Ohm ±5%, 1/4W | 100–2243 | 1 |
| —— | Blank Circuit Board | 519–0024 | 1 |

## TABLE 6–10. 64K MEMORY CIRCUIT BOARD ASSEMBLY – 919–0110
(Sheet 1 of 2)

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| C1 THRU C3 | Capacitor, Ceramic, 0.01 uF +20%, 25V | 000–1044 | 3 |
| C4 | Capacitor, Tantalum, 1 uF ±10%, 35V | 064–1063 | 1 |
| C8 THRU C28 | Capacitor, Ceramic, 0.01 uF ±20%, 25V | 000–1044 | 21 |
| J1 THRU J24 | Jumper, Programmable | 340–0004 | 24 |
| S2 | Switch, 8–SPST, 16–Pin DIP | 340–0003 | 1 |
| U1 | Resistor Network, 410A472, 4.7 k Ohm, Single–In–Line Package, 10–Pin | 226–4740 | 1 |
| U2 | Integrated Circuit, SN74LS138N, 1 of 8 Decoder, 16–Pin DIP | 228–2138 | 1 |
| U3 | Resistor Network, 410A472, 4.7 k Ohm, Single–In–Line Package, 10–Pin | 226–4740 | 1 |
| U4 | Integrated Circuit, SN74LS138N, 1 of 8 Decoder, 16–Pin DIP | 228–2138 | 1 |
| U5 | Resistor Network, 410A472, 4.7 k Ohm, Single–In–Line Package, 10–Pin | 226–4740 | 1 |
| U6,U7 | Integrated Circuit, SN74LS138N, 1 of 8 Decoder, 16–Pin DIP | 228–2138 | 2 |
| U10 | Resistor Network, 783–1–R4.7K, 4.7 k Ohm, Single–In–Line Package, 6–Pin | 226–4741 | 1 |
| U14 THRU U17 | Integrated Circuit, SN74LS244N, Octal Tri–State Bus Driver, 20–Pin DIP | 228–2244 | 4 |

## TABLE 6–10. 64K MEMORY CIRCUIT BOARD ASSEMBLY – 919–0110
(Sheet 2 of 2)

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| U19 | Resistor Network, 410A472, 4.7 k Ohm, Single–In–Line Package, 10–Pin | 226–4740 | 1 |
| U20 | Integrated Circuit, SN74LS20N, Schottky Dual 4–Input NAND Gate, 14–Pin DIP | 228–2420 | 1 |
| U21 | Integrated Circuit, SN74LS04N, Low–Power Schottky Hex Inverter, 14–Pin DIP | 228–2404 | 1 |
| X1 | Integrated Circuit, HM6116P–4, 2K X 8 RAM, CMOS, 24–Pin DIP | 229–6116 | 1 |
| X2 | Integrated Circuit, MK48Z02B–25, EEPROM 2K X 8, CMOS, 24–Pin DIP | 220–2816 | 1 |
| —— | Socket, 24–Pin DIP | 417–2404 | 32 |
| —— | Header, 3–Pin | 417–0003 | 24 |
| —— | Socket, 14–Pin DIP | 417–1404 | 2 |
| —— | Socket, 16–Pin DIP | 417–1604 | 4 |
| —— | Socket, 20–Pin DIP | 417–2004 | 4 |
| —— | Blank Circuit Board | 518–0017 | 1 |

## TABLE 6–11. CABLE ASSEMBLY, FM MICROPROCESSOR – 949–0191–001

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| J2 | Connector, 6–Pin | 418–0006 | 1 |
| J4 | Connector, 16–Pin DIP | 417–1605 | 1 |
| J5 | Connector, 24–Pin | 417–2403 | 1 |
| J6 | Connector, Circuit Board Edge, 16–Pin | 417–0073 | 1 |
| J6 | Connector, Plug, 25–Pin | 417–0251 | 1 |
| J7 | Connector, 15–Pin, Male | 418–2379 | 1 |
| P3, P3<br>P5, P5 | Connector, Circuit board Edge, 26–Pin | 417–2615 | 4 |
| P1,P4 | Connector, 6–Pin | 418–0670 | 2 |
| P7 | Connector, Housing, 15–Pin | 417–2379 | 1 |
| P8 | Connector, 2–Pin | 417–0499 | 1 |
| —— | Switch, Toggle, 3PDT, 5A @ 120V ac or 28V dc, 2A @ 250V ac (MVDS Power Switch) | 340–0062 | 1 |
| S1 | Header, Programmable, 8–Pin DIP | 340–0006 | 1 |
| W6, W6<br>W10, W10 | Plug, BNC, Dual Crimp | 418–0034 | 4 |
| —— | Pins Connector 641294–1 | 417–0053 | 20 |
| —— | Pins Connector, MOD–IV | 417–8766 | 2 |
| —— | Pins, Connector | 417–0036 | 20 |
| —— | Connector, Circuit Board Edge, 50–Pin | 417–0072 | 2 |
| —— | Connector, DIN, 5–Pin | 417–0132 | 1 |
| —— | Pins, Connector | 417–0142 | 4 |

## TABLE 6–12. ASSEMBLY, EXHAUST AIR TEMPERATURE SENSOR – 919–0082
(Sheet 1 of 2)

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| C1,C2 | Capacitor, Mica, 390 pF ±5%, 100V | 042–3922 | 2 |
| C3,C4 | Capacitor, Ceramic, 0.001 uF ±10%, 1 kV | 002–1034 | 2 |
| J1 | Socket, 4–Pin | 418–0255 | 1 |
| R1 | Resistor, 10 k Ohm ±5%, 1/4W | 100–1053 | 1 |
| R2 | Resistor, 2.2 k Ohm ±5%, 1/4W | 100–2243 | 1 |

## TABLE 6–12. ASSEMBLY, EXHAUST AIR TEMPERATURE SENSOR – 919–0082
(Sheet 2 of 2)

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| U1 | Integrated Circuit, LM35DZ, Celsius Temperature Sensor, TO–92 Case | 220–0035 | 1 |
| —— | Blank Circuit Board | 519–0082 | 1 |

## TABLE 6–13. SOFTWARE KIT, MVDS VDM 60 Hz – 979–0113

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| U7,U28 | Integrated Circuit, AM2764A–2DC, EPROM, 8K X 8, Programmed with Video Display Module Control and Character Generator | 220–2764 | 2 |

## TABLE 6–14. SOFTWARE KIT, MVDS VDM 50 Hz – 979–0112

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| U7,U28 | Integrated Circuit, AM2764A–2DC, EPROM, 8K X 8, Programmed with Video Display Module Control and Character Generator | 220–2764 | 2 |

## TABLE 6–15. SOFTWARE KIT, FM–30B – 979–0091–014

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| X3 THRU X24,X29,X30 | Integrated Circuit, MM2716Q, EPROM, NMOS, 24–Pin DIP with MVDS Software for FM–30B Transmitter | 229–2716 | 24 |

## TABLE 6–16. SOFTWARE KIT, FM–3.5B – 979–0091–024

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| X3 THRU X24,X29,X30 | Integrated Circuit, MM2716Q, EPROM, NMOS, 24–Pin DIP with MVDS Software for FM–3.5B Transmitter | 229–2716 | 24 |

## TABLE 6–17. SOFTWARE KIT, FM–5B – 979–0091–034

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| X3 THRU X24,X29,X30 | Integrated Circuit, MM2716Q, EPROM, NMOS, 24–Pin DIP with MVDS Software for FM–5B Transmitter | 229–2716 | 24 |

## TABLE 6–18. SOFTWARE KIT, FM–10B – 979–0091–054

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| X3 THRU X24,X29,X30 | Integrated Circuit, MM2716Q, EPROM, NMOS, 24–Pin DIP with MVDS Software for FM–10B Transmitter | 229–2716 | 24 |

## TABLE 6–19. SOFTWARE KIT, FM–35B – 979–0091–064

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| X3 THRU X24,X29,X30 | Integrated Circuit, MM2716Q, EPROM, NMOS, 24–Pin DIP with MVDS Software for FM–35B Transmitter | 229–2716 | 24 |

## TABLE 6–20. SOFTWARE KIT, FM–20B – 979–0091–074

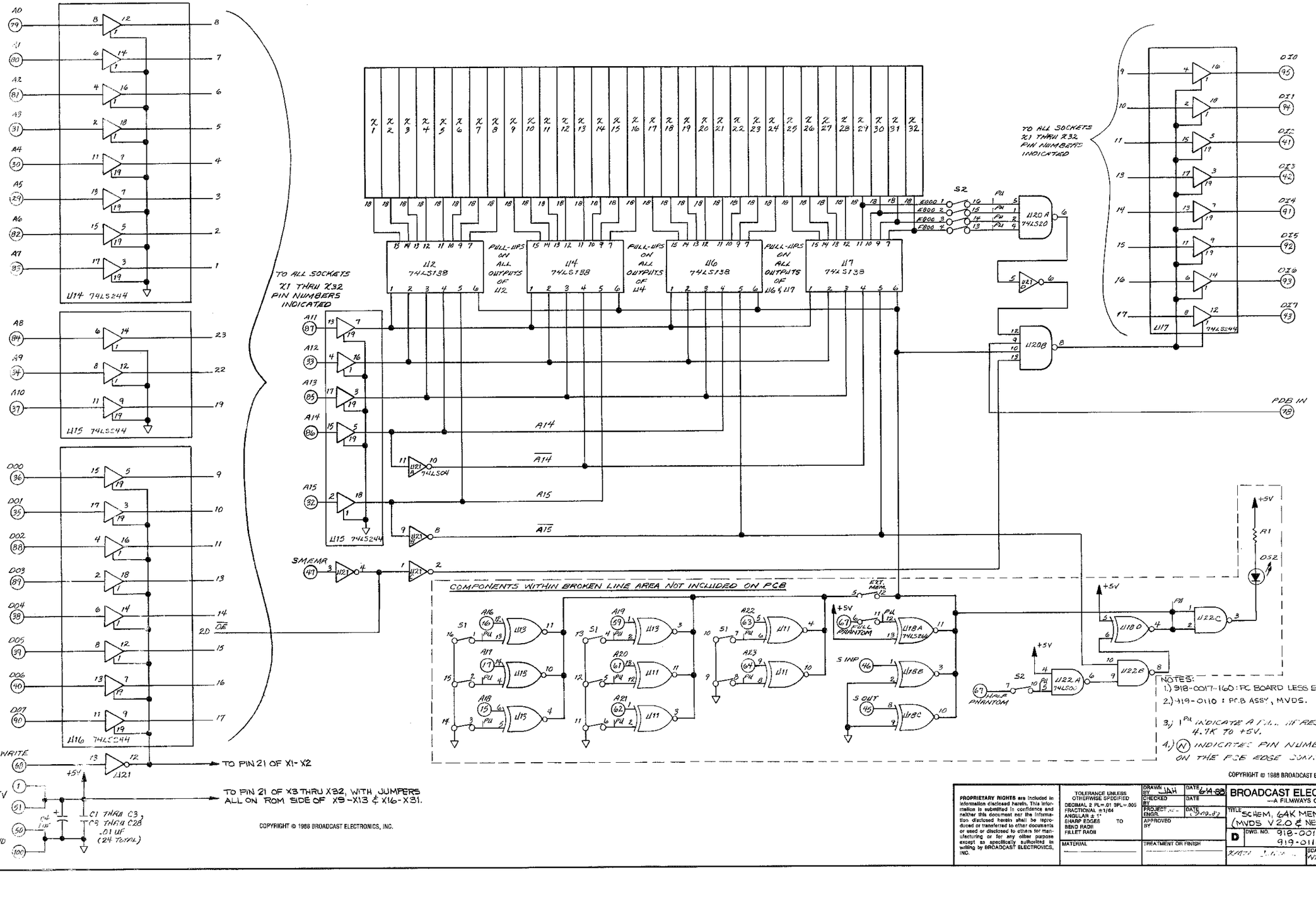
| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| X3 THRU X24,X29,X30 | Integrated Circuit, MM2716Q, EPROM, NMOS, 24–Pin DIP with MVDS Software for FM–20B Transmitter | 229–2716 | 24 |

# SECTION VII
# MVDS DRAWINGS

## 7–1. INTRODUCTION.

7–2. This section provides assembly drawings, schematic diagrams, and cable diagrams as indexed below for the Broadcast Electronics MVDS.

| FIGURE | TITLE | NUMBER |
|---|---|---|
| 7–1 | SCHEMATIC DIAGRAM, 64K MEMORY CIRCUIT BOARD | SD919–0110 |
| 7–2 | ASSEMBLY DIAGRAM, 64K MEMORY CIRCUIT BOARD | AC919–0110 |
| 7–3 | SCHEMATIC DIAGRAM, ANALOG/DIGITAL CIRCUIT BOARD | SD919–0058 |
| 7–4 | ASSEMBLY DIAGRAM, ANALOG/DIGITAL CIRCUIT BOARD | AD919–0058 |
| 7–5 | COMPONENT LOCATOR, ANALOG/DIGITAL CIRCUIT BOARD | 597–0036–21 |
| 7–6 | SCHEMATIC DIAGRAM, INPUT/OUTPUT CIRCUIT BOARD | SD919–0024 |
| 7–7 | ASSEMBLY DIAGRAM, INPUT/OUTPUT CIRCUIT BOARD | AD919–0024 |
| 7–8 | COMPONENT LOCATOR, INPUT/OUTPUT CIRCUIT BOARD | 597–0036–22 |
| 7–9 | SCHEMATIC DIAGRAM, CPU CIRCUIT BOARD | SD919–0059 |
| 7–10 | ASSEMBLY DIAGRAM, CPU CIRCUIT BOARD | AD919–0059 |
| 7–11 | SCHEMATIC DIAGRAM, VDM CIRCUIT BOARD | SD919–0036 |
| 7–12 | ASSEMBLY DIAGRAM, VDM CIRCUIT BOARD | AD919–0036 |
| 7–13 | SCHEMATIC DIAGRAM, EMI FILTER CIRCUIT BOARD | SC919–0057 |
| 7–14 | ASSEMBLY DIAGRAM, EMI FILTER CIRCUIT BOARD | AC919–0057 |
| 7–15 | SCHEMATIC DIAGRAM, EXHAUST AIR TEMPERATURE SENSOR CIRCUIT BOARD | SB919–0082 |
| 7–16 | ASSEMBLY DIAGRAM, EXHAUST AIR TEMPERATURE SENSOR CIRCUIT BOARD | AB919–0082 |
| 7–17 | WIRING DIAGRAM, MVDS POWER SUPPLY | SD959–0298–001 |
| 7–18 | SCHEMATIC DIAGRAM, POWER SUPPLY | 597–0036–23 |
| 7–19 | ASSEMBLY DIAGRAM, MOTHERBOARD | AC919–0023 |
| 7–20 | ASSEMBLY DIAGRAM, CONTROLLER CABINET RIBBON CABLES | 597–0036–24 |
| 7–21 | CABLE DIAGRAM, PARALLEL LOG PRINTER | AC949–0110 |
| 7–22 | CABLE DIAGRAM, SCA GENERATOR | AB949–0111 |
| 7–23 | CABLE DIAGRAM, SCA GENERATOR WITH A MODEM | AC949–0112 |
| 7–24 | CABLE DIAGRAM, SERIAL LOG PRINTER | AB949–0113 |
| 7–25 | CABLE DIAGRAM, MODEM | AB949–0114 |
| 7–26 | CABLE DIAGRAM, KEYBOARD TO CONTROLLER | AB949–0105 |




COPYRIGHT © 1988 BROADCAST ELECTRONICS, INC.

PROPRIETARY RIGHTS are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE UNLESS OTHERWISE SPECIFIED
DECIMAL 2 PL=.01 3PL=.005
FRACTIONAL ±1/64
ANGULAR ± 1°
SHARP EDGES TO BEND RADII FILLET RADII

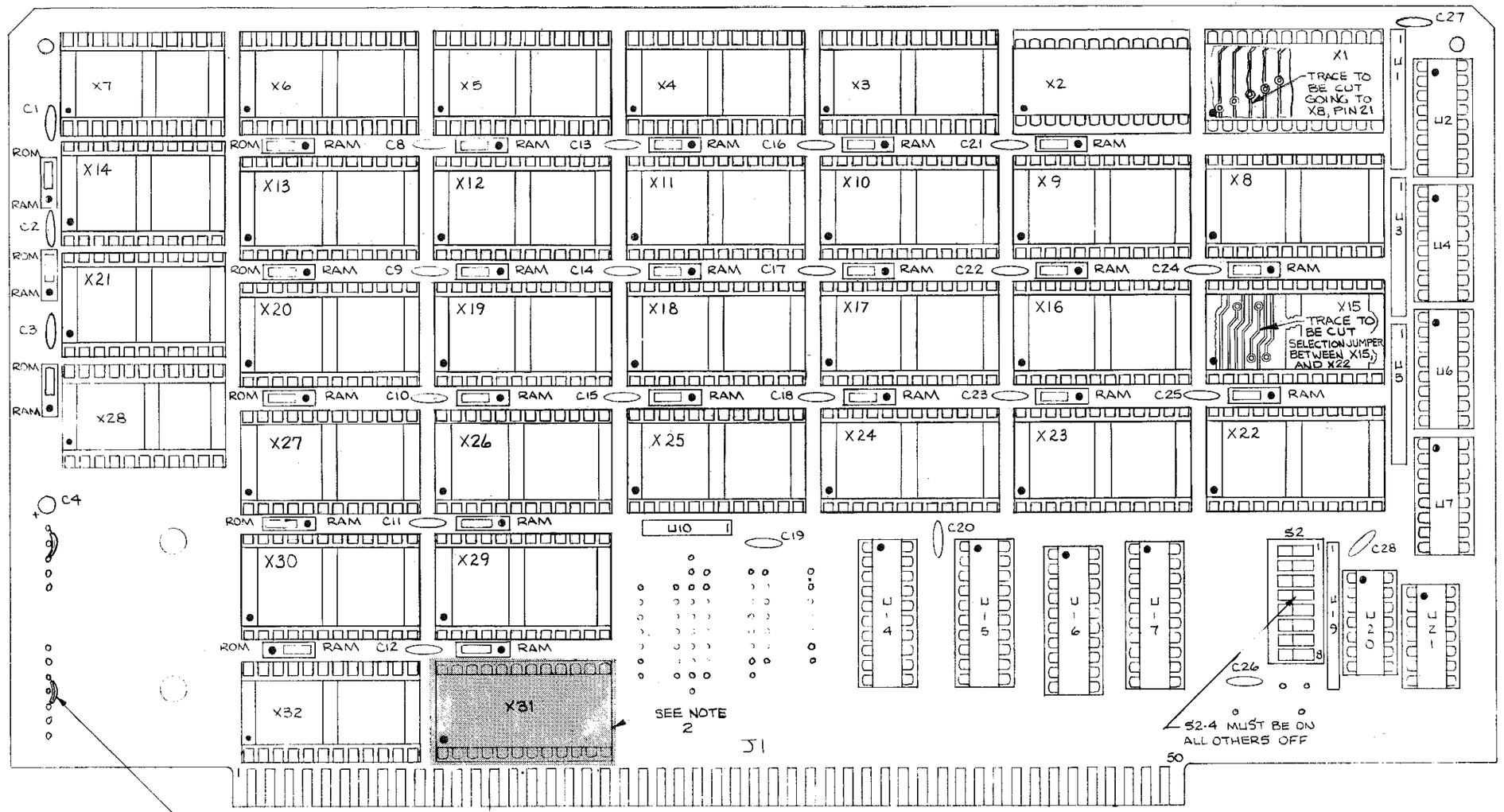
DRAWN BY JAH DATE 6-14-88
CHECKED BY DATE
PROJECT ENGR. DATE 9-19-88
APPROVED BY
MATERIAL
TREATMENT OR FINISH

BROADCAST ELECTRONICS INC.
—A FILMWAYS COMPANY—

TITLE SCHEM, 64K MEMORY BOARD (MVDS V2.0 & NEWER SOFTWARE)

D DWG. NO. 918-0017-160 REV. D
919-0110

SCALE WT: SHEET 1 OF 1




SEE SCHEMATIC *SD919-0110

NOTE:

1. 2716 EPROM'S (X29, X30) ARE TO BE PROGRAMMED FOR FM-20B.
2. SOCKET X31, INDICATED BY SHADED AREA, TO BE FILLED WITH PROGRAMMED EPROM ONLY ON BOARDS PROGRAMMED FOR USE IN FM-30A OR FM-35A. THIS EPROM WILL BE ADDED BY TRANSMITTER TEST, IF REQUIRED.

PROPRIETARY RIGHTS are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1

DWN. BY JAH 9-9-93
CHKD
ME
PROJ. ENGR. KLC 09-09-93
MFG.

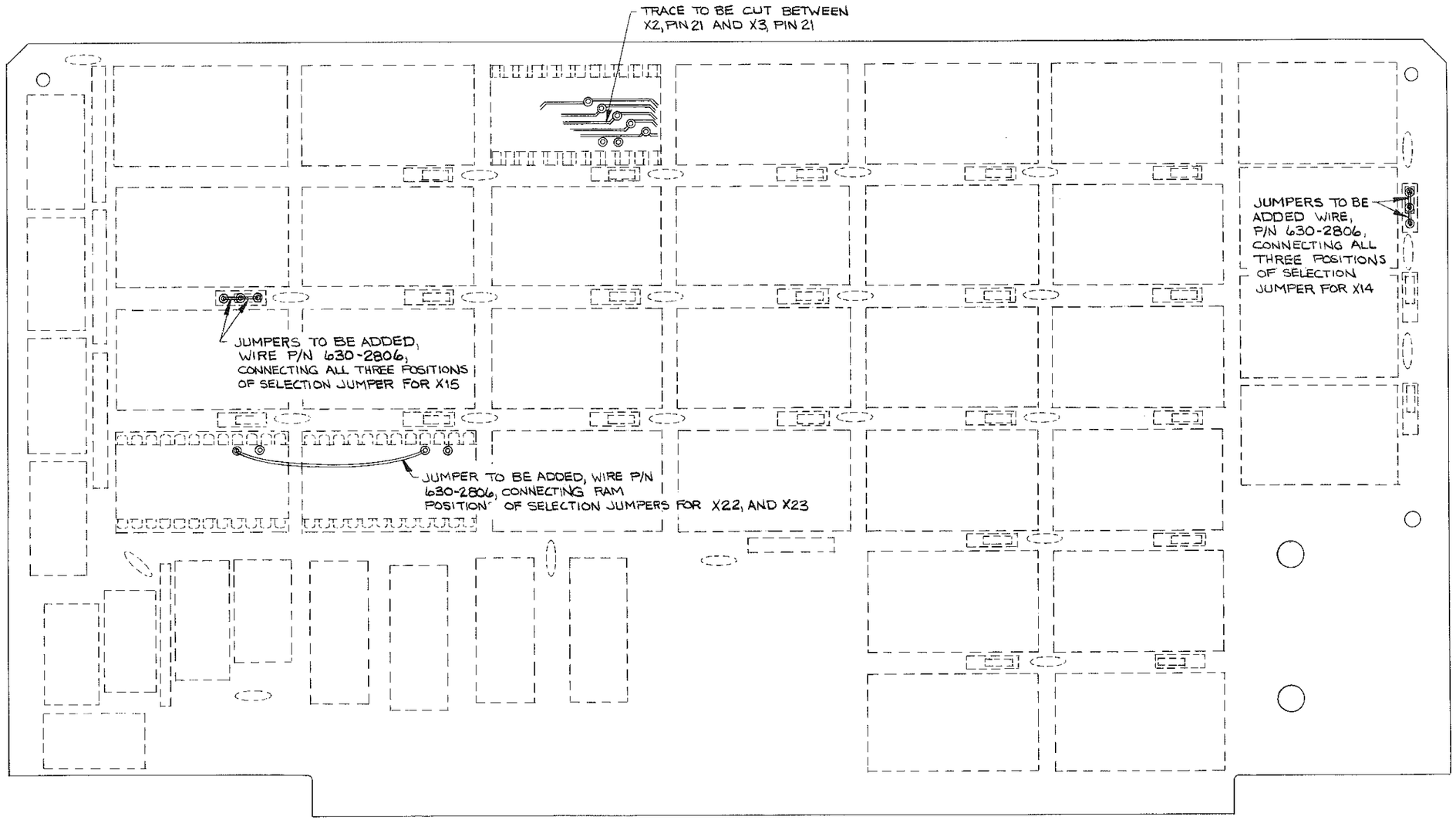
MATERIAL SEE B/M 919-0110
FINISH
NEXT ASSY.

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O. BOX 3606 QUINCY, IL 62305 217 224-9600
TELEX 250142 CABLE BROADCAST

TITLE PCB ASSEMBLY, 64K MEMORY BOARD

TYPE A | SIZE C | DWG. NO. 919-0110 | REV D

MODEL XMTR CONTROLLER | SCALE 2/1 | SHEET 1 OF 2




REAR VIEW OF 919-0110

**PROPRIETARY RIGHTS** are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY JAH 9-9-88
CHKD
ME
PROJ. ENGR. RLC 09-09-88
MFG.

MATERIAL SEE B/M 919-0110
FINISH SEE DWG RA592-0000
NEXT ASSY.

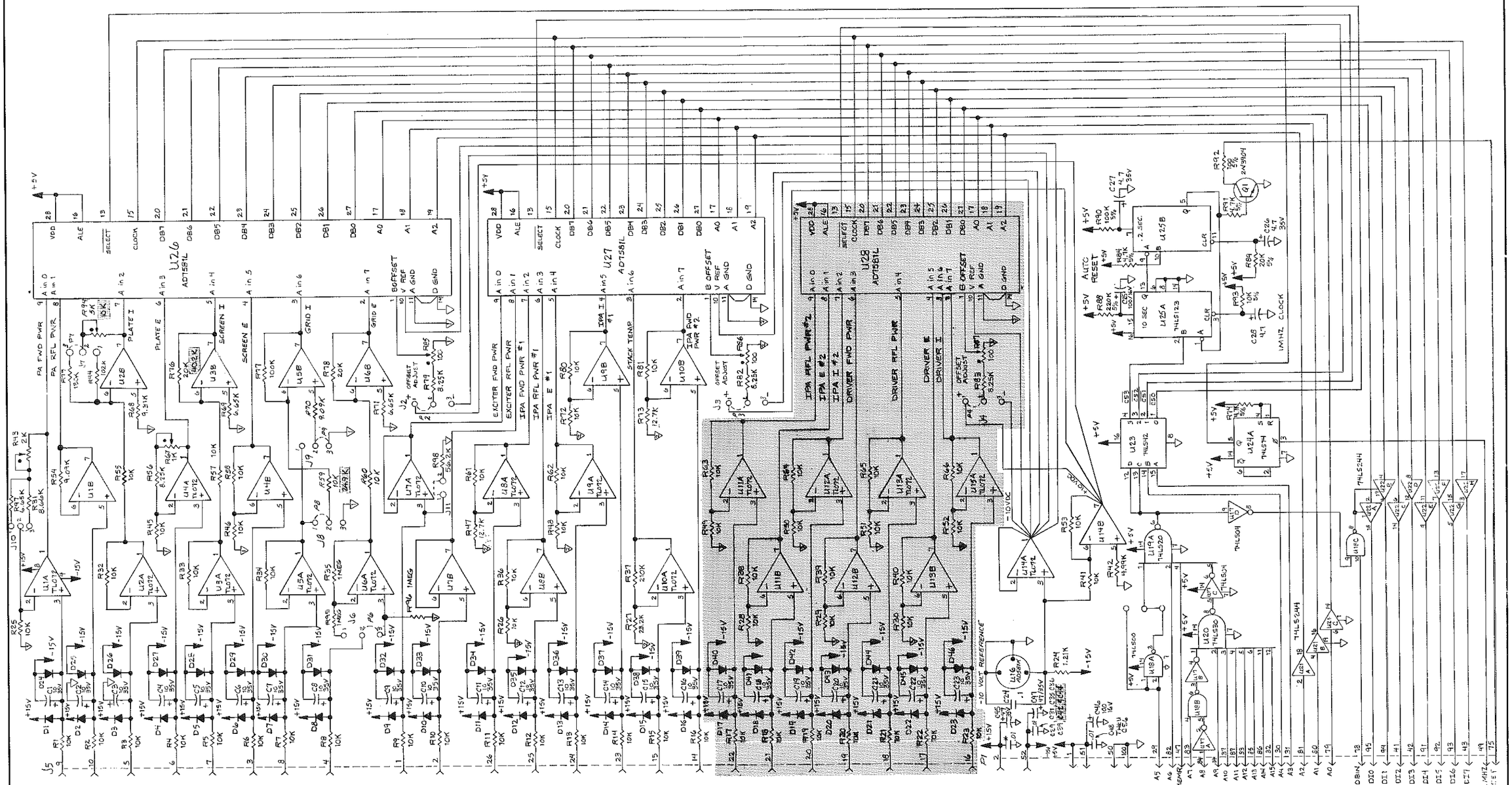
BE® BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O.BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE PCB ASSEMBLY, 64K MEMORY BOARD

| TYPE | SIZE | DWG. NO. | REV |
|---|---|---|---|
| A | C | 919-0110 | D |

MODEL XMTR CONTROLLER | SCALE 2/1 | SHEET 2 OF 2

COPYRIGHT © 1988 BROADCAST ELECTRONICS, INC.




| Jumper Select Table | | | | |
|---|---|---|---|---|
| Model | J6 | J7 | J8 | J9 |
| FM1A/B FM1.5N/B | 1-2 | 1-2 | 2-3 | 1-2 |
| FM3.5A FM5A FM5A5 FM10A | 2-3 | 2-3 | 1-2 | 2-3 |
| FM3.5B FM5B FM5B5 FM10B | 2-3 | 1-2 | 1-2 | 2-3 |
| FM20A/B FM30A/B FM35A/B | 2-3 | 1-2 | 1-2 | 2-3 |

NOTES:
1. ALL RESISTORS IN OHMS, 1/4 W 1%; ALL DIODES IN4148; CAPACITORS IN MICROFARADS; U.O.S.
2. * DENOTES C30, C32, C33, C34, C37, C38, C40, C41, C43.
3. COMPONENTS LAST USED: C56, D46, J11, Q1, R98 & U28.
4. COMPONENTS NOT USED: U15B, U17-E&F, U18D, U19B, U21-D&E, F, G&H, U24B
5. J11 TO BE IN POSITION 1-2 ONLY WHEN FX-50 FORWARD POWER SOFTWARE TABLE IS PRESENT. ALL "B" SERIES XMTRS HAVE FX-50 SOFTWARE TABLE. ALL "A" SERIES XMTRS SHIPPED WITHOUT FX-50 SOFTWARE TABLE.
6. COMPONENTS WITHIN SHADED AREA APPLY TO 20, 30, 35kw 'A' & 'B' TRANSMITTERS ONLY.
7. J10 TO BE IN POSITION 1-2 FOR SOFTWARE VERSIONS 2.0 & HIGHER; J10 TO BE IN POSITION 2-3 FOR SOFTWARE VERSION 1.0-1.4.

COPYRIGHT © 1985 BROADCAST ELECTRONICS, INC.

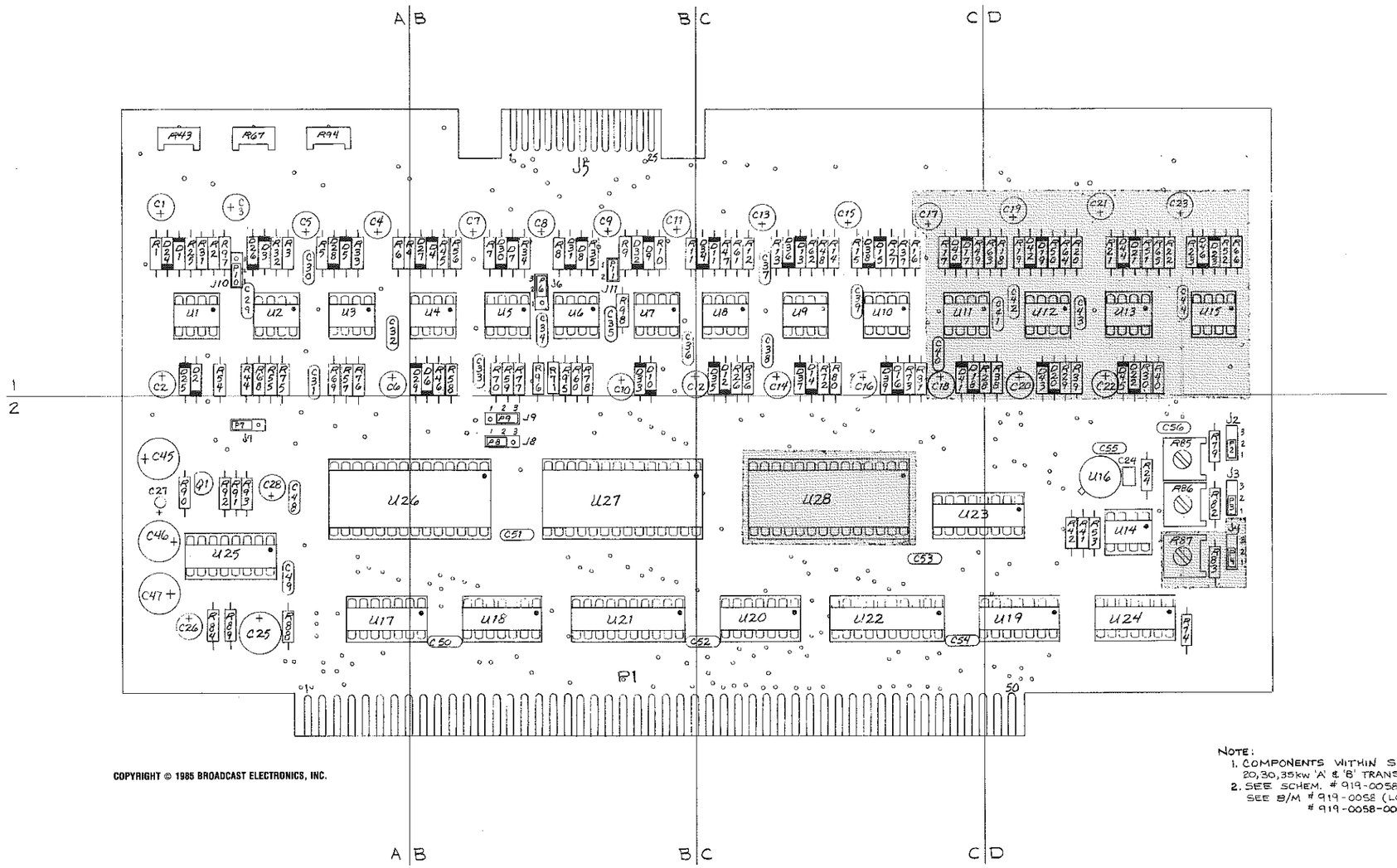
PROPRIETARY RIGHTS are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE (DECIMAL) U.O.S. .x ± .030 .xxx ± .005 .xx ± .015 ANGLES ± 1°

DWN. BY MJ OFF 9-12-85
CHKD JH 1-19-86
ME
PROJ. ENGR. 1-17-86
MFG.
MATERIAL
FINISH
NEXT ASSY.

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O. BOX 3606, QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE SCHEMATIC ANALOG/DIGITAL PCB
TYPE 3 SIZE D DWG. NO. 919-0058, 919-0058-001 REV R
MODEL FM - XMTRS SCALE NTS SHEET 1 OF 1




COPYRIGHT © 1985 BROADCAST ELECTRONICS, INC.

NOTE:
1. COMPONENTS WITHIN SHADED AREA APPLY TO 20,30,35kw 'A' & 'B' TRANSMITTERS ONLY.
2. SEE SCHEM. # 919-0058 & 919-0058-001
   SEE B/M # 919-0058 (LOW POWER XMTRS)
   # 919-0058-001 (FM-30 XMTR)

COPYRIGHT © 1985 BROADCAST ELECTRONICS, INC.

PROPRIETARY RIGHTS are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY MJ OAK 9-21-89
CHKD MM 1-19-84
ME
PROJ. ENGR. [illegible]
MFG.

MATERIAL
FINISH
NEXT ASSY.

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O.BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE PCB ASSEMBLY
# ANALOG/DIGITAL PCB

TYPE A | SIZE D | DWG. NO. 919-0058 & 919-0058-001 | REV P

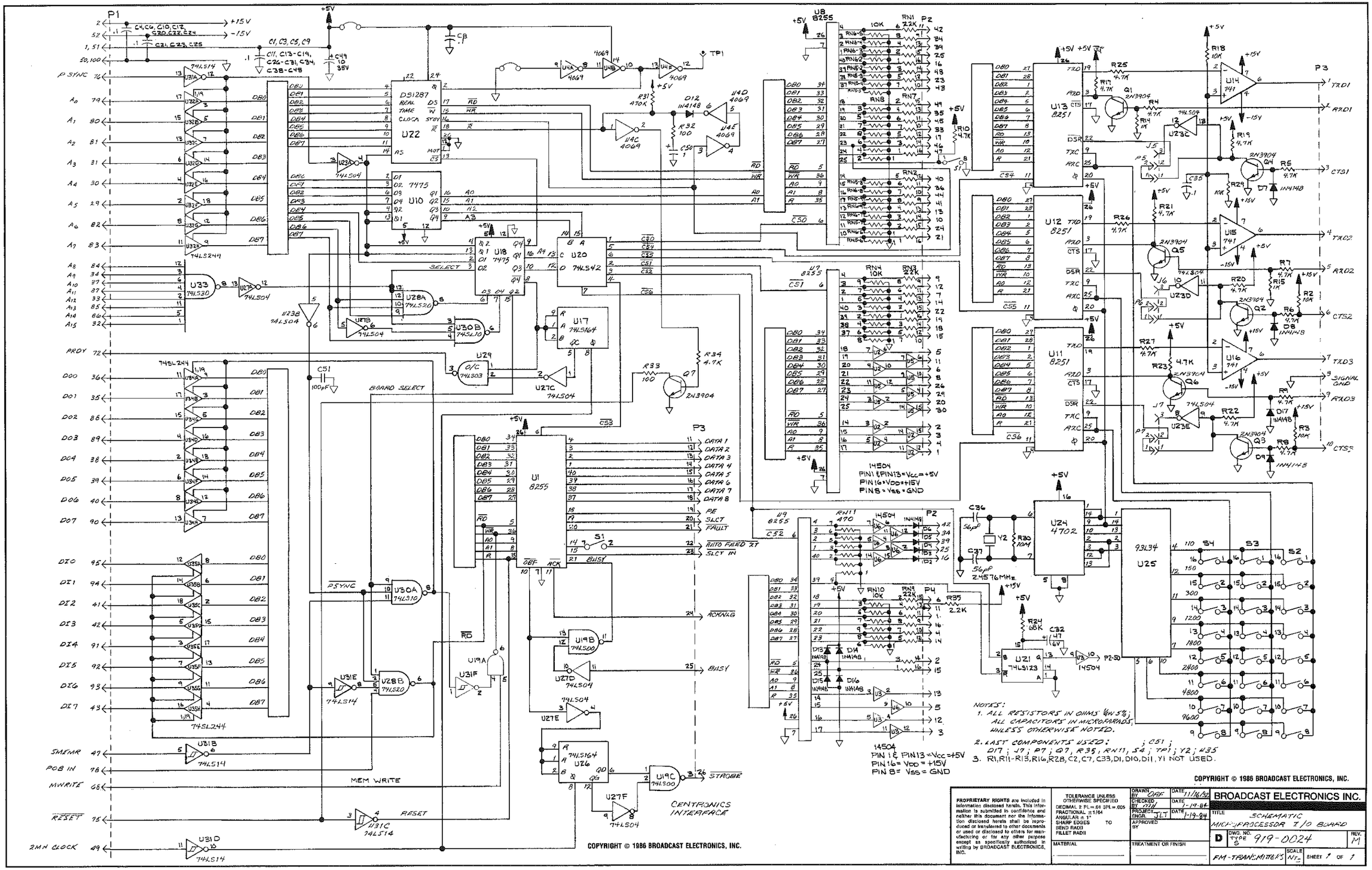
MODEL FM-XMTRS | SCALE 2/1 | SHEET 1 OF 1

| REF | ZONE | REF | ZONE | REF | ZONE | REF | ZONE | REF | ZONE |
|---|---|---|---|---|---|---|---|---|---|
| C1 | A1 | D1 | A1 | P3 | D2 | R48 | C1 | U6 | B1 |
| C2 | A1 | D2 | A1 | P4 | D2 | R49 | C1 | U7 | B1 |
| C3 | A1 | D3 | A1 | P6 | B1 | R50 | D1 | U8 | C1 |
| C4 | A1 | D4 | B1 | P7 | A2 | R51 | D1 | U9 | C1 |
| C5 | A1 | D5 | A1 | P8 | B2 | R52 | D1 | U10 | C1 |
| C6 | A1 | D6 | B1 | P9 | B2 | R53 | D2 | U11 | C1 |
| C7 | B1 | D7 | B1 | P10 | A1 | R54 | A1 | U12 | D1 |
| C8 | B1 | D8 | B1 | P11 | B1 | R55 | A1 | U13 | D1 |
| C9 | B1 | D9 | B1 | Q1 | A2 | R56 | B1 | U14 | D2 |
| C10 | B1 | D10 | B1 | R1 | A1 | R57 | A1 | U15 | D1 |
| C11 | B1 | D11 | C1 | R2 | A1 | R58 | B1 | U16 | D2 |
| C12 | B1-C1 | D12 | C1 | R3 | A1 | R59 | B1 | U17 | A2 |
| C13 | C1 | D13 | C1 | R4 | A1-B1 | R60 | B1 | U18 | B2 |
| C14 | C1 | D14 | C1 | R5 | A1 | R61 | C1 | U19 | D2 |
| C15 | C1 | D15 | C1 | R6 | A1 | R62 | C1 | U20 | C2 |
| C16 | C1 | D16 | C1 | R7 | B1 | R63 | D1 | U21 | B2 |
| C17 | C1 | D17 | C1 | R8 | B1 | R64 | D1 | U22 | C2 |
| C18 | C1 | D18 | C1 | R9 | B1 | R65 | D1 | U23 | C2-D2 |
| C19 | D1 | D19 | D1 | R10 | B1 | R66 | D1 | U24 | D2 |
| C20 | D1 | D20 | D1 | R11 | B1 | R67 | A1 | U25 | A2 |
| C21 | D1 | D21 | D1 | R12 | C1 | R68 | A1 | U26 | A2-B2 |
| C22 | D1 | D22 | D1 | R13 | C1 | R69 | A1 | U27 | B2 |
| C23 | D1 | D23 | D1 | R14 | C1 | R70 | B1 | U28 | C2 |
| C24 | D2 | D24 | A1 | R15 | C1 | R71 | B1 | | |
| C25 | A2 | D25 | A1 | R16 | C1 | R72 | C1 | | |
| C26 | A2 | D26 | A1 | R17 | C1 | R73 | C1 | | |
| C27 | A2 | D27 | B1 | R18 | D1 | R74 | D2 | | |
| C28 | A2 | D28 | A1 | R19 | D1 | R75 | A1 | | |
| C29 | A1 | D29 | B1 | R20 | D1 | R76 | A1 | | |
| C30 | A1 | D30 | B1 | R21 | D1 | R77 | B1 | | |
| C31 | A1 | D31 | B1 | R22 | D1 | R78 | B1 | | |
| C32 | A1 | D32 | B1 | R23 | D1 | R79 | D2 | | |
| C33 | B1 | D33 | B1 | R24 | D2 | R80 | C1 | | |
| C34 | B1 | D34 | C1 | R25 | A1 | R81 | C1 | | |
| C35 | B1 | D35 | C1 | R26 | C1 | R82 | D2 | | |
| C36 | B1 | D36 | C1 | R27 | C1 | R83 | D2 | | |
| C37 | C1 | D37 | C1 | R28 | C1-D1 | R84 | A2 | | |
| C38 | C1 | D38 | C1 | R29 | D1 | R85 | D2 | | |
| C39 | C1 | D39 | C1 | R30 | D1 | R86 | D2 | | |
| C40 | C1 | D40 | C1 | R31 | A1 | R87 | D2 | | |
| C41 | D1 | D41 | C1 | R32 | A1 | R88 | A2 | | |
| C42 | D1 | D42 | D1 | R33 | A1 | R89 | A2 | | |
| C43 | D1 | D43 | D1 | R34 | B1 | R90 | A2 | | |
| C44 | D1 | D44 | D1 | R35 | B1 | R91 | A2 | | |
| C45 | A2 | D45 | D1 | R36 | C1 | R92 | A2 | | |
| C46 | A2 | D46 | D1 | R37 | C1 | R93 | A2 | | |
| C47 | A2 | J2 | D2 | R38 | D1 | R94 | A1 | | |
| C48 | A2 | J3 | D2 | R39 | D1 | R95 | B1 | | |
| C49 | A2 | J4 | D2 | R40 | D1 | R96 | B1 | | |
| C50 | B2 | J6 | B1 | R41 | D2 | R97 | A1 | | |
| C51 | B2 | J7 | A2 | R42 | D2 | R98 | B1 | | |
| C52 | B2 | J8 | B2 | R43 | A1 | U1 | A1 | | |
| C53 | C2 | J9 | B2 | R44 | A1 | U2 | A1 | | |
| C54 | C2 | J10 | A1 | R45 | B1 | U3 | A1 | | |
| C55 | D2 | J11 | B1 | R46 | B1 | U4 | B1 | | |
| C56 | D2 | P2 | D2 | R47 | C1 | U5 | B1 | | |

COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597-0036-21

**FIGURE 7-5. COMPONENT LOCATOR, ANALO/DIGITAL CIRCUIT BOARD**

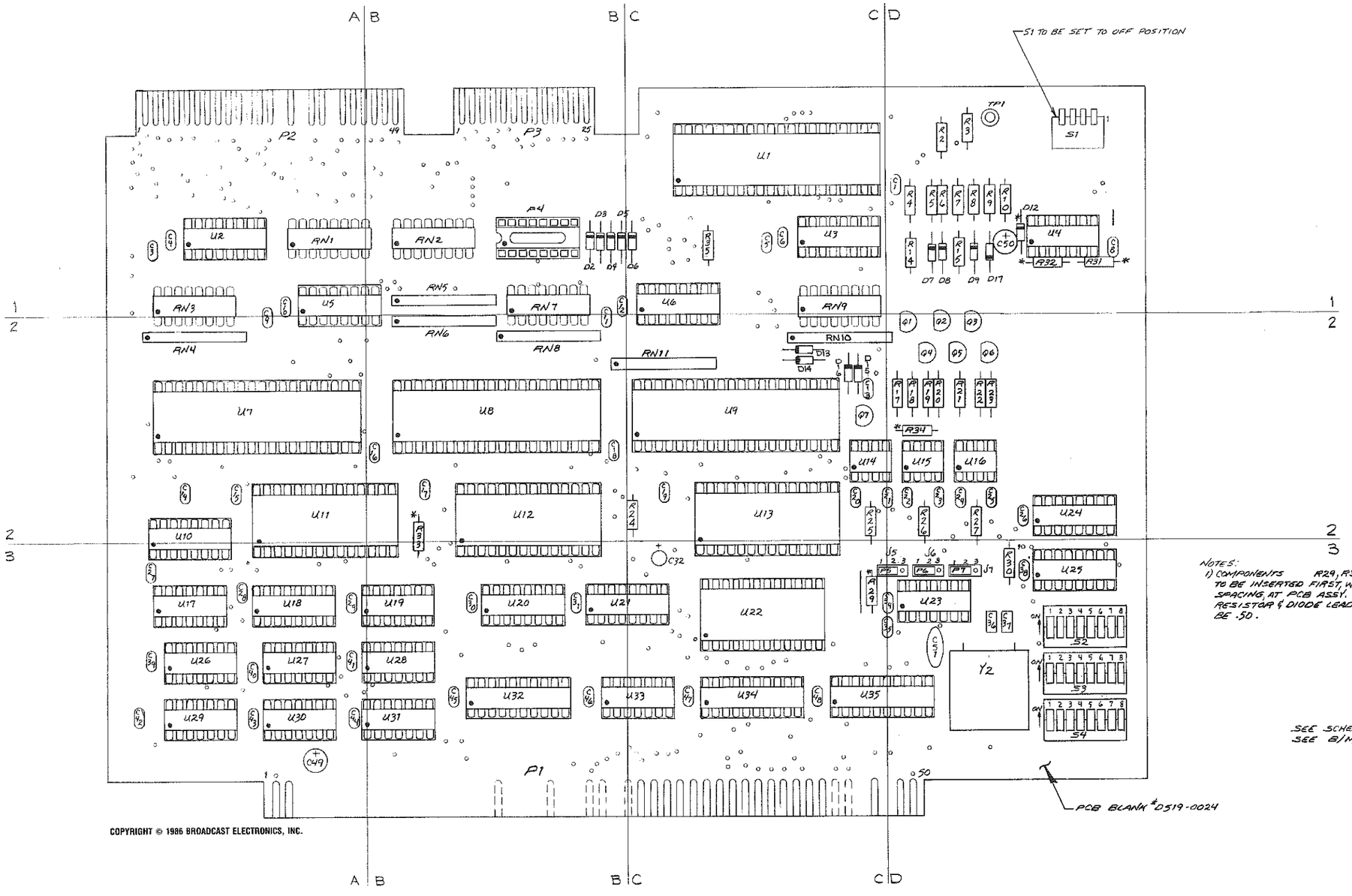



COPYRIGHT © 1986 BROADCAST ELECTRONICS, INC.

PROPRIETARY RIGHTS are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE UNLESS OTHERWISE SPECIFIED
DECIMAL 2 PL = .01 3PL = .005
FRACTIONAL ± 1/64
ANGULAR ± 1°
SHARP EDGES TO BEND RADII
FILLET RADII

| | | |
|---|---|---|
| DRAWN BY ORF | DATE 11/16/82 | BROADCAST ELECTRONICS INC. |
| CHECKED BY MH | DATE 1-19-84 | |
| PROJ ENGR. JLT | DATE 1-19-84 | TITLE SCHEMATIC MICROPROCESSOR I/O BOARD |
| APPROVED BY | | D DWG. NO. TYPE S 919-0024 REV. M |
| MATERIAL | TREATMENT OR FINISH | FM-TRANSMITTERS SCALE NTS SHEET 1 OF 1 |




NOTES:
1) COMPONENTS R29, R31-R34 & D12 TO BE INSERTED FIRST, WITH .40 LEAD SPACING, AT PCB ASSY. ALL OTHER RESISTOR & DIODE LEAD SPACINGS TO BE .50.

SEE SCHEMATIC #0919-0024
SEE B/M #919-0024

COPYRIGHT © 1986 BROADCAST ELECTRONICS, INC.

COPYRIGHT © 1986 BROADCAST ELECTRONICS, INC.

PROPRIETARY RIGHTS are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE UNLESS OTHERWISE SPECIFIED
DECIMAL 2 PL=.01 3PL=.005
FRACTIONAL ±1/64
ANGULAR ± 1°
SHARP EDGES TO BEND RADII
FILLET RADII

MATERIAL

TREATMENT OR FINISH

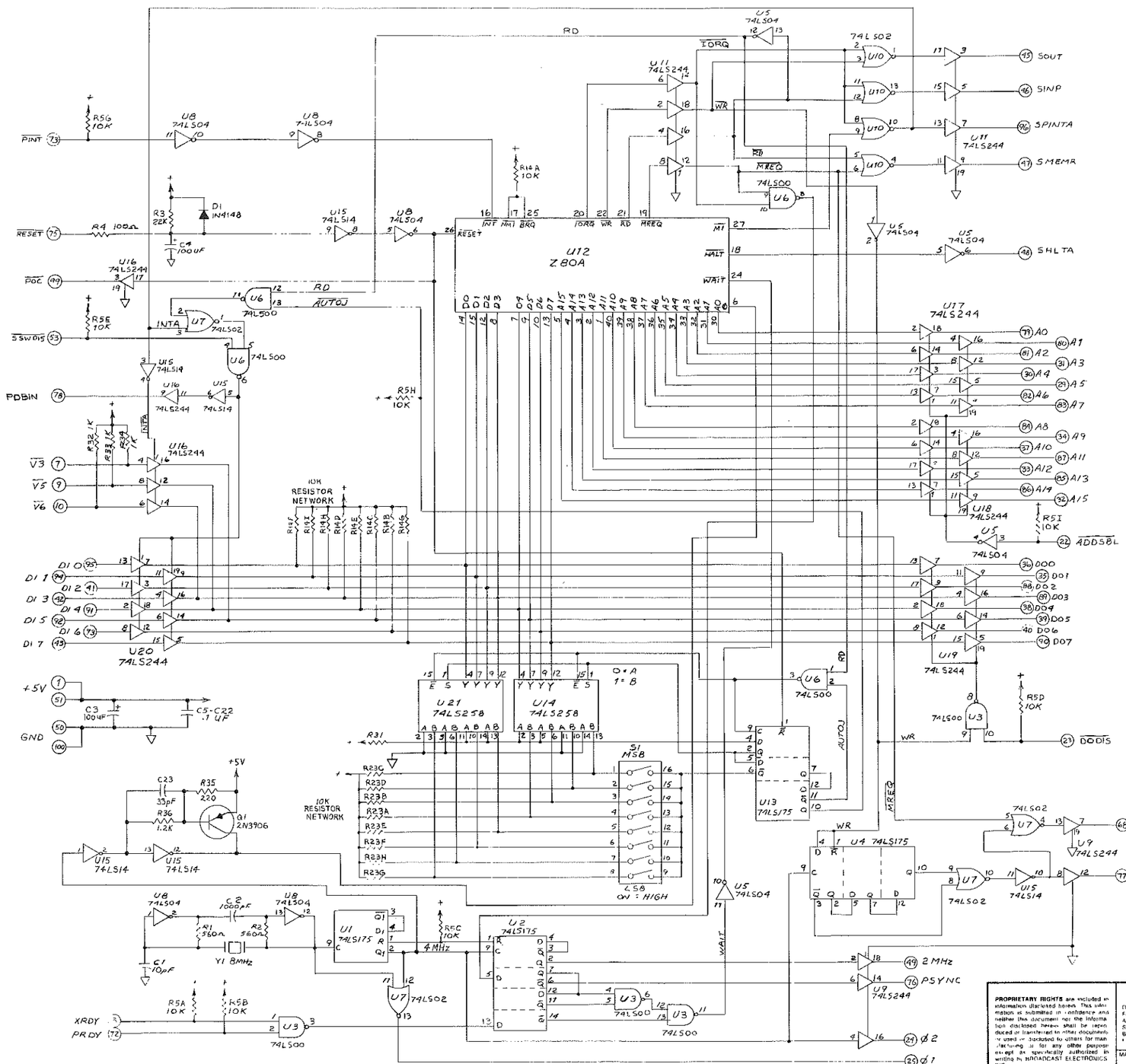
| | | |
|---|---|---|
| DRAWN BY ORF | DATE 6-6-83 | BROADCAST ELECTRONICS INC. |
| CHECKED BY AM | DATE 7-19-84 | |
| PROJECT ENGR. JTJ | DATE 7-19-84 | TITLE PCB ASSEMBLY MICROPROCESSOR I/O BOARD |
| APPROVED BY | | D DWG. NO. TYPE A 919-0024 REV. R |
| | | FM-TRANSMITTERS SCALE 2/1 SHEET 1 OF 1 |

| REF | ZONE | REF | ZONE | REF | ZONE | REF | ZONE |
|---|---|---|---|---|---|---|---|
| BAT1 | -- | D4 | B1 | R29 | C3 | U35 | C3-D3 |
| BAT2 | -- | D5 | B1 | R30 | D3 | Y1 | -- |
| BAT3 | -- | D6 | C1 | R31 | D1 | Y2 | D3 |
| C1 | D1 | D7 | D1 | R32 | D1 | | |
| C2 | -- | D8 | D1 | R33 | B2 | | |
| C3 | A1 | D9 | D1 | R34 | D2 | | |
| C4 | A1 | D10 | -- | R35 | C1 | | |
| C5 | C1 | D11 | -- | RN1 | A1 | | |
| C6 | C1 | D12 | D1 | RN2 | B1 | | |
| C7 | -- | D13 | C2 | RN3 | A1 | | |
| C8 | D1 | D14 | C2 | RN4 | A2 | | |
| C9 | A1-A2 | D15 | C2 | RN5 | B1 | | |
| C10 | A1 | D16 | C2 | RN6 | B2 | | |
| C11 | B1-B2 | D17 | D1 | RN7 | B1 | | |
| C12 | B1 | J5 | C3-D3 | RN8 | B2 | | |
| C13 | C2 | J6 | D3 | RN9 | C1 | | |
| C14 | A2 | J7 | D3 | RN10 | C1 | | |
| C15 | A2 | P4 | B1 | RN11 | C1 | | |
| C16 | B2 | P5 | C3-D3 | S1 | D1 | | |
| C17 | B2 | P6 | D3 | S2 | D3 | | |
| C18 | B2 | P7 | D3 | S3 | D3 | | |
| C19 | C2 | Q1 | D2 | S4 | D3 | | |
| C20 | C2 | Q2 | D2 | U1 | C1 | | |
| C21 | C2-D2 | Q3 | D2 | U2 | A1 | | |
| C22 | D2 | Q4 | D2 | U3 | C1 | | |
| C23 | D2 | Q5 | D2 | U4 | D1 | | |
| C24 | D2 | Q6 | D2 | U5 | A1 | | |
| C25 | D2 | Q7 | C2 | U6 | C1 | | |
| C26 | D2 | R1 | -- | U7 | A2 | | |
| C27 | A3 | R2 | D1 | U8 | B2 | | |
| C28 | A3 | R3 | D1 | U9 | C2 | | |
| C29 | A3 | R4 | D1 | U10 | A2-A3 | | |
| C30 | B3 | R5 | D1 | U11 | A2 | | |
| C31 | B3 | R6 | D1 | U12 | B2 | | |
| C32 | C3 | R7 | D1 | U13 | C2 | | |
| C33 | -- | R8 | D1 | U14 | C2 | | |
| C34 | C3-D3 | R9 | D1 | U15 | D2 | | |
| C35 | C3-D3 | R10 | D1 | U16 | D2 | | |
| C36 | D3 | R11 | -- | U17 | A3 | | |
| C37 | D3 | R12 | -- | U18 | A3 | | |
| C38 | D3 | R13 | -- | U19 | B3 | | |
| C39 | A3 | R14 | D1 | U20 | B3 | | |
| C40 | A3 | R15 | D1 | U21 | B3-C3 | | |
| C41 | A3 | R16 | D1 | U22 | C3 | | |
| C42 | A3 | R17 | D2 | U23 | D3 | | |
| C43 | A3 | R18 | D2 | U24 | D2 | | |
| C44 | A3 | R19 | D2 | U25 | D3 | | |
| C45 | B3 | R20 | D2 | U26 | A3 | | |
| C46 | B3 | R21 | D2 | U27 | A3 | | |
| C47 | C3 | R22 | D2 | U28 | B3 | | |
| C48 | C3 | R23 | D2 | U29 | A3 | | |
| C49 | A3 | R24 | C2 | U30 | A3 | | |
| C50 | D1 | R25 | C2 | U31 | B3 | | |
| D1 | -- | R26 | D2 | U32 | B3 | | |
| D2 | B1 | R27 | D2 | U33 | B3-C3 | | |
| D3 | B1 | R28 | -- | U34 | C3 | | |

COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597-0036-22

**FIGURE 7-8. COMPONENT LOCATOR, INPUT/OUTP7T CIRCUIT BOARD**




NOTES:

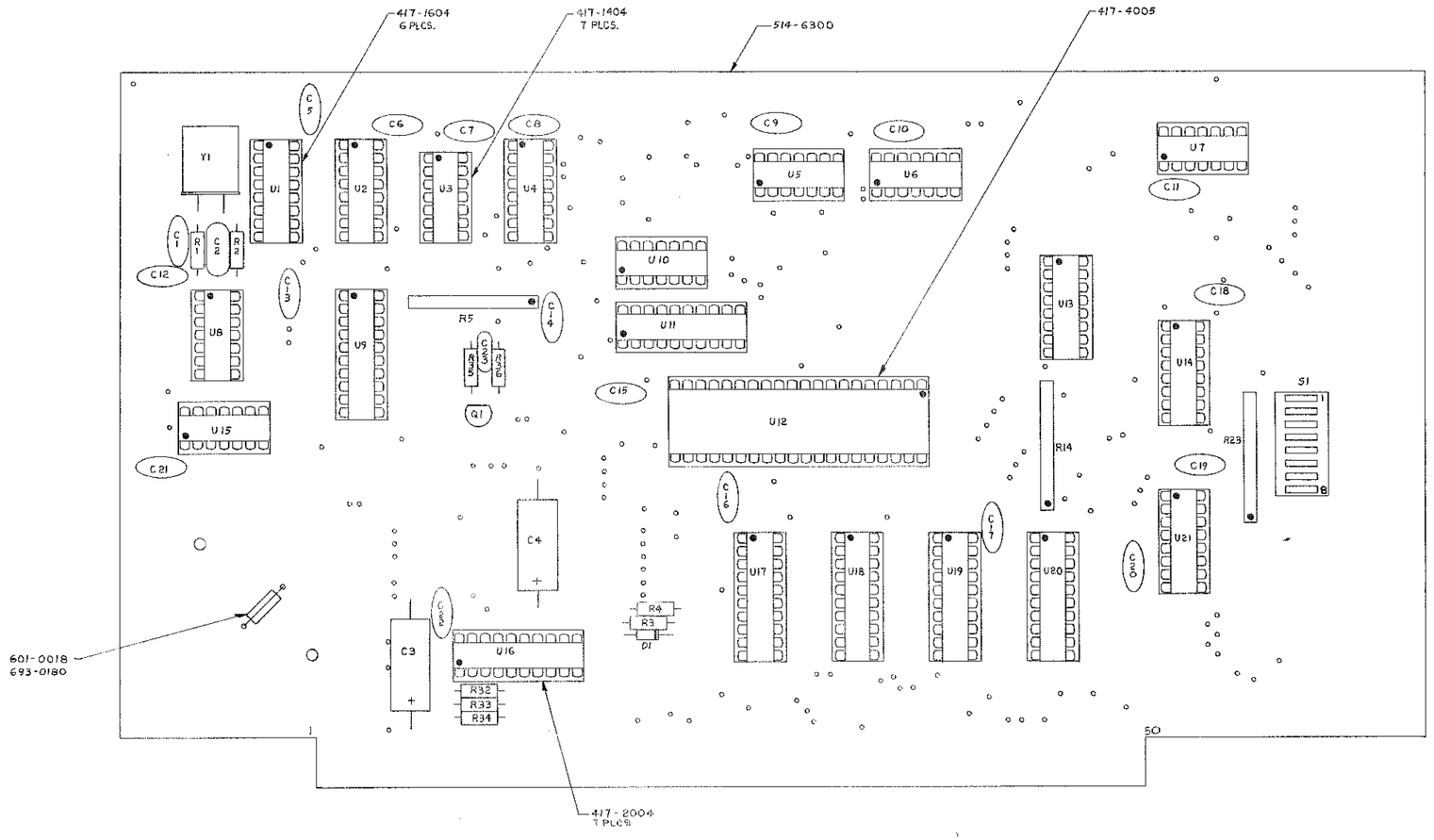
TO DISABLE POWER ON JUMP REMOVE IC'S U13 - U14 - U21 & S1.

LAST COMPONENTS USED: C23 - R36 - S1 - U21 - Q1 Y1.

COMPONENTS NOT USED: R5F, R6 - R13, R15 - R22, R24 - R31, U22.

SEE PCB ASSY. #D919-0059

| | | | |
|---|---|---|---|
| PROPRIETARY RIGHTS are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS INC. | TOLERANCE UNLESS OTHERWISE SPECIFIED: DECIMAL ± .01 3PL .005; FRACTIONAL ± 1/64; ANGULAR ± 1; SHARP EDGES TO BEND RADII; FILLET RADII | DRAWN BY T.B. DATE 2-7-83; CHECKED BY DATE; PROJECT ENGR DATE 5-26-83; APPROVED BY MH 5-26-83 | BROADCAST ELECTRONICS INC. |
| | MATERIAL | TREATMENT OR FINISH | TITLE SCHEMATIC CPU BOARD |
| | | | D DWG NO TYPE S 919-0059 REV. B |
| | | | TRANSMITTER CONTROLLER SCALE SHEET 1 OF 1 |




SEE B/M # 919-0059
SEE SCHEMATIC # D919-0059

**PROPRIETARY RIGHTS** are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE UNLESS OTHERWISE SPECIFIED
DECIMAL 2 PL= .01 3PL=.005
FRACTIONAL ±1/64
ANGULAR ± 1°
SHARP EDGES TO BEND RADII
FILLET RADII
MATERIAL

DRAWN BY T.B. DATE 2-4-83
CHECKED BY DATE
PROJECT ENGR. DATE 5-26-83
APPROVED BY MH

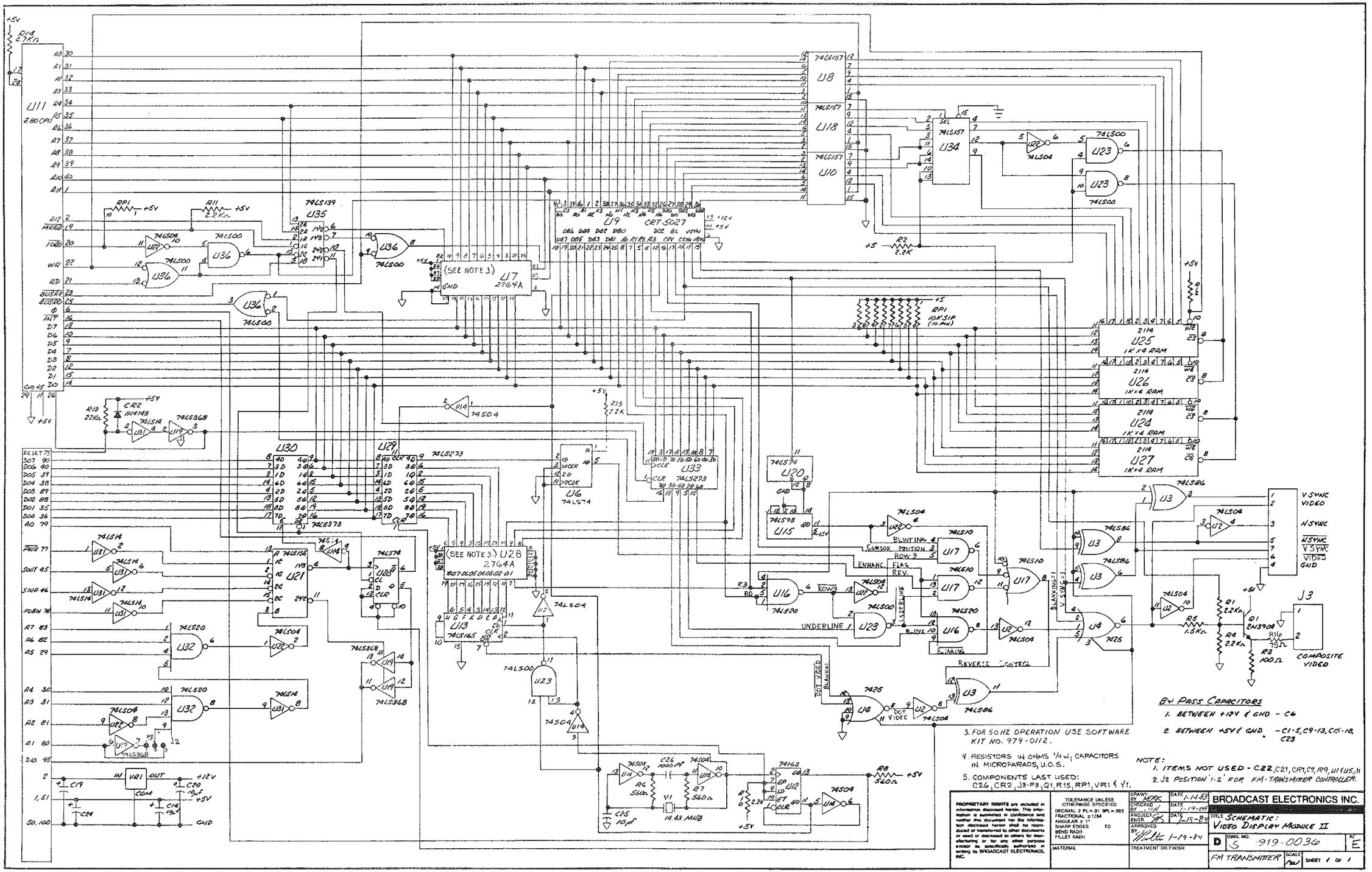
TREATMENT OR FINISH

BROADCAST ELECTRONICS INC.

TITLE PCB ASSEMBLY CPU BOARD

D | OWG. NO. TYPE A 919-0059 | REV. C

TRANSMITTER CONTROLLER | SCALE 2/1 | SHEET 1 OF 1




## By Pass Capacitors

1. Between +12V & GND – C6
2. Between +5V & GND – C1-5, C9-13, C15-18, C23

NOTE:
1. ITEMS NOT USED – C22, C21, CR1, C7, R9, U1 FUSE
2. J2 POSITION 1-2 FOR FM TRANSMITTER CONTROLLER.

3. FOR 50 HZ OPERATION USE SOFTWARE KIT NO. 979-0112.
4. RESISTORS IN OHMS 1/4 W; CAPACITORS IN MICROFARADS, U.O.S.
5. COMPONENTS LAST USED: C26, CR2, J3-P3, Q1, R15, RP1, VR1 & Y1.

PROPRIETARY RIGHTS are included in information disclosed hereon. The information is submitted in confidence and neither this document nor the information disclosed hereon shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE UNLESS OTHERWISE SPECIFIED
DECIMAL: 2 PL = .01 3PL = .005
FRACTIONAL ± 1/64
ANGULAR ± 1°
SHARP EDGES TO BEND RADII
FILLET RADII
MATERIAL
TREATMENT OR FINISH

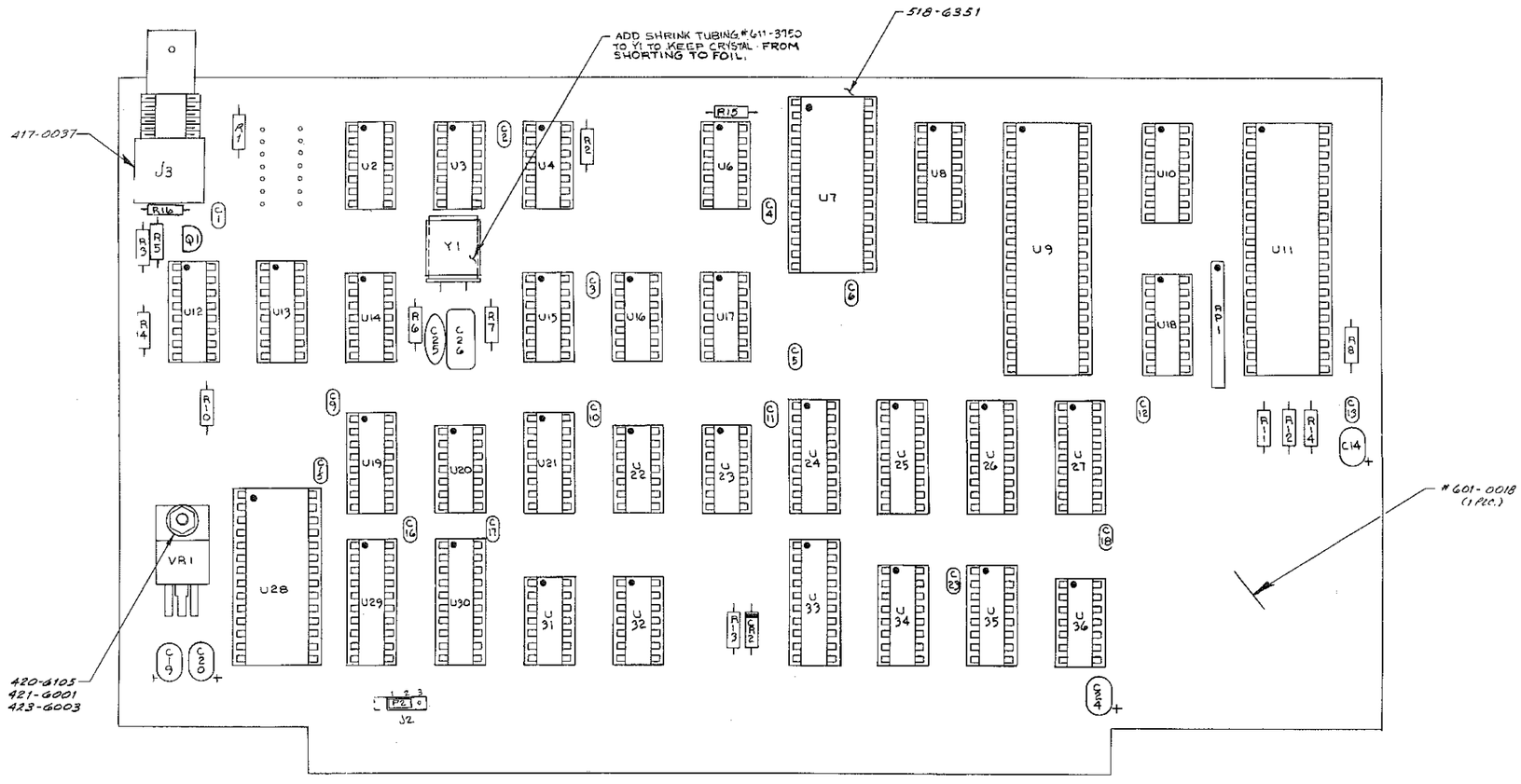
DRAWN BY MERK DATE 1-14-83
CHECKED BY DATE 1-19-84
PROJECT ENGR DATE 1-19-84
APPROVED BY 1-19-84

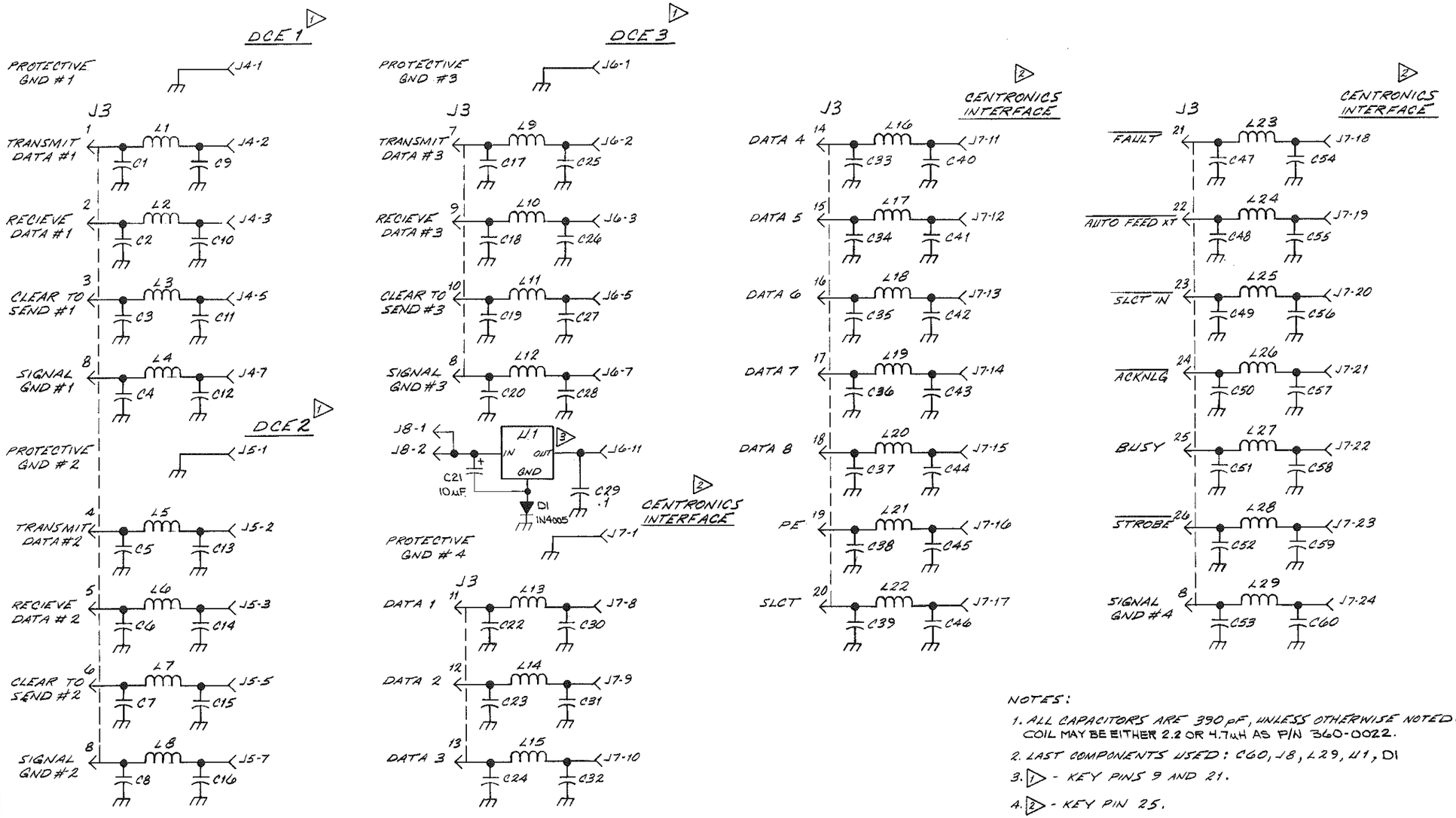
BROADCAST ELECTRONICS INC.

TITLE: SCHEMATIC: VIDEO DISPLAY MODULE II

SIZE D | DWG. NO. S-919-0036 | REV. E

FM TRANSMITTER | SCALE | SHEET 1 OF 1


ADD SHRINK TUBING #611-3150 TO Y1 TO KEEP CRYSTAL FROM SHORTING TO FOIL.
518-6351
417-0037
#601-0018 (1 REQ.)
420-6105
421-6001
423-6003
J3
J2
VR1
Y1
U2
U3
U4
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
U22
U23
U24
U25
U26
U27
U28
U29
U30
U31
U32
U33
U34
U35
U36
R15
R16
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
C24
C25
C26
C27
C28
C29
C30
C31
C32
C33
C34
C35
C36
C37
C38
C39
C40




COPYRIGHT © 1986 BROADCAST ELECTRONICS, INC.

NOTES:

1. ALL CAPACITORS ARE 390 pF, UNLESS OTHERWISE NOTED. COIL MAY BE EITHER 2.2 OR 4.7µH AS P/N 360-0022.
2. LAST COMPONENTS USED: C60, J8, L29, U1, D1
3. (1) - KEY PINS 9 AND 21.
4. (2) - KEY PIN 25.
5. (3) - HEATSINK REQUIRED, BE P/N 455-7805
6. PINS J6-25, J5-24, J4-23 & J7-4 ARE USED FOR KEYING PINS

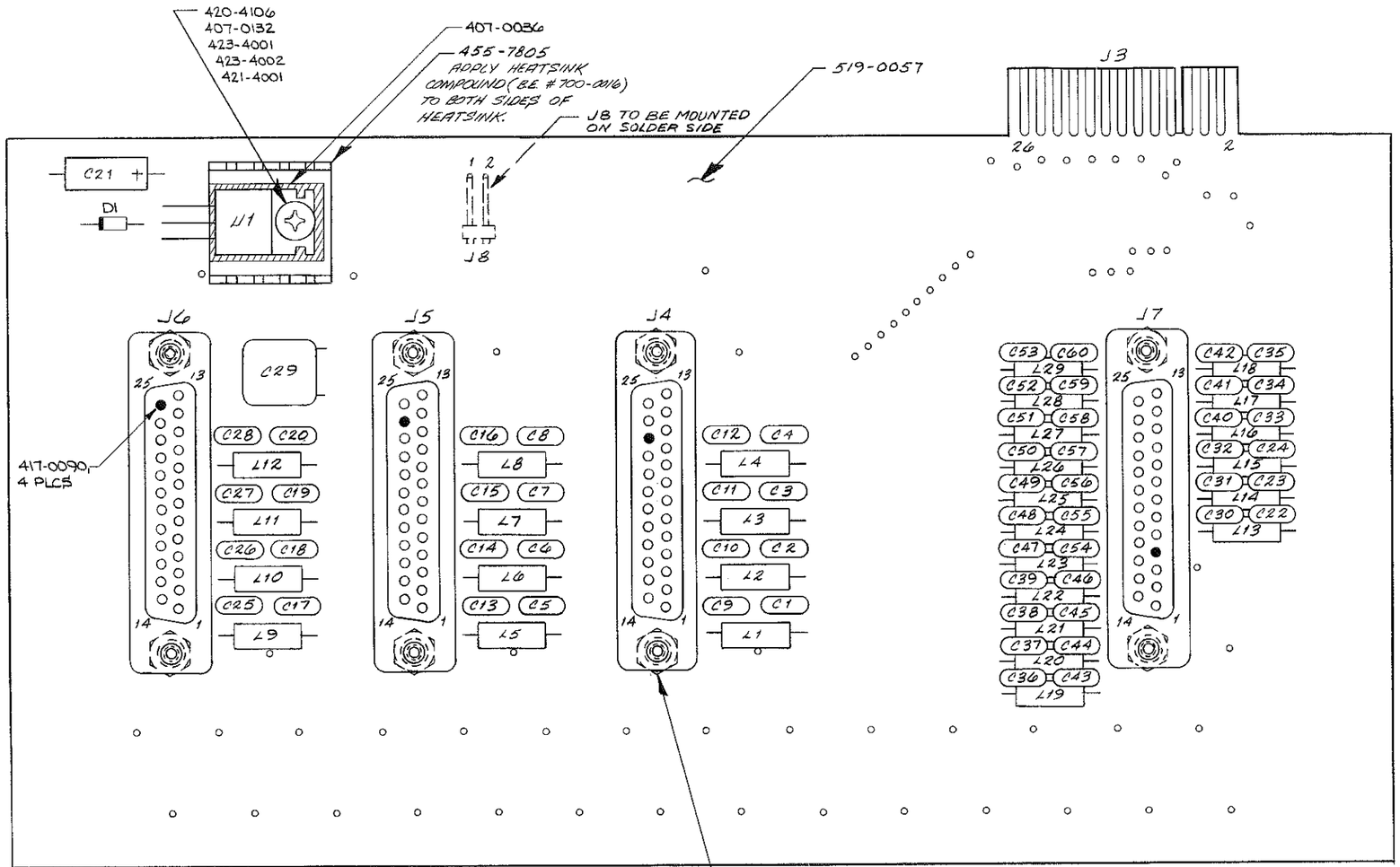
SEE ASSEMBLY #C919-0057
SEE B/M #919-0057

COPYRIGHT © 1986 BROADCAST ELECTRONICS, INC.

PROPRIETARY RIGHTS are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE (DECIMAL) U.O.S.
.X ± .030 .XXX ± .005
.XX ± .015 ANGLES ± 1°

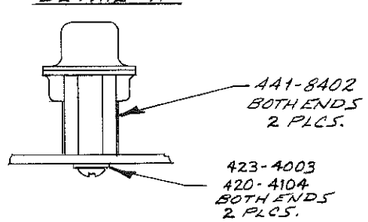
| | | | |
|---|---|---|---|
| DWN. BY MARKEL 1-27-83 | NEXT ASSY 959-0046 | BROADCAST ELECTRONICS INC. | |
| CHKD. | | 4100 N. 24TH ST. QUINCY, IL 62305 217/224-9600 | |
| ME | PRODUCT USED ON FM-XMTRS | TELEX 250142 CABLE BCST ELECT QUI | |
| EE 1-19-84 | | TITLE PCB SCHEMATIC — MICROPROCESSOR EMI FILTER BOARD | SHEET 1 OF 1 |
| PROJ. ENGR. 1-19-84 | FINISH | | SCALE — REV D |
| DPTG. SUPVR. 1-19-84 | | TYPE 5 SIZE C | DWG. NO. 919-0057 |
| MFG. | | | |




COPYRIGHT © 1986 BROADCAST ELECTRONICS, INC.

NOTE:
L1 - L28 MAY BE EITHER 2.2 OR 4.7 µH AS P/N 360-0022

DETAIL "A"




COPYRIGHT © 1986 BROADCAST ELECTRONICS, INC.

PROPRIETARY RIGHTS are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE (DECIMAL) U.O.S.
.X ± .030 .XXX ± .005
.XX ± .015 ANGLES ± 1°

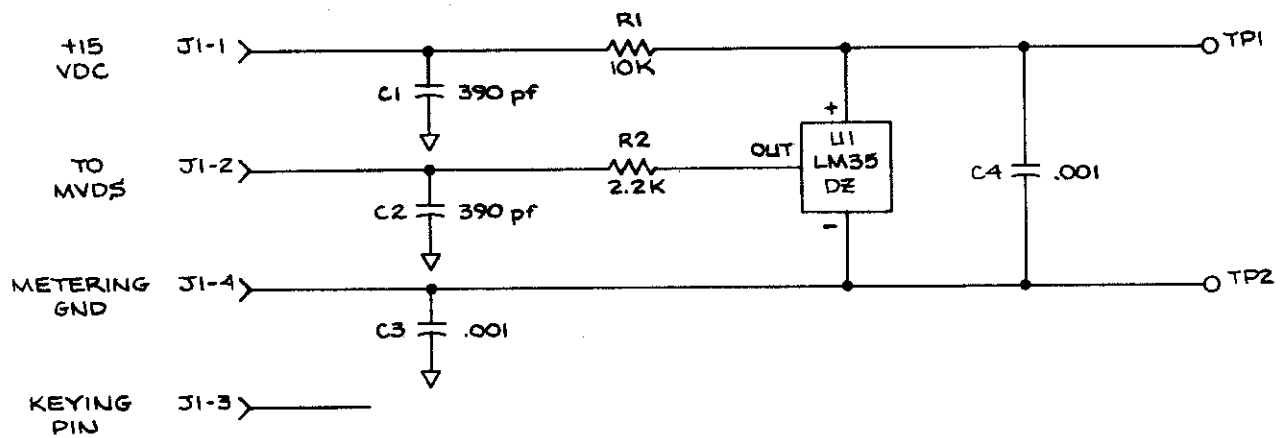
DWN. BY MERKEL 1-26-83
CHKD.
ME
EE 1-19-84
PROJ. ENGR. 1-19-84
DFTG. SUPVR. MH 1-19-84
MFG.

NEXT ASSY. 959-0046
PRODUCT USED ON FM-XMTRS
FINISH

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST. QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BCST ELECT QUI

TITLE PCB ASSEMBLY — MICROPROCESSOR EMI FILTER BOARD
SHEET 1 OF 1
SCALE 2/1
REV G
TYPE A
SIZE C
DWG. NO. 919-0057

| REVISIONS | | | | | |
|---|---|---|---|---|---|
| REV | DATE | DESCRIPTION | DFTSMN | ENGR | ECN |
| A | 5-22-84 | ENGINEERING RELEASE | MK | JMK | — |




NOTES:
1) ALL RESISTORS IN OHMS 1/4 WATT, 5%, ALL CAPACITORS IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.
2) LAST COMPONENT USED: C4, J1, R2, TP2, U1

COPYRIGHT © 1985 BROADCAST ELECTRONICS, INC.

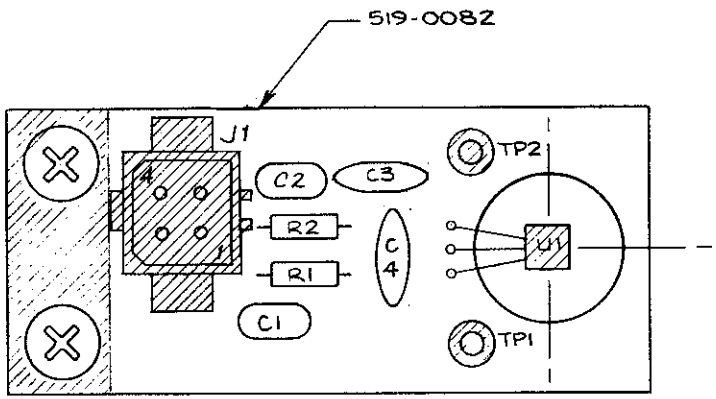
PROPRIETARY RIGHTS are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

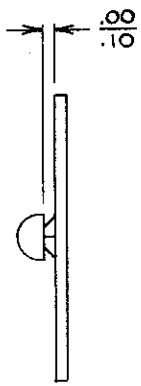
TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

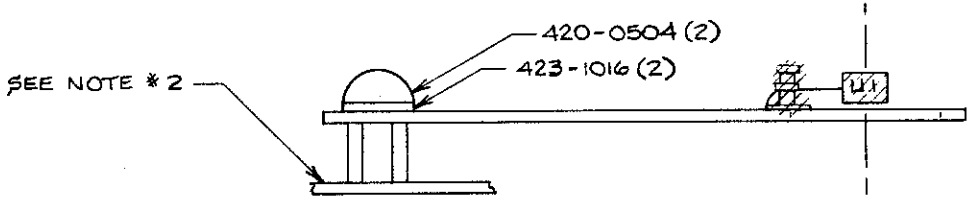
DWN. BY MSE 5-17-84
CHK'D MA 5-22-84
M/E
PROJ. ENGR. JMK 5-22-84
MFG.
MATERIAL
FINISH
NEXT ASSY.

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O. BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE SCHEMATIC, EXHAUST AIR TEMPERATURE SENSOR, PCB
TYPE S SIZE B DWG. NO. 919-0082 REV A
MODEL FM3.5A/5A MVDS OPTION SCALE ~ SHEET 1 OF 1




NOTES:
1) U1 CENTERED IN .630 HOLE.
2) BOARD SHOWN MOUNTED TO 959-0048 SHIELD CELL ASM.
3) SEE SCHEMATIC 919-0082
4) COVER WITH URETHANE CONFORMAL COATING (700-0126) AFTER COMPONENTS ARE SOLDERED. SEE COATING INSTRUCTIONS.

COATING INSTRUCTIONS:
1) MASK BODY OF DEVICE U1 COMPLETELY, MASK TURRETS TP1 + TP2, INSERT 418-0240 DUMMY PLUG IN J1, AND MASK BOTH SIDES OF PCB AT MOUNTING HOLE END AS SHADED.
2) APPLY ONE COAT OF 700-0126, SPRAY ON BOTH SIDES, PER VENDOR INSTRUCTIONS, THEN REMOVE MASKING.
3) ALLOW 15 MINS. DRYING TIME.

**PROPRIETARY RIGHTS** are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY MSE 5-17-84
CHKD MH 5-22-84
ME
PROJ. ENGR. 5-31-84
MFG.

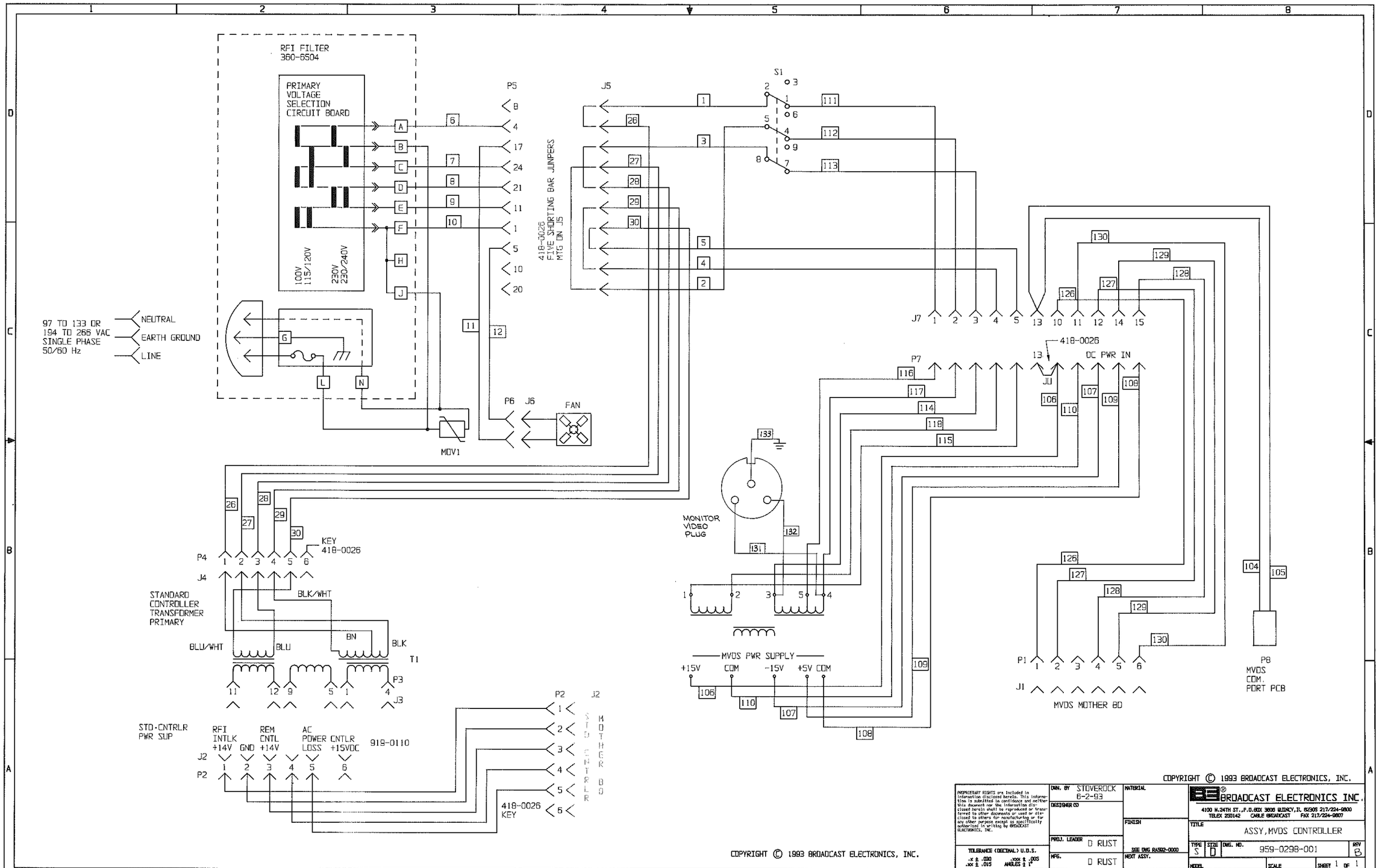
MATERIAL SEE B/M 919-0082
FINISH
NEXT ASSY.

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O. BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE ASM., PCB EXHAUST AIR TEMPERATURE SENSOR

| TYPE | SIZE | DWG. NO. | REV |
|---|---|---|---|
| A | B | 919-0082 | B |

MODEL FM3.5A/5A MVDS OPTION | SCALE 2/1 | SHEET 1 OF 1




COPYRIGHT © 1993 BROADCAST ELECTRONICS, INC.

PROPRIETARY RIGHTS are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE (DECIMAL) U.D.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY STOVEROCK 6-2-93
DESIGNER (S)
PROJ. LEADER D RUST
MFG. D RUST
MATERIAL
FINISH
SEE DWG RA502-0000
NEXT ASSY.

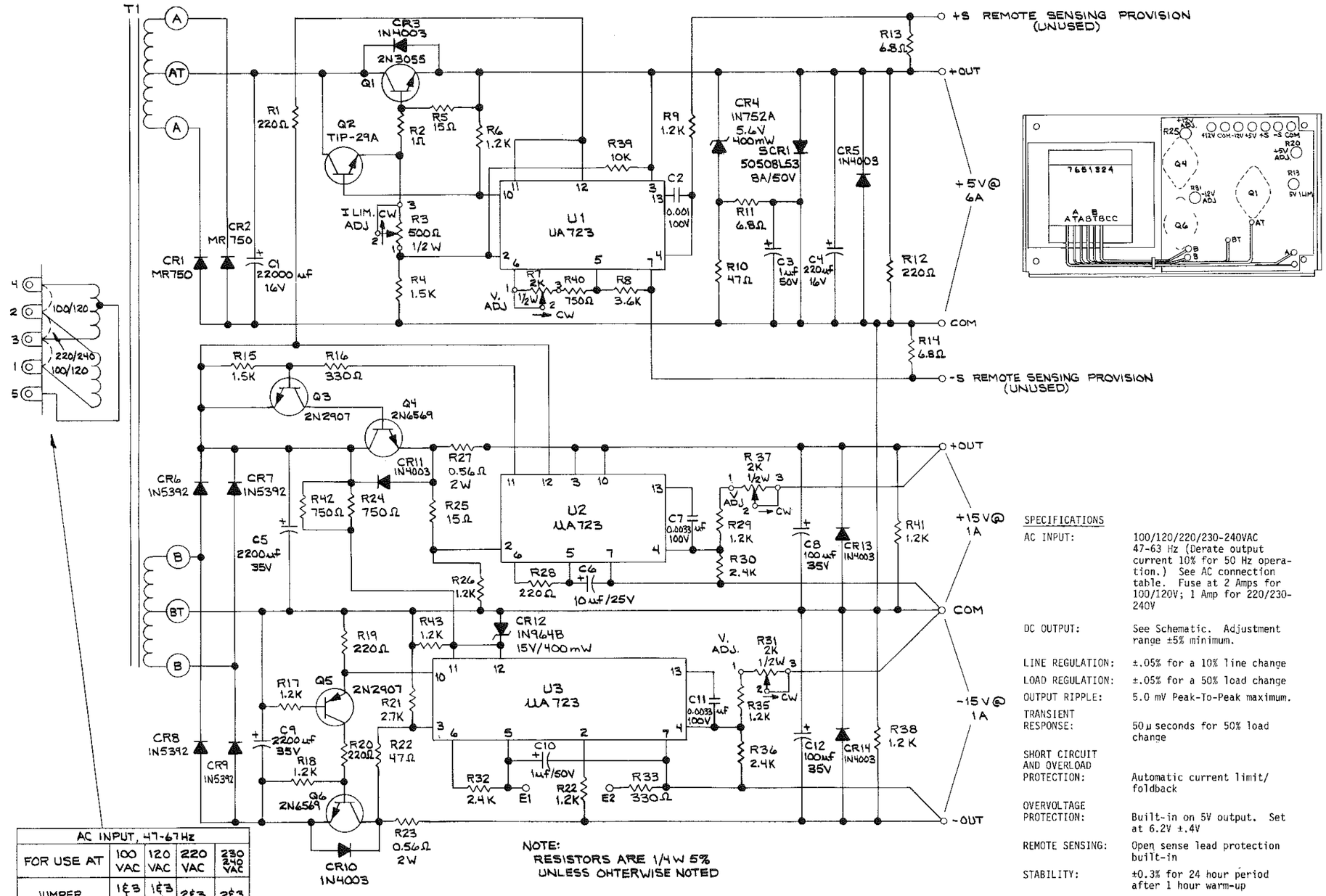
BROADCAST ELECTRONICS INC.
4100 N.24TH ST., P.O.BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST FAX 217/224-9607

TITLE ASSY, MVDS CONTROLLER

TYPE S | SIZE D | DWG. NO. 959-0298-001 | REV B

MODEL | SCALE | SHEET 1 OF 1

COPYRIGHT © 1993 BROADCAST ELECTRONICS, INC.




| AC INPUT, 47-67Hz | | | | |
|---|---|---|---|---|
| FOR USE AT | 100 VAC | 120 VAC | 220 VAC | 230 240 VAC |
| JUMPER | 1&3 2&4 | 1&3 2&4 | 2&3 | 2&3 |
| APPLY AC | 1&5 | 4&1 | 1&4 | 4&1 |

TOLERANCE FOR 100/120/220 VAC OPERATION IS +10%,-13%
TOLERANCE FOR 230/240 VAC OPERATION IS+15%,-10%

NOTE:
RESISTORS ARE 1/4W 5%
UNLESS OHTERWISE NOTED

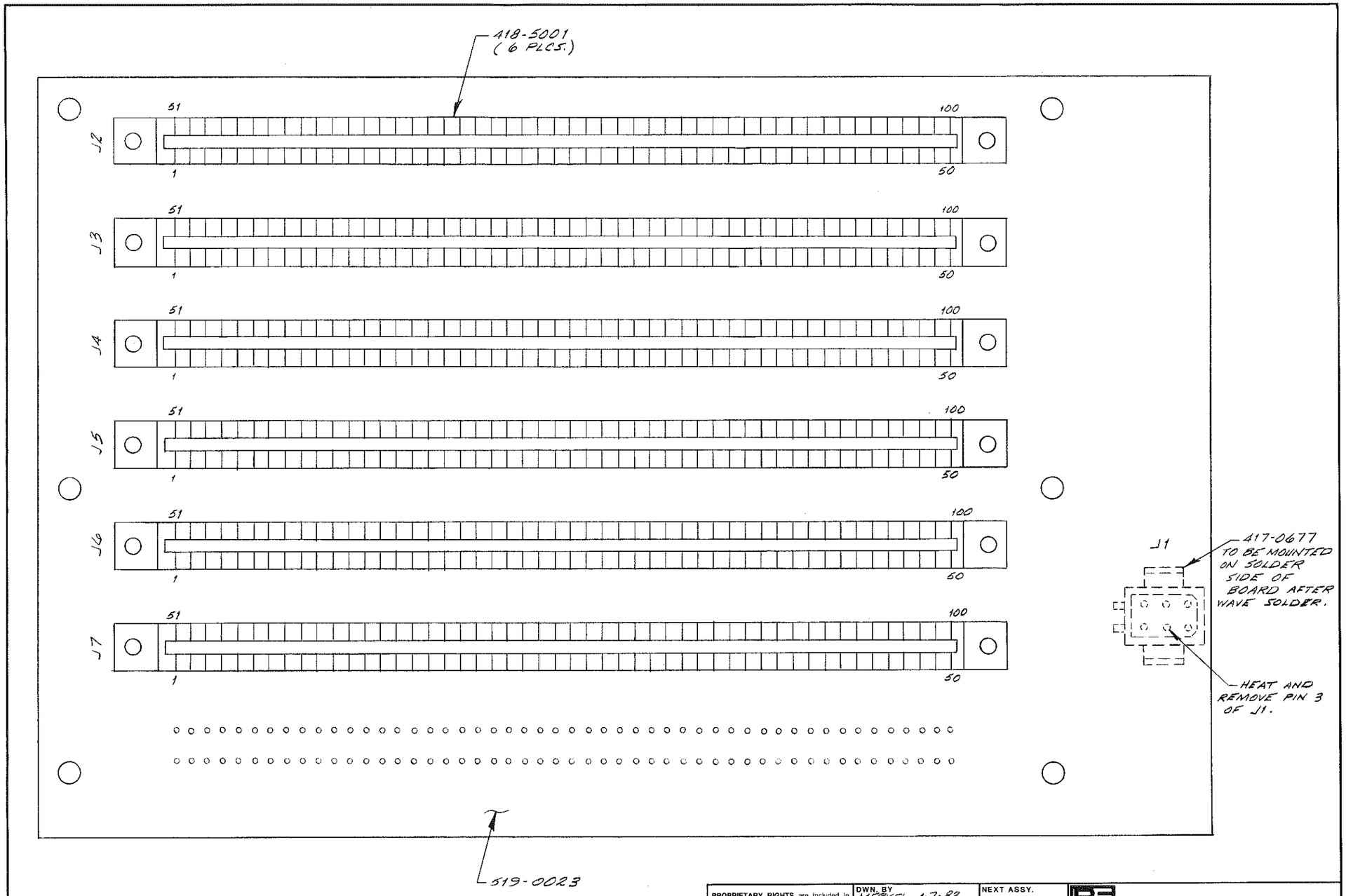
SPECIFICATIONS

| | |
|---|---|
| AC INPUT: | 100/120/220/230-240VAC 47-63 Hz (Derate output current 10% for 50 Hz operation.) See AC connection table. Fuse at 2 Amps for 100/120V; 1 Amp for 220/230-240V |
| DC OUTPUT: | See Schematic. Adjustment range ±5% minimum. |
| LINE REGULATION: | ±.05% for a 10% line change |
| LOAD REGULATION: | ±.05% for a 50% load change |
| OUTPUT RIPPLE: | 5.0 mV Peak-To-Peak maximum. |
| TRANSIENT RESPONSE: | 50 μ seconds for 50% load change |
| SHORT CIRCUIT AND OVERLOAD PROTECTION: | Automatic current limit/ foldback |
| OVERVOLTAGE PROTECTION: | Built-in on 5V output. Set at 6.2V ±.4V |
| REMOTE SENSING: | Open sense lead protection built-in |
| STABILITY: | ±0.3% for 24 hour period after 1 hour warm-up |
| TEMPERATURE RATING: | 0°C to 50°C full-rated, derated linearly to 40% at 70°C |
| TEMPERATURE COEFFICIENT: | ±.03%/°C maximum |
| EFFICIENCY: (Typical) | 5V 45%; 15V 55% |

COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597-0036-23

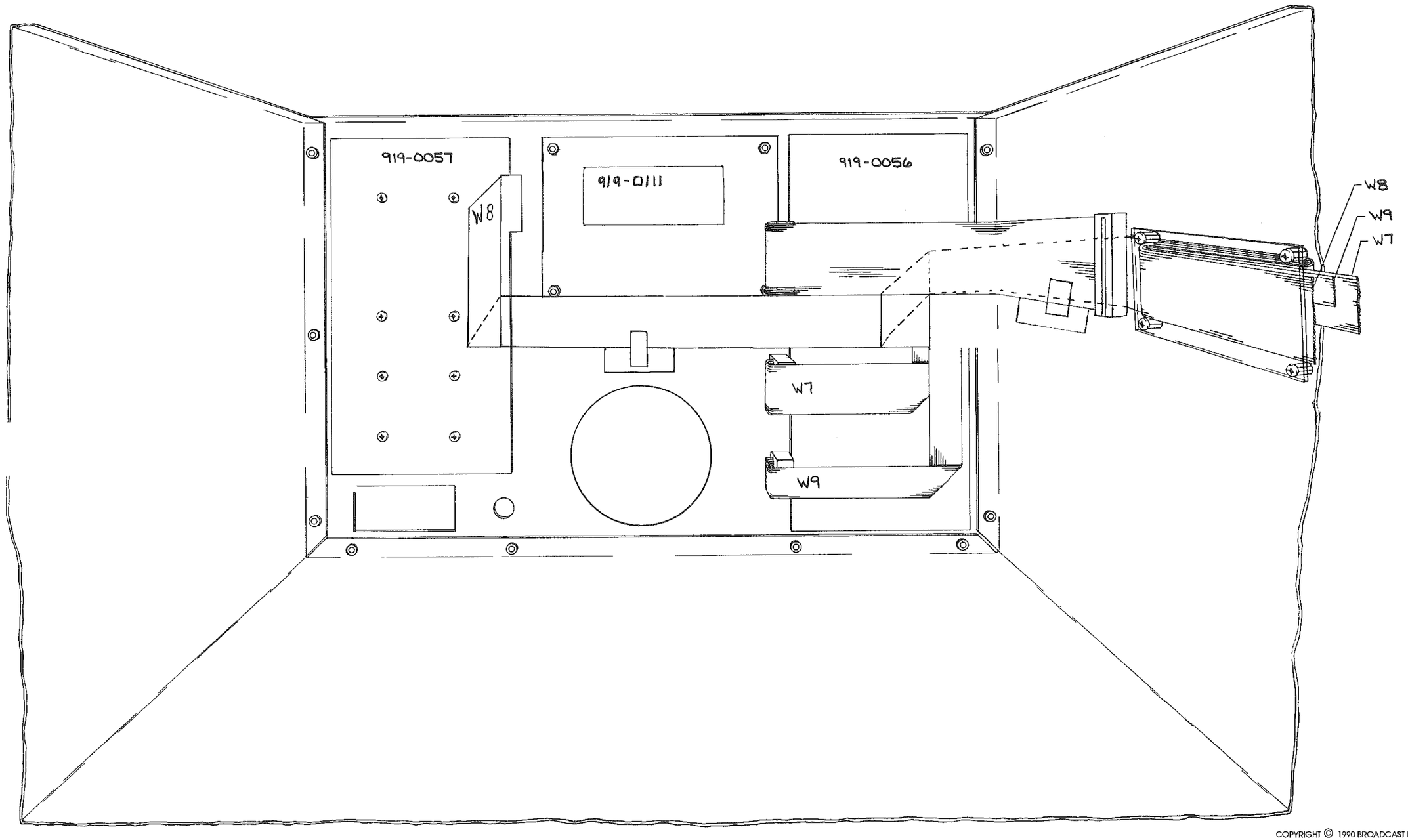
**FIGURE 7-18. SCHEMATIC DIAGRAM POWER SUPPLY**




**PROPRIETARY RIGHTS** are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE (DECIMAL) U.O.S.
.X ± .030 .XXX ± .005
.XX ± .015 ANGLES ± 1°

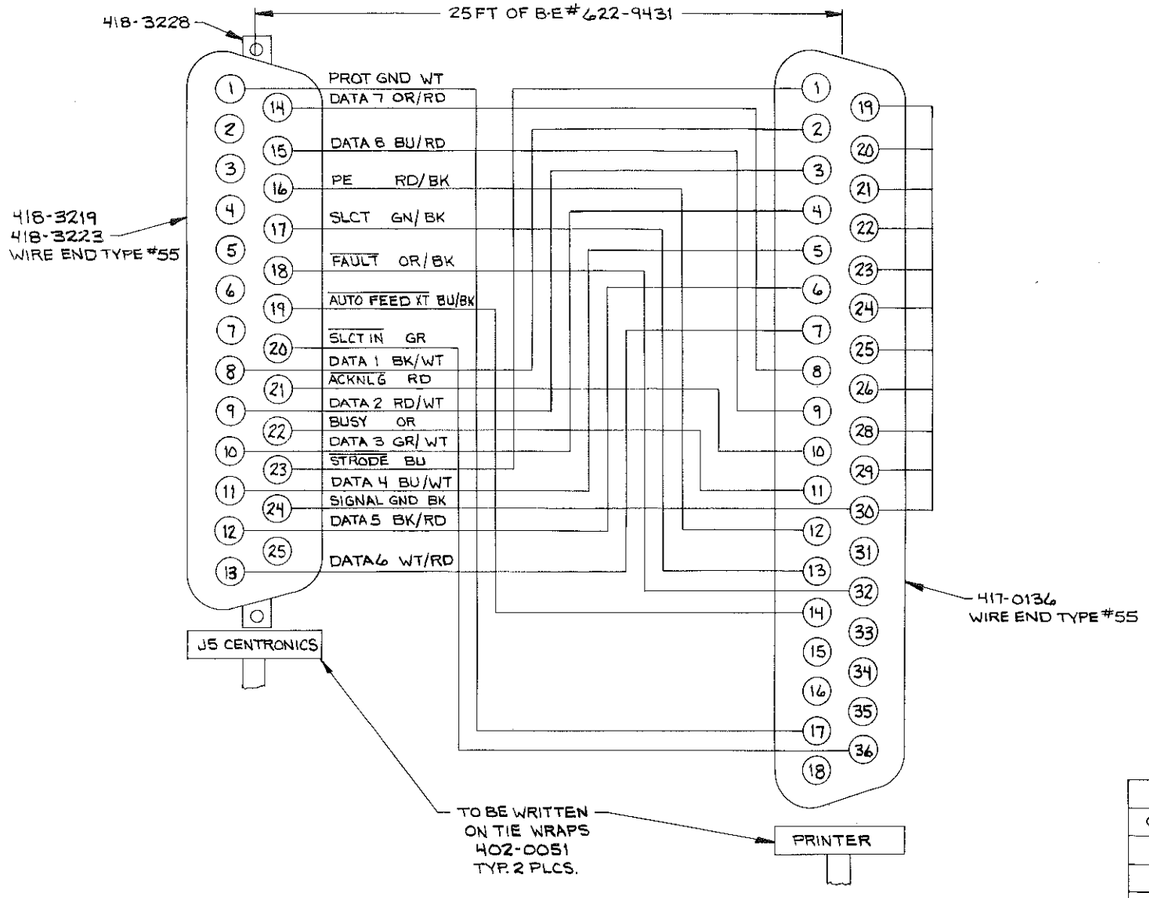
| | | |
|---|---|---|
| DWN. BY MERRELL 1-7-83 | NEXT ASSY. | BROADCAST ELECTRONICS INC. |
| CHKD. | | 4100 N. 24TH ST. QUINCY, IL 62305 217/224-9600 |
| ME | PRODUCT USED ON TRANSMITTER CONTROLLER | TELEX 250142 CABLE BCST ELECT QUI |
| EE 5-26-83 | | TITLE PCB ASSEMBLY - MICROPROCESSOR MOTHERBOARD |
| PROJ. ENGR. 5-26-83 | FINISH | SHEET 1 OF 1 |
| DFTG. SUPVR. 5-26-83 MJA | | SCALE 2/1 REV C |
| MFG. | | TYPE A SIZE C DWG. NO. 919-0023 |




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597-0036-24

FIGURE 7-20. ASSEMBLY DIAGRAM, CONTROLLER CABINET RIBBON CABLES




| PARTS LIST | | |
|---|---|---|
| QTY | B-E P/N | DESCRIPTION |
| 1 | 418-3219 | CONNECTOR, 25-PIN |
| 1 | 417-0136 | CONNECTOR, 36-PIN (CENTRONICS) |
| 25 FT | 622-9431 | CABLE, 20 CONDUCTOR |
| 1 | 418-3223 | CONNECTOR, HOOD |
| 1 | 418-3228 | LOCKING KIT |

NOTE:
REMAINING HOLES OF CONNECTOR TO BE FILLED WITH EMPTY PINS

COPYRIGHT © 1985 BROADCAST ELECTRONICS, INC.

COPYRIGHT © 1985 BROADCAST ELECTRONICS, INC.

PROPRIETARY RIGHTS are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY JAH 10-3-84
CHKD
ME
PROJ. ENGR.
MFG.
MATERIAL
FINISH
NEXT ASSY.

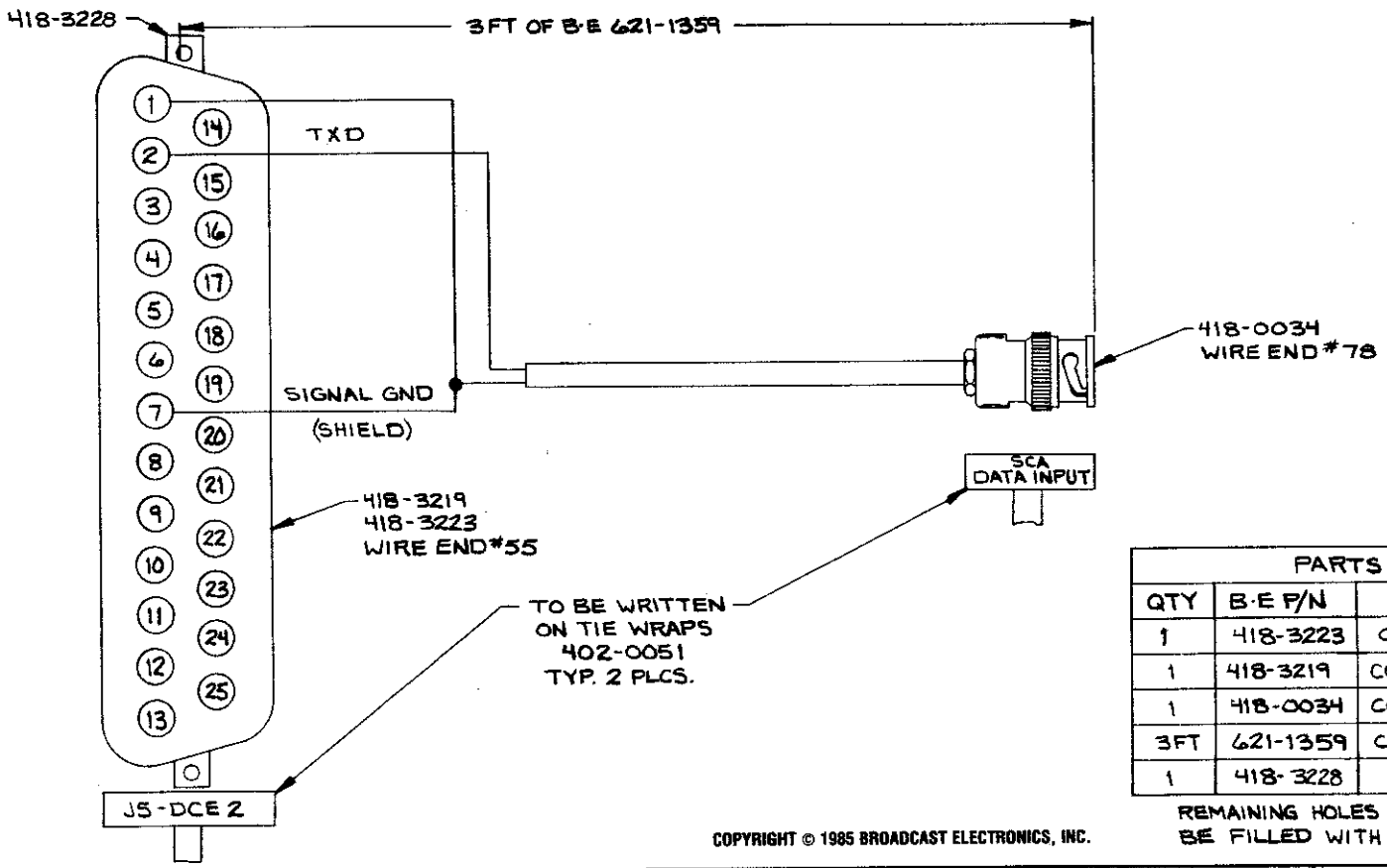
BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O. BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE CABLE ASSEMBLY, MVDS LOCAL PARALLEL PRINTER LOGGING

TYPE A | SIZE C | DWG. NO. 949-0110 | REV A

MODEL FM XMTR | SCALE — | SHEET 1 OF 1

| REVISIONS | | | | | |
|---|---|---|---|---|---|
| REV | DATE | DESCRIPTION | DFTSMN | ENGR | ECN |




| PARTS LIST | | |
|---|---|---|
| QTY | B·E P/N | DESCRIPTION |
| 1 | 418-3223 | CONNECTOR, HOOD |
| 1 | 418-3219 | CONNECTOR, 25-PIN |
| 1 | 418-0034 | CONNECTOR, BNC |
| 3FT | 621-1359 | COAX CABLE, RG316U |
| 1 | 418-3228 | LOCKING KIT |

REMAINING HOLES OF CONNECTOR TO BE FILLED WITH EMPTY PINS.

COPYRIGHT © 1985 BROADCAST ELECTRONICS, INC.

PROPRIETARY RIGHTS are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY JAH 10-3-84
CHKD
ME
PROJ. ENGR.
MFG.

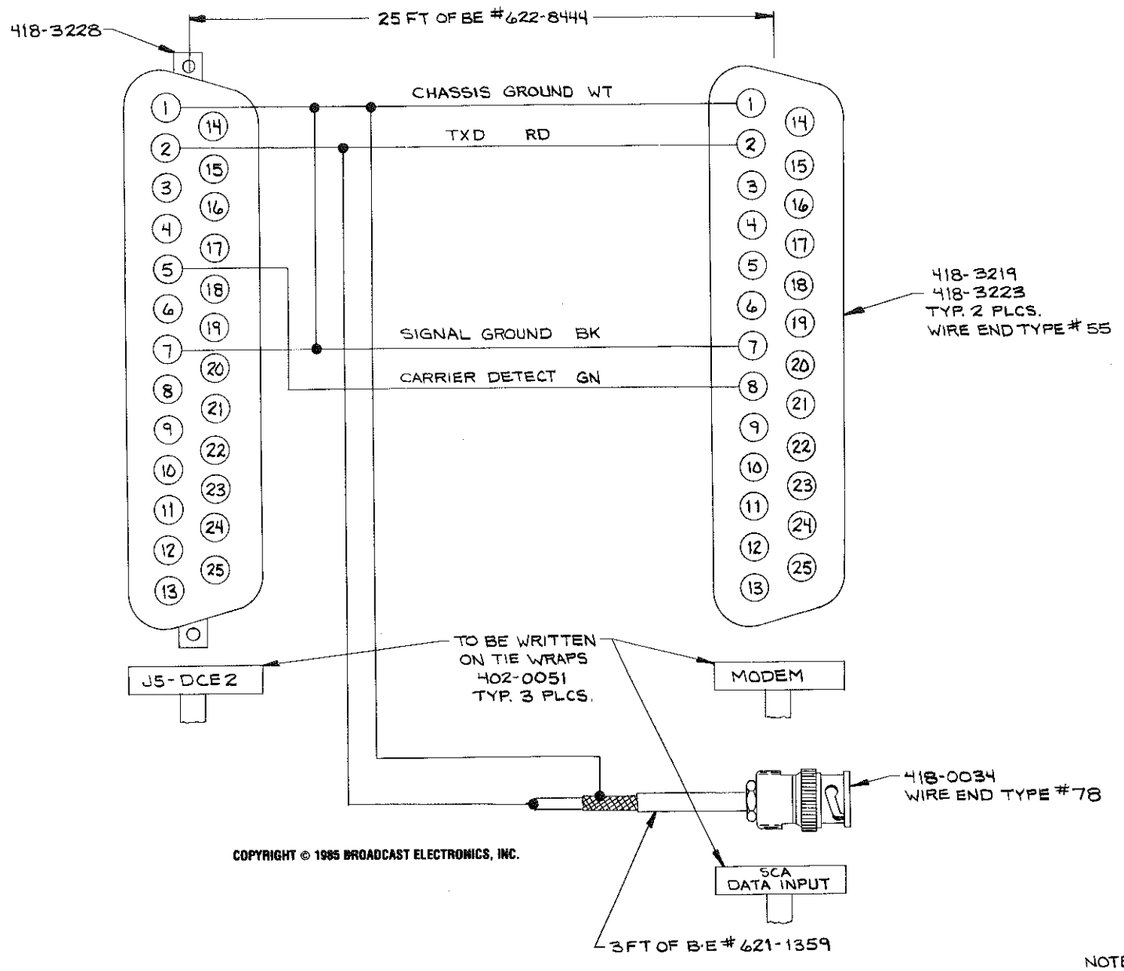
MATERIAL —
FINISH —
NEXT ASSY. —

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O. BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE CABLE ASSEMBLY, MVDS SCA LOGGING PATH

TYPE A | SIZE B | DWG. NO. 949-0111 | REV A

MODEL FM XMTR | SCALE — | SHEET 1 OF 1




COPYRIGHT © 1985 BROADCAST ELECTRONICS, INC.

| PARTS LIST | | |
|---|---|---|
| QTY | B·E P/N | DESCRIPTION |
| 2 | 418-3219 | CONNECTOR, 25-PIN |
| 1 | 418-0034 | CONNECTOR, BNC |
| 3FT | 621-1359 | COAX CABLE RG316 |
| 25FT | 622-8444 | CABLE, 4 CONDUCTOR |
| 2 | 418-3223 | CONNECTOR, HOOD |
| 1 | 418-3228 | LOCKING KIT |

NOTE:
REMAINING HOLES OF CONNECTOR TO BE FILLED WITH EMPTY PINS

COPYRIGHT © 1985 BROADCAST ELECTRONICS, INC.

**PROPRIETARY RIGHTS** are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY JAH 10-4-84
CHKD
ME
PROJ. ENGR.
MFG.

MATERIAL
FINISH —
NEXT ASSY. —

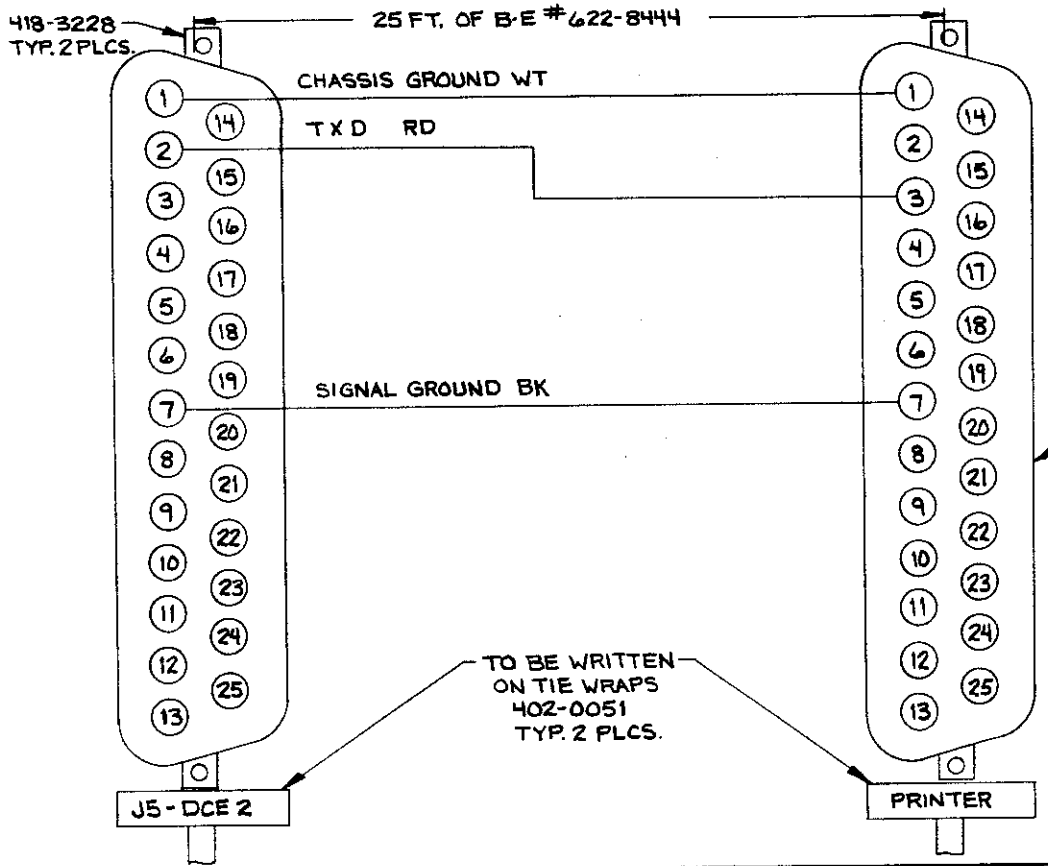
BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O.BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE CABLE ASSEMBLY, MVDS MODEM & SCA LOGGING PATHS

TYPE A | SIZE C | DWG. NO. 949-0112 | REV A

MODEL FM XMTR | SCALE — | SHEET 1 OF 1

| REVISIONS | | | | | |
|---|---|---|---|---|---|
| REV | DATE | DESCRIPTION | DFTSMN | ENGR | ECN |




| PARTS LIST | | |
|---|---|---|
| QTY | B·E P/N | DESCRIPTION |
| 2 | 418-3219 | CONNECTOR, 25-PIN |
| 25 FT | 622-8444 | CABLE, 4 CONDUCTOR |
| 2 | 418-3223 | CONNECTOR, HOOD |
| 1 | 418-3228 | LOCKING KIT |

FILL REMAINING HOLES WITH EMPTY PINS

COPYRIGHT © 1985 BROADCAST ELECTRONICS, INC.

**PROPRIETARY RIGHTS** are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY JAH 10-2-84
CHKD
ME
PROJ. ENGR.
MFG.

MATERIAL
FINISH
NEXT ASSY.

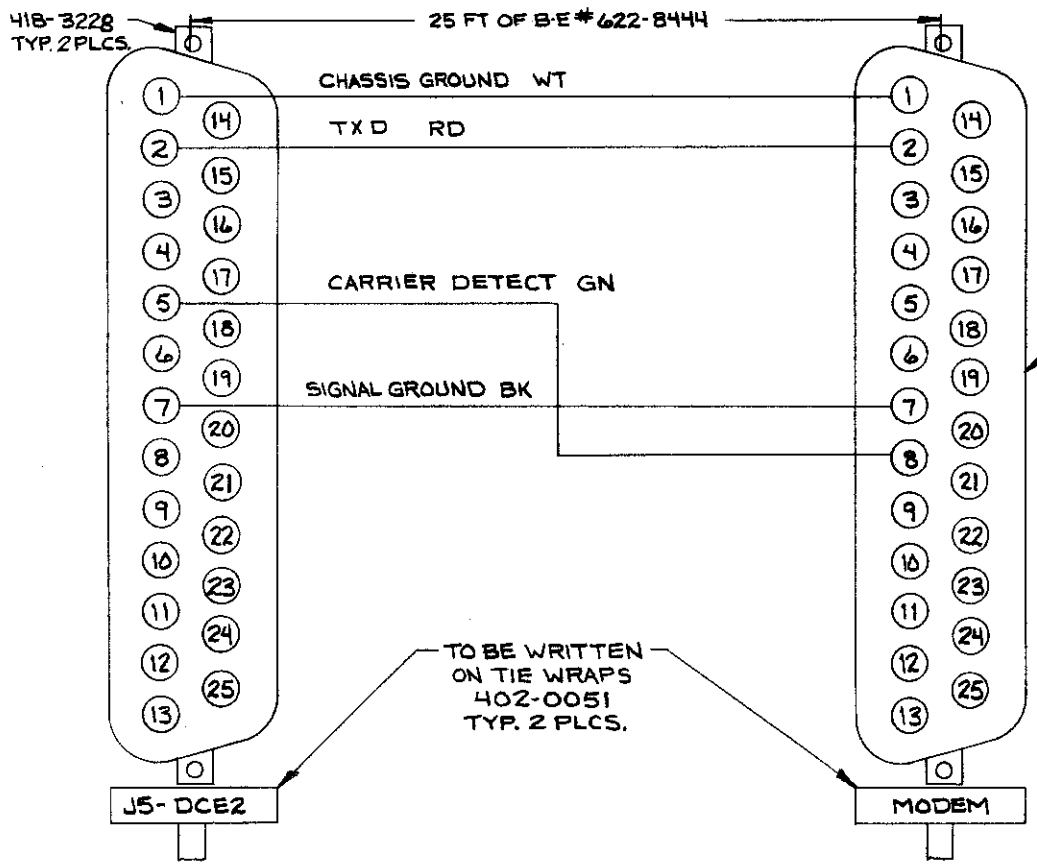
BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O. BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE CABLE ASSEMBLY, MVDS LOCAL SERIAL PRINTER LOGGING

TYPE A | SIZE B | DWG. NO. 949-0113 | REV A

MODEL FM XMTR | SCALE — | SHEET 1 OF 1

| REVISIONS | | | | | |
|---|---|---|---|---|---|
| REV | DATE | DESCRIPTION | DFTSMN | ENGR | ECN |




| PARTS LIST | | |
|---|---|---|
| QTY | B·E P/N | DESCRIPTION |
| 2 | 418-3219 | CONNECTOR, 25-PIN |
| 25FT | 622-8444 | CABLE, 4 CONDUCTOR |
| 2 | 418-3223 | CONNECTOR, HOOD |
| 1 | 418-3228 | LOCKING KIT |

NOTE:
REMAINING HOLES OF CONNECTOR TO BE FILLED WITH EMPTY PINS

COPYRIGHT © 1985 BROADCAST ELECTRONICS, INC.

PROPRIETARY RIGHTS are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY JAH 10-3-84
CHKD
ME
PROJ. ENGR.
MFG.

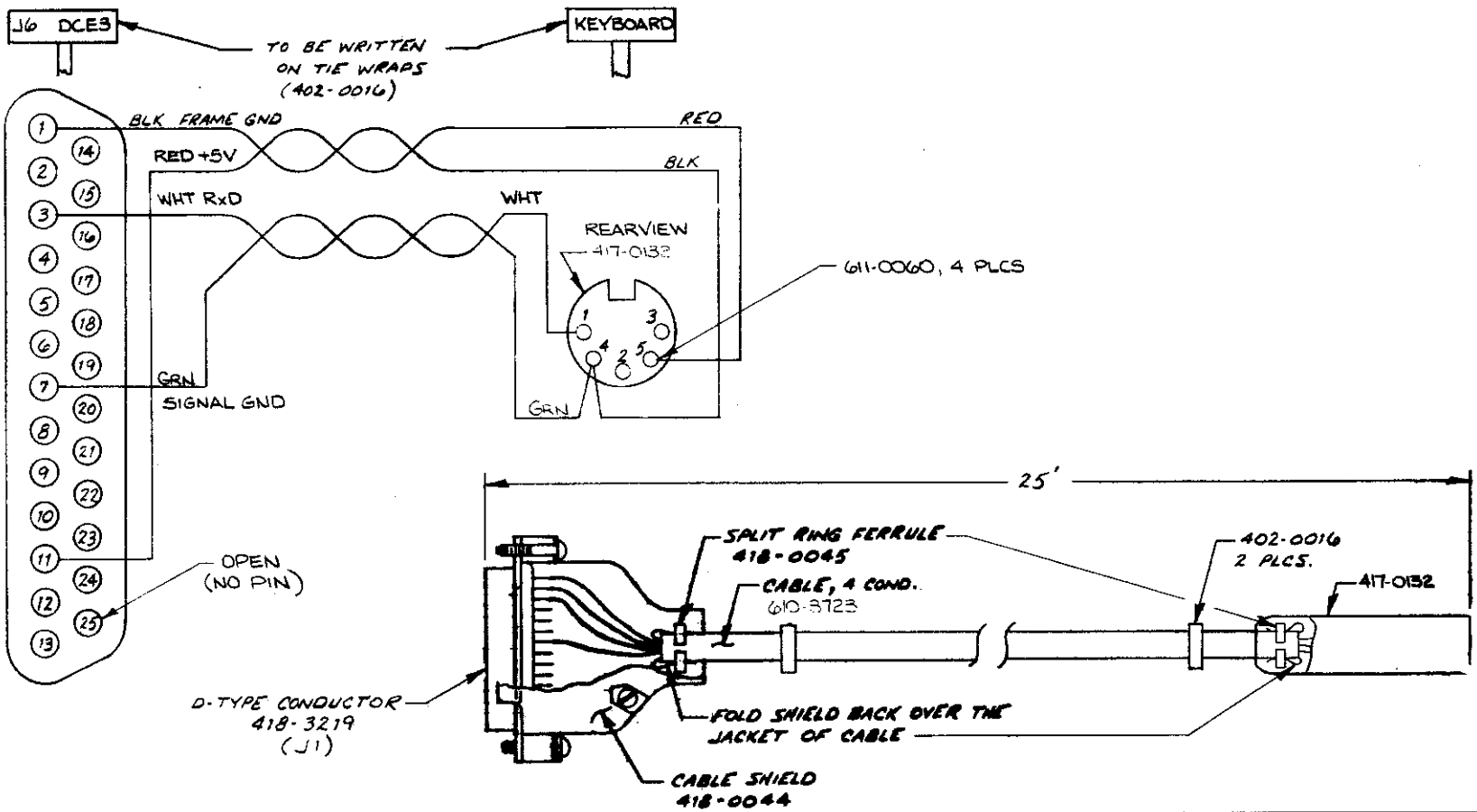
MATERIAL
FINISH
NEXT ASSY.

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O. BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE CABLE ASSEMBLY, MVDS MODEM LOGGING PATH

TYPE | SIZE B | DWG. NO. 949-0114 | REV A

MODEL FM XMTR | SCALE —— | SHEET 1 OF 1




**PROPRIETARY RIGHTS** are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1

DWN. BY MSE 6-2-86
CHKD
ME
PROJ. ENGR.
MFG.

MATERIAL —
FINISH
NEXT ASSY.

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O. BOX 3606 QUINCY, IL 62305 217 224-9600
TELEX 250142 CABLE BROADCAST

TITLE CABLE ASSEMBLY - MVDS TO MICROSWITCH KEYBOARD

TYPE A | SIZE B | DWG. NO. 949-0105 | REV H

MODEL | SCALE NL | SHEET 7 OF 8

# APPENDIX A
# MVDS MANUFACTURERS DATA

## A–1. INTRODUCTION.

A–2. This section provides the following technical data relative to the operation and maintenance of the MVDS. Information contained in this section is listed in the following order.

A. Instruction Manual, Toshiba Video Monitor, TVM–1001.

B. Instruction Sheet, CRT Video Timer–Controller, CRT 5027.

C. Instruction Sheet, Intel Programmable Communication Interface, 8251A.

D. Instruction Sheet, Zilog Central Processing Unit, Z80.

E. Instruction Sheet, Analog Devices Eight–Bit Eight–Channel DAS, AD7581L.

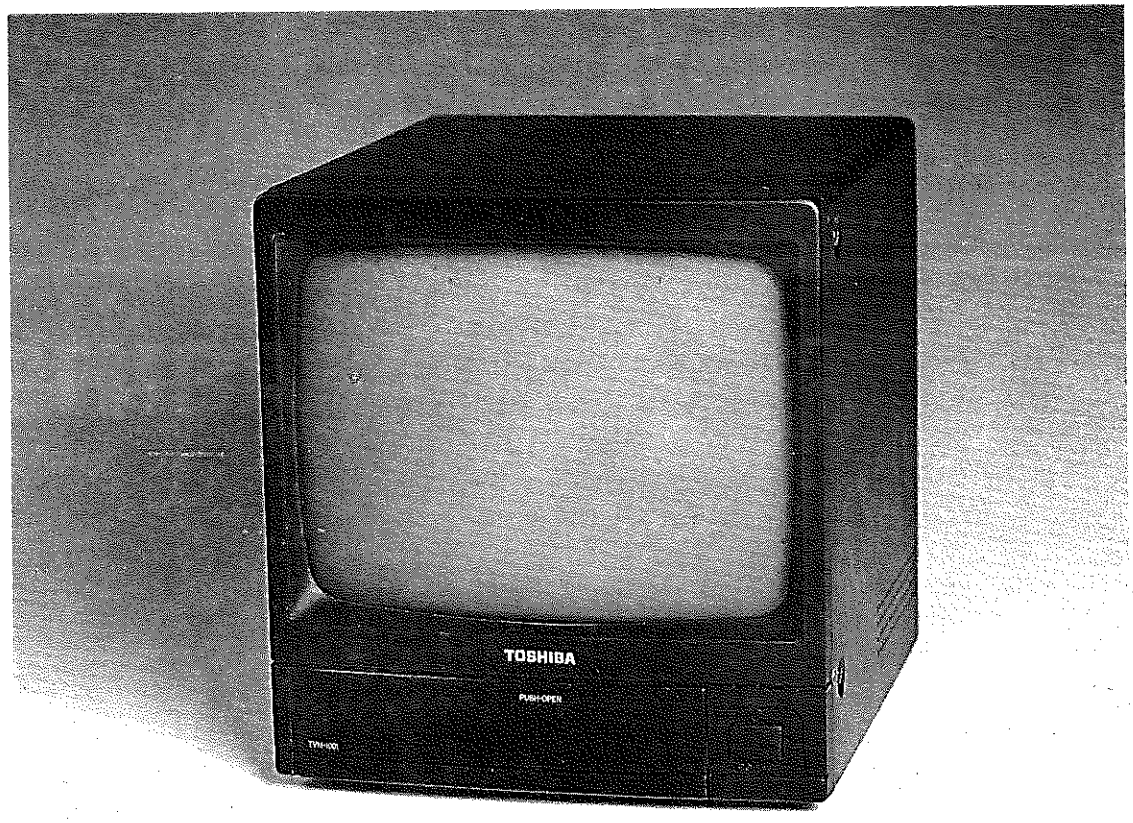
F. Instruction Sheet, Dallas Real–Time Clock, DS1287.

G. Instruction Sheet, Intel Programmable Peripheral Interface, 8255A.

# TOSHIBA

TOSHIBA VIDEO MONITOR
INSTRUCTION MANUAL

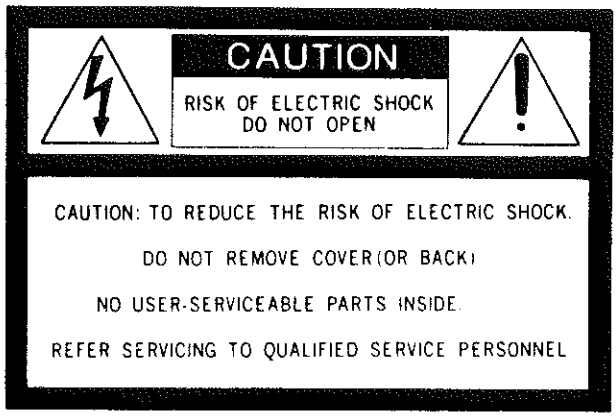
# TVM-1001



**WARNING**

TO REDUCE THE RISK OF FIRE OR SHOCK HAZARD, DO NOT EXPOSE THIS APPLIANCE TO RAIN, WATER, WET LOCATIONS.
DO NOT INSERT ANY METALLIC OBJECT THROUGH VENTILATION GRILLES.

**CAUTION**




**Explanation of Graphical Symbols**

This symbol is intended to alert the user to the presence of uninsulated "dangerous voltage" within the product's enclosure that may be of sufficient magnitude to constitute a risk of electric shock to persons.

This symbol is intended to alert the user to the presence of important operating and maintenance (Servicing) instructions in the literature accompanying the appliance.

Record in space provided below the model No. and the Serial No. as found on the lable on the back of this unit.

Model No._____

Serial No._____

Retain this information for future reference.

USER-INSTALLER CAUTION: YOUR AUTHORITY TO OPERATE THIS FCC VERIFIED EQUIPMENT COULD BE VOIDED IF YOU MAKE CHANGES OR MODIFICATIONS NOT EXPRESSLY APPROVED BY THE PARTY RESPONSIBLE FOR COMPLIANCE TO PART 15 OF THE FCC RULES.

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

THIS DIGITAL APPARATUS DOES NOT EXCEED THE CLASS A LIMITS FOR RADIO NOISE EMISSIONS FROM DIGITAL APPARATUS SET OUT IN THE RADIO INTERFERENCE REGULATIONS OF THE CANADIAN DEPARTMENT OF COMMUNICATIONS.

LE PRÉSENT APPAREIL NUMÉRIQUE N'EMET PAS DE BRUITS RADIOÉLECTRIQUES DÉPASSANT LES LIMITES APPLICABLES AUX APPAREILS NUMÉRIQUES DE LA CLASS A PRESCRITES DANSLE RÉGLEMENT SUR LE BROUILLAGE DADIOÉLECTRIQUE ÉDICTÉ PAR LE MINISTÈRE DES COMMUNICATIONS DU CANADA.

## ■ SPECIFICATIONS

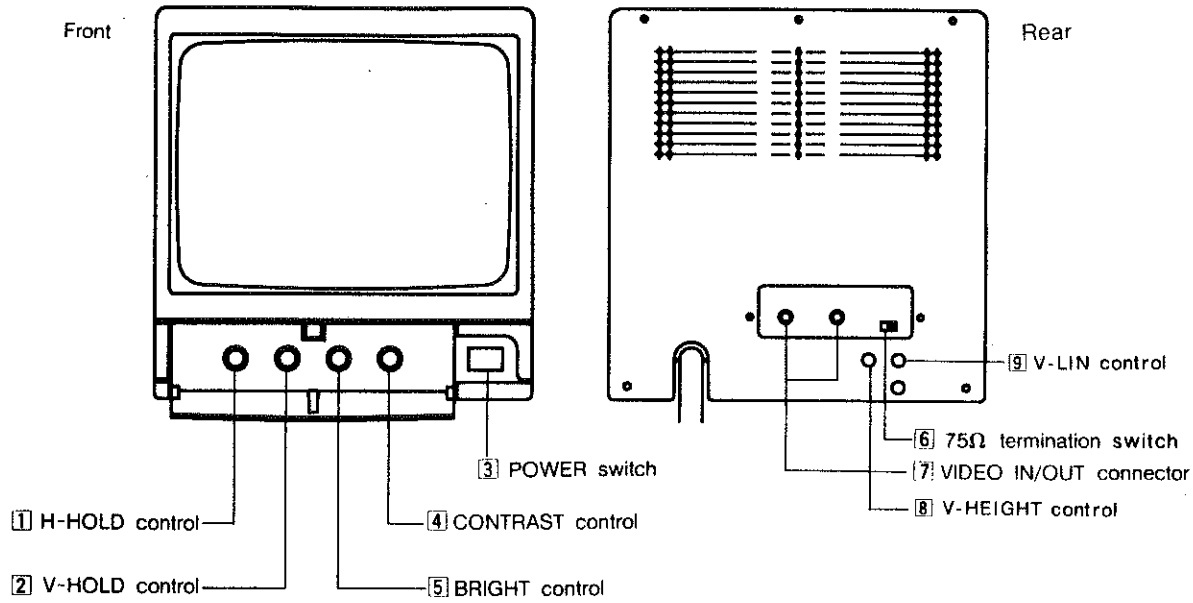
| | |
|---|---|
| Picture Tube | 10-inch Diagonal, 90° Deflection Angle |
| Power Source | AC120V, 60Hz |
| Power Consumption | 27 Watts |
| System | EIA standard |
| Resolution | More than 800 TV lines (center) |
| Video input impedance | High impedance for loop-through;75Ω terminated |
| Video output impedance | Over 10k Ω |
| Video Input | Composite 0.5-2Vp-p, Sync Negative |
| Video Output | Composite 0.5-2Vp-p, Sync Negative |
| Dimensions | 220×237×247m/m(8.66×9.33×9.72 inch) |
| Weight | 5.90Kg(12.98 lbs) |
| Ambient Temperature | -10℃~40℃(Performance Range) |

**Design and specifications subject to change without notice.**

## FEATURES

- Possible use as a closed circuit television monitor or a video preview/playback monitor.
- Loop through connection.
- Electronic circuits provide safeguards against interference, noise and changing signal strength to maintain a clear and stable picture.

## OPERATING INSTRUCTIONS




**[1] H-HOLD (horizontal hold) control**

When the picture has slanting horizontal bars, rotate the H-HOLD control in either direction until a stationary picture is obtained.

**[2] V-HOLD (vertical hold) control**

When the picture rolls up or down on the screen, adjust V-HOLD control until there is a single steady picture.

**[3] POWER switch**

To turn the monitor power on, press once and to turn the power off, press once again.

**[4] CONTRAST control**

Turn clockwise to increase picture contrast and counterclockwise to decrease it.

**[5] BRIGHT (brightness) control**

Turn clockwise for more brightness and counterclockwise for less.

**[6] 75 termination switch**

Set to 75Ω when only one monitor is used, or when the monitor is used as the last of looped chain. Set to HIGH when another monitor is connected to the VIDEO OUT connector.

**[7] VIDEO IN/OUT connector**

Connect to the video output of a VCR or another monitor (for loop-through connection), or to a video camera.

Loop-through output of the VIDEO IN connector. Connect the video input of another monitor or a VCR.

**[8] V-HEIGHT control**

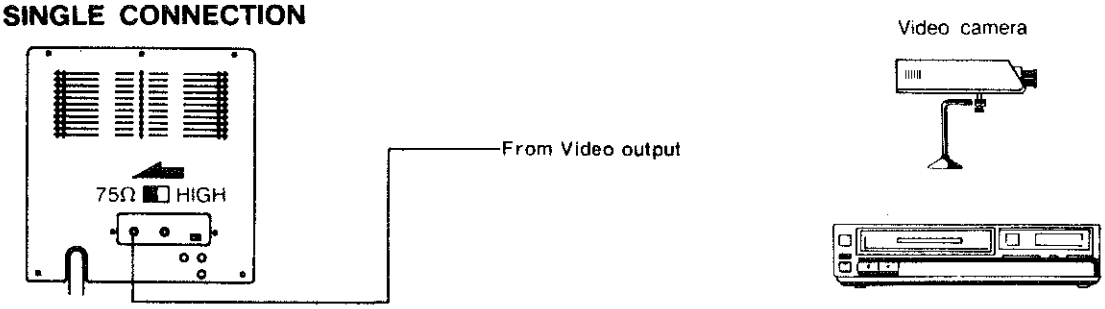
To adjust this control for the vertical size of the picture.

**[9] V-LIN control**

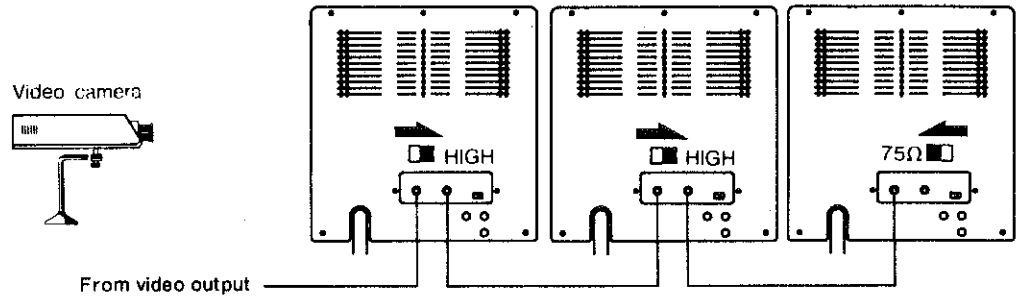
To adjust this control for the vertical linearity of the picture.

## ■ CONNCETION

### SINGLE CONNECTION




### MULTIPLE CONNECTION




Up to 3 monitors can be connected using the loop-through feature of this unit.
When this monitor is connected to additional monitors, the same picture can be obtained on all the connected monitors.

## ■ PRECAUTIONS

**Safety**

- Should any liquid or solid object fall into the cabinet, unplug the unit and have it checked by the qualified personnel before operating it any further.
- Unplug the unit from the wall outlet if it is not going to be used for several days or more. To disconnect the cord, pull it out by the plug. Never pull the cord itself.
- Allow adequate air circulation to prevent internal heat build-up. Do not place the unit on surfaces (rugs, blankets, etc.) or near materials(curtains, draperies) that may block the ventilation holes.
- Height and vertical linearity controls located at the rear panel are for special adjustments by qualified personnel only.

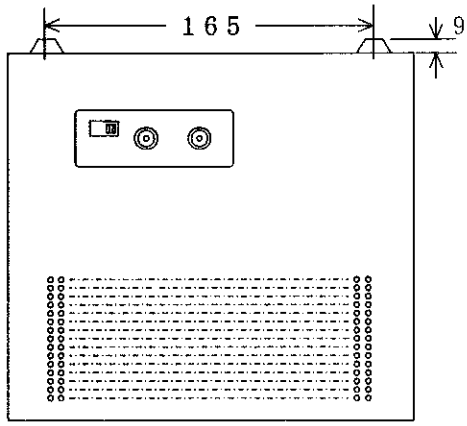
**Installation**

- Do not install the unit in an extremely hot or humid place or in a place subject to excessive dust or mechanical vibration.
- The unit is not designed to be waterproof. Exposure to rain or water may damage the unit.

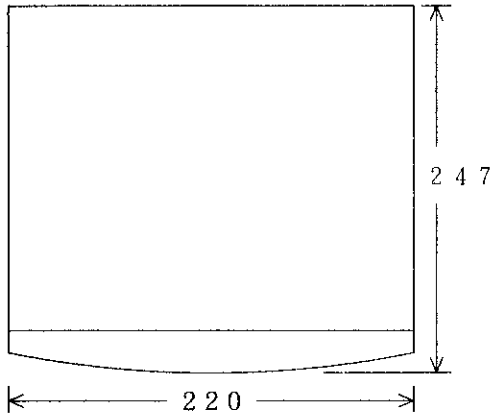
**Cleaning**

- Clean the unit with a slightly damp soft cloth. Use a mild household detergent. Never use strong solvents such as thinner or benzine as they might damage the finish of the unit.

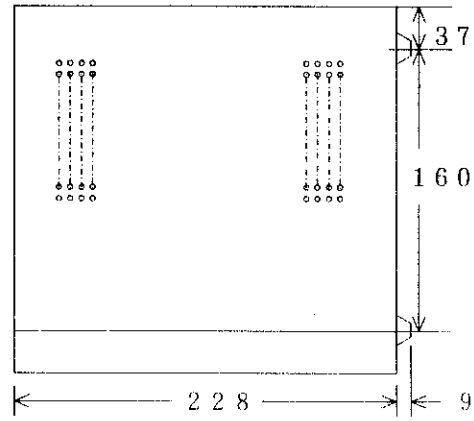
## EXTERIOR VIEW



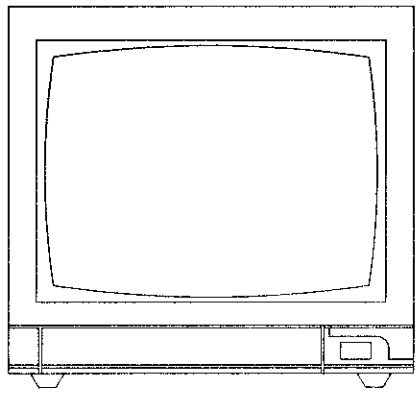

REAR




TOP




RIGHT



FRONT

DIMENSIONS mm

# LIMITED WARRANTY
## TOSHIBA VIDEO MONITOR

Toshiba America Consumer Products, Inc. ("TACP"), makes the following limited warranties. These limited warranties extend to the original end-user purchaser.

**Limited One (1) Year Warranty of Labor and Parts**
TACP warrants this product and its parts against defects in materials or workmanship for a period of one year after the date of original retail purchase. During this period, TACP will repair a defective product or part, without charge to you. You must deliver the entire product to a TACP Service Center. You pay for all transportation and insurance charges for the product to the Service Center.

**Instruction Manual (Owner's Manual)**
You should read the instruction manual (owner's manual) thoroughly before operating this product.

**Your Responsibility**
The above warranties are subject to the following conditions:
1. You must retain your bill of sale or provide other proof of purchase.
2. You must notify TACP Service within thirty (30) days after you discover a defective product or part.
3. All warranty servicing of this product must be made by TACP Service Center.
4. These warranties are effective only if the product is purchased and operated in the U.S.A.
5. Labor service charges for installation and adjustment of customer controls are not covered by this warranty.
6. Warranties extend only to defects in materials or workmanship as limited above and do not extend to any product or parts which have been lost or discarded by you or to damage to products or parts caused by misuse, accident, improper installation, improper maintenance or use in violation of instructions furnished by us; or to units which have been altered or modified without authorization of TACP or to damage to products or parts thereof which have had the serial number removed, altered, defaced or rendered illegible.

**Step-By-Step Procedures — How to Obtain Warranty Service**
To obtain warranty servicing, you should:
1. Contact TACP Service Center listed below for warranty service within thirty (30) days after you find a defective product or part.
2. Arrange for the delivery of the product to TACP Service Center. Products shipped to the Service Center must be insured and safely and securely packed, preferably in the original shipping carton, and a letter explaining the defect and also a copy of the bill of sale or other proof of purchase must be enclosed. All transportation and insurance charges must be prepaid by you.
3. If you have any questions about service, please contact the following TACP Service Center:

**EAST**
82 Totowa Road, Wayne,
NJ 07470
Phone Number: (201) 628-8000

**WEST**
19500 South Vermont Ave.
Torrance, CA 90502
Phone Number: (213) 538-9960
(213) 770-3300

**SOUTHEAST/SOUTHWEST**
1401 Valwood Parkway,
Carrollton, TX 75006
Phone Number: (214) 484-5808

**MIDWEST**
1010 Johnson Drive,
Buffalo Grove, IL 60089
Phone Number: (708) 541-9400

**ALL WARRANTIES IMPLIED BY STATE LAW, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, ARE EXPRESSLY LIMITED TO THE DURATION OF THE LIMITED WARRANTIES SET FORTH ABOVE.** Some states do not allow limitations on how long an implied warranty lasts, so the above limitation may not apply to you. **WITH THE EXCEPTION OF ANY WARRANTIES IMPLIED BY STATE LAW AS HEREBY LIMITED, THE FOREGOING EXPRESS WARRANTY IS EXCLUSIVE AND IN LIEU OF ALL OTHER WARRANTIES, GUARANTEES, AGREEMENTS AND SIMILAR OBLIGATIONS OF MANUFACTURER OR SELLER WITH RESPECT TO THE REPAIR OR REPLACEMENT OF ANY PRODUCT OR PARTS.**
**IN NO EVENT SHALL TACP BE LIABLE FOR CONSEQUENTIAL OR INCIDENTAL DAMAGES.** Some states do not allow the exclusion or limitation of incidental or consequential damages so the above limitation may not apply to you.

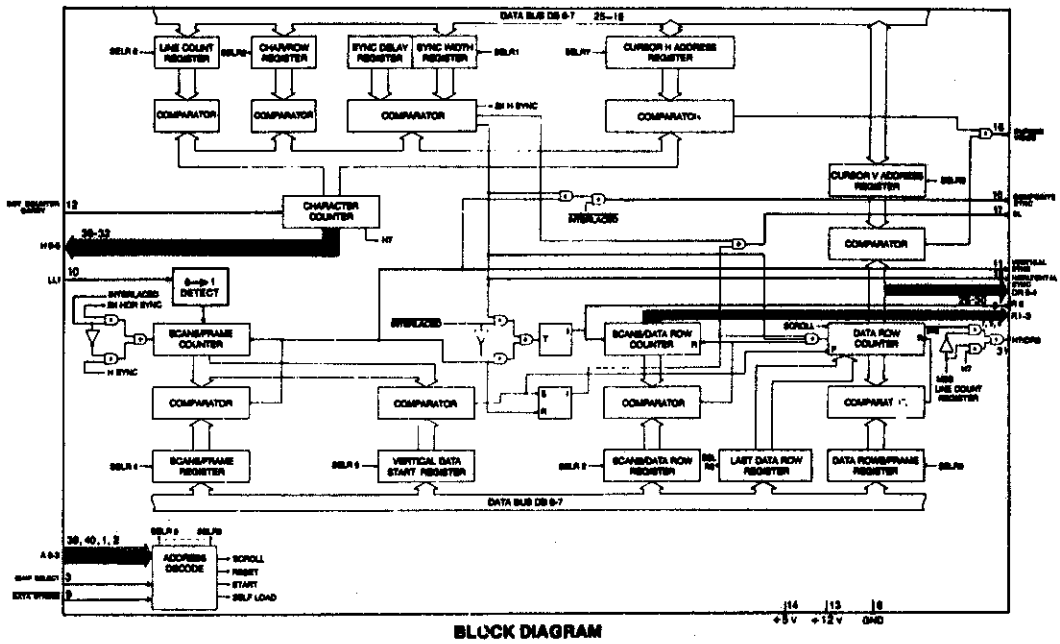
No person, agent, distributor, dealer, service station or company is authorized to change, modify or extend the terms of these warranties in any manner whatsoever. The time within which an action must be commenced to enforce any obligation of TACP arising under this warranty or under any statute, or law of the United States or any state thereof, is hereby limited to one year from the date you discover or should have discovered, the defect. This limitation does not apply to implied warranties arising under state law. Some states do not permit limitation of the time within which you may bring an action beyond the limits provided by state law so the above provision may not apply to you. This warranty gives you specific legal rights and you may also have other rights which vary from state to state.

**TOSHIBA AMERICA CONSUMER PRODUCTS, INC.**

**TOSHIBA**

## Description of Pin Functions

| Pin No. | Symbol | Name | Input/ Output | Function |
|---|---|---|---|---|
| 25-18 | DBØ-7 | Data Bus | I/O | Data bus. Input bus for control words from microprocessor or PROM. Bidirectional bus for cursor address. |
| 3 | CS | Chip Select | I | Signals chip that it is being addressed |
| 39,40,1,2 | AØ-3 | Register Address | I | Register address bits for selecting one of seven control registers or either of the cursor address registers |
| 9 | $\overline{DS}$ | Data Strobe | I | Strobes DBØ-7 into the appropriate register or outputs the cursor character address or cursor line address onto the data bus |
| 12 | DCC | DOT Counter Carry | I | Carry from off chip dot counter establishing basic character clock rate. Character clock. |
| 38-32 | HØ-6 | Character Counter Outputs | O | Character counter outputs. |
| 7, 5, 4 | R1-3 | Scan Counter Outputs | O | Three most significant bits of the Scan Counter; row select inputs to character generator. |
| 31 | H7/DR5 | H7/DR5 | O | Pin definition is user programmable. Output is MSB of Character Counter if horizontal line count (REG.Ø) is ≥128; otherwise output is MSB of Data Row Counter. |
| 8 | RØ | Scan Counter LSB | O | Least significant bit of the scan counter. In the interlaced mode with an even number of scans per data row, RØ will toggle at the field rate; for an odd number of scans per data row in the interlaced mode, RØ will toggle at the data row rate. |
| 26-30 | DRØ-4 | Data Row Counter Outputs | O | Data Row counter outputs. |
| 17 | BL | Blank | O | Defines non active portion of horizontal and vertical scans. |
| 15 | HSYN | Horizontal Sync | O | Initiates horizontal retrace. |
| 11 | VSYN | Vertical Sync | O | Initiates vertical retrace. |
| 10 | CSYN/ LLI | Composite Sync Output/ Line Lock Input | O/I | Composite sync is provided on the CRT 5027 and CRT 5037. This output is active in non-interlaced mode only. Provides a true RS-170 composite sync wave form. For the CRT 5057, this pin is the Line Lock Input. The line frequency waveform, processed to conform to the VTAC's® specified logic levels, is applied to this pin. |
| 16 | CRV | Cursor Video | O | Defines cursor location in data field. |
| 14 | Vcc | Power Supply | PS | +5 volt Power Supply |
| 13 | VDD | Power Supply | PS | +12 volt Power Supply |




**BLOCK DIAGRAM**

# 8251A
# PROGRAMMABLE COMMUNICATION INTERFACE

- Synchronous and Asynchronous Operation
- Synchronous 5–8 Bit Characters; Internal or External Character Synchronization; Automatic Sync Insertion
- Asynchronous 5–8 Bit Characters; Clock Rate—1, 16 or 64 Times Baud Rate; Break Character Generation; 1, 1½, or 2 Stop Bits; False Start Bit Detection; Automatic Break Detect and Handling
- Synchronous Baud Rate—DC to 64K Baud
- Asynchronous Baud Rate—DC to 19.2K Baud
- Full-Duplex, Double-Buffered Transmitter and Receiver
- Error Detection—Parity, Overrun and Framing
- Compatible with an Extended Range of Intel Microprocessors
- 28-Pin DIP Package
- All Inputs and Outputs are TTL Compatible
- Single +5V Supply
- Single TTL Clock

The Intel® 8251A is the enhanced version of the industry standard, Intel 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART), designed for data communications with Intel's microprocessor families such as MCS-48, 80, 85, and iAPX-86, 88. The 8251A is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM "bi-sync"). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPTY. The chip is fabricated using N-channel silicon gate technology.

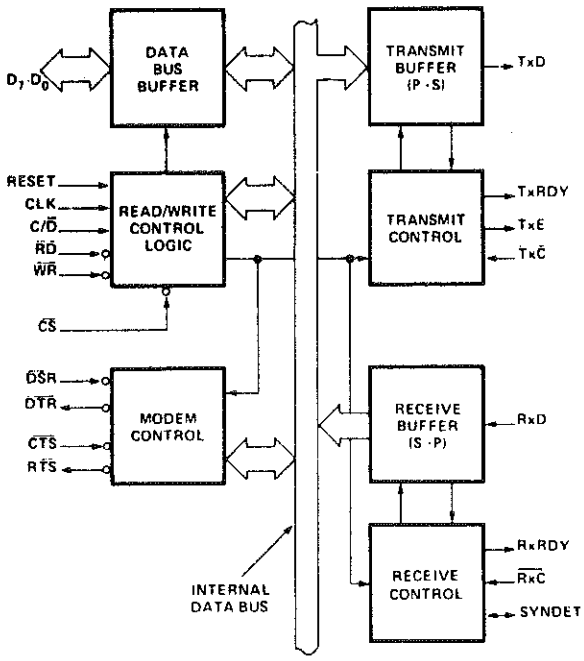



Figure 1. Block Diagram

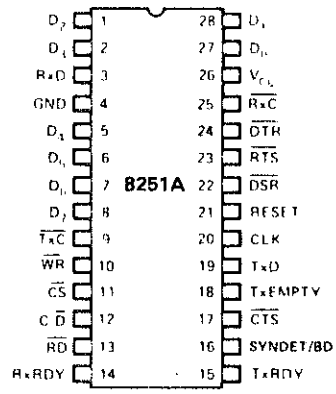



Figure 2. Pin Configuration

*INTEL CORPORATION, 1981

## FEATURES AND ENHANCEMENTS

The 8251A is an advanced design of the industry standard USART, the Intel® 8251. The 8251A operates with an extended range of Intel microprocessors and maintains compatibility with the 8251. Familiarization time is minimal because of compatibility and involves only knowing the additional features and enhancements, and reviewing the AC and DC specifications of the 8251A.

The 8251A incorporates all the key features of the 8251 and has the following additional features and enhancements:

- 8251A has double-buffered data paths with separate I/O registers for control, status, Data In, and Data Out, which considerably simplifies control programming and minimizes CPU overhead.
- In asynchronous operations, the Receiver detects and handles "break" automatically, relieving the CPU of this task.
- A refined Rx initialization prevents the Receiver from starting when in "break" state, preventing unwanted interrupts from a disconnected USART.
- At the conclusion of a transmission, TxD line will always return to the marking state unless SBRK is programmed.
- Tx Enable logic enhancement prevents a Tx Disable command from halting transmission until all data previously written has been transmitted. The logic also prevents the transmitter from turning off in the middle of a word.
- When External Sync Detect is programmed, Internal Sync Detect is disabled, and an External Sync Detect status is provided via a flip-flop which clears itself upon a status read.
- Possibility of false sync detect is minimized by ensuring that if double character sync is programmed, the characters be contiguously detected and also by clearing the Rx register to all ones whenever Enter Hunt command is issued in Sync mode.
- As long as the 8251A is not selected, the $\overline{RD}$ and $\overline{WR}$ do not affect the internal operation of the device.
- The 8251A Status can be read at any time but the status update will be inhibited during status read.
- The 8251A is free from extraneous glitches and has enhanced AC and DC characteristics, providing higher speed and better operating margins.
- Synchronous Baud rate from DC to 64K.

## FUNCTIONAL DESCRIPTION

### General

The 8251A is a Universal Synchronous/Asynchronous Receiver/Transmitter designed for a wide range of Intel microcomputers such as 8048, 8080, 8085, 8086 and 8088. Like other I/O devices in a microcomputer system, its functional configuration is programmed by the system's software for maximum flexibility. The 8251A can support most serial data techniques in use, including IBM "bi-sync."

In a communication environment an interface device must convert parallel format system data into serial format for transmission and convert incoming serial format data into parallel system data for reception. The interface device must also delete or insert bits or characters that are functionally unique to the communication technique. In essence, the interface should appear "transparent" to the CPU, a simple input or output of byte-oriented system data.

### Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the 8251A to the system Data Bus. Data is transmitted or received by the buffer upon execution of INput or OUTput instructions of the CPU. Control words, Command words and Status information are also transferred through the Data Bus Buffer. The Command Status, Data-In and Data-Out registers are separate, 8-bit registers communicating with the system bus through the Data Bus Buffer.

This functional block accepts inputs from the system Control bus and generates control signals for overall device operation. It contains the Control Word Register and Command Word Register that store the various control formats for the device functional definition.

### RESET (Reset)

A "high" on this input forces the 8251A into an "Idle" mode. The device will remain at "Idle" until a new set of control words is written into the 8251A to program its functional definition. Minimum RESET pulse width is 6 $t_{CY}$ (clock must be running).

A command reset operation also puts the device into the "Idle" state.

# Z80® CPU Central Processing Unit

Zilog

## Product Specification

**Features**

- The instruction set contains 158 instructions. The 78 instructions of the 8080A are included as a subset; 8080A software compatibility is maintained.
- Six MHz, 4 MHz and 2.5 MHz clocks for the Z80B, Z80A, and Z80 CPU result in rapid instruction execution with consequent high data throughput.
- The extensive instruction set includes string, bit, byte, and word operations. Block searches and block transfers together with indexed and relative addressing result in the most powerful data handling capabilities in the microcomputer industry.
- The Z80 microprocessors and associated family of peripheral controllers are linked by a vectored interrupt system. This system may be daisy-chained to allow implementation of a priority interrupt scheme. Little, if any, additional logic is required for daisy-chaining.
- Duplicate sets of both general-purpose and flag registers are provided, easing the design and operation of system software through single-context switching, background-foreground programming, and single-level interrupt processing. In addition, two 16-bit index registers facilitate program processing of tables and arrays.
- There are three modes of high speed interrupt processing: 8080 compatible, non-Z80 peripheral device, and Z80 Family peripheral with or without daisy chain.
- On-chip dynamic memory refresh counter.

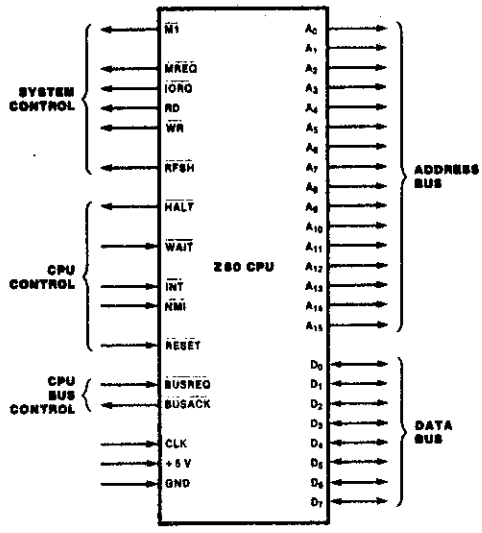



Figure 1. Pin Functions

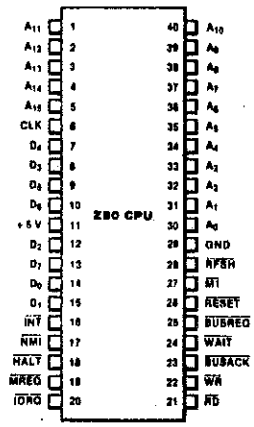



Figure 2. Pin Assignments

## General Description

The Z80, Z80A, and Z80B CPUs are third-generation single-chip microprocessors with exceptional computational power. They offer higher system throughput and more efficient memory utilization than comparable second- and third-generation microprocessors. The internal registers contain 208 bits of read/write memory that are accessible to the programmer. These registers include two sets of six general-purpose registers which may be used individually as either 8-bit registers or as 16-bit register pairs. In addition, there are two sets of accumulator and flag registers. A group of "Exchange" instructions makes either set of main or alternate registers accessible to the programmer. The alternate set allows operation in foreground-background mode or it may be reserved for very fast interrupt response.

The Z80 also contains a Stack Pointer, Program Counter, two index registers, a Refresh register (counter), and an Interrupt register. The CPU is easy to incorporate into a system since it requires only a single +5 V power source, all output signals are fully decoded and timed to control standard memory or peripheral circuits, and is supported by an extensive family of peripheral controllers. The internal block diagram (Figure 3) shows the primary functions of the Z80 processors. Subsequent text provides more detail on the Z80 I/O controller family, registers, instruction set, interrupts and daisy chaining, and CPU timing.

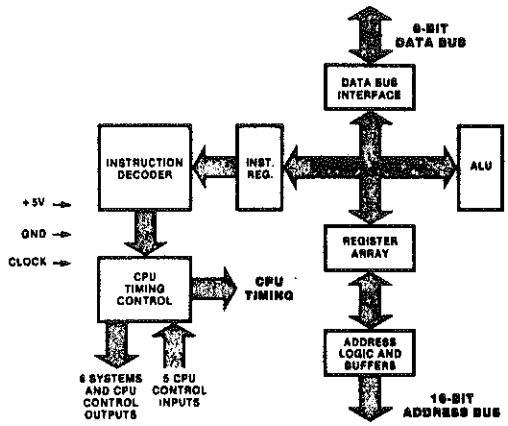


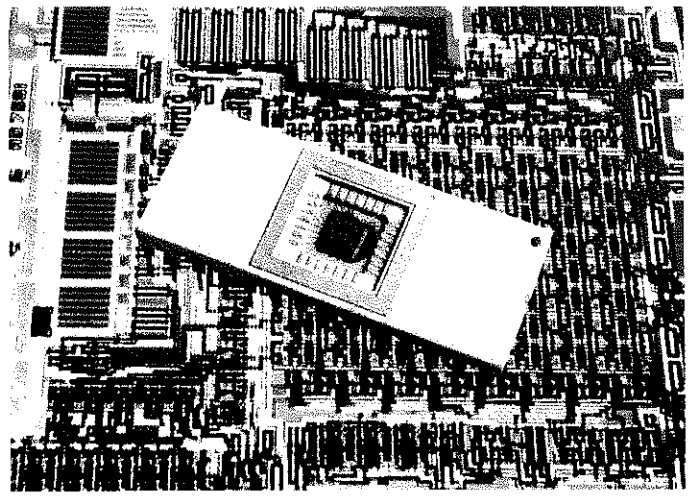

**Figure 3. Z80 CPU Block Diagram**

# ANALOG DEVICES

# CMOS µP Compatible 8-Bit 8-Channel DAS

AD7581

**FEATURES**
- 8-Bit Resolution
- On-Chip 8 X 8 Dual-Port Memory
- No Missed Codes Over Full Temperature Range
- Interfaces Directly to Z80/8085/6800
- CMOS, TTL Compatible Digital Inputs
- Three-State Data Drivers
- Ratiometric Capability
- Single +5V Supply
- Interleaved DMA Operation
- Fast Conversion
- A/D Process Totally Transparent to µP
- Low Cost

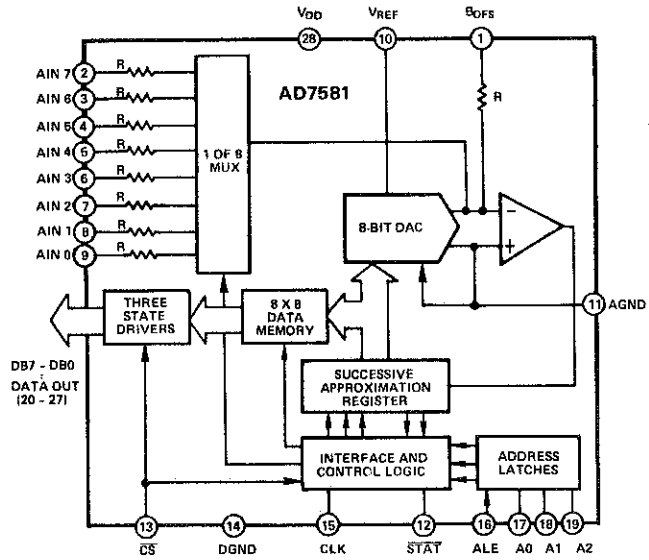


## GENERAL DESCRIPTION

The AD7581 is a microprocessor compatible 8 bit, 8 channel, memory buffered, data-acquisition system on a monolithic CMOS chip. It consists of an 8 bit successive approximation A/D converter, an 8 channel multiplexer, 8 X 8 dual-port RAM, three-state DATA drivers (for interface), address latches and microprocessor compatible control logic. The device interfaces directly to 8080, 8085, Z80, 6800 and other microprocessor systems.

The successive approximation conversion takes place on a continuous, channel sequencing, basis using microprocessor control signals for the clock. Data is automatically transferred to its proper location in the 8 X 8 dual-port RAM at the end of each conversion. When under microprocessor control, a READ DATA operation is allowed at any time for any channel since on-chip logic provides interleaved DMA. The facility to latch the address inputs ($A_0 - A_2$) with ALE enables the AD7581 to interface with µP systems which feature either shared or separate address and data buses.

## FUNCTIONAL DIAGRAM




## ORDERING INFORMATION

| Differential Nonlinearity | Temperature Range and Package: Plastic 0 to +70°C | Temperature Range and Package: Ceramic -25°C to +85°C |
|---|---|---|
| ±1 7/8LSB | AD7581JN | AD7581AD |
| ±7/8LSB | AD7581KN | AD7581BD |
| ±3/4LSB | AD7581LN | AD7581CD |

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 TWX: 710/394-6577
West Coast 714/842-1717 Mid-West 312/894-3300 Texas 214/231-5094

# DC SPECIFICATIONS ($V_{DD}$ = +5V, $V_{REF}$ = -10V, Unipolar Operation, unless otherwise stated)

| Parameter | Version[1] | Typical at +25°C | Limit Over Temperature | Units | Conditions/Comments |
|---|---|---|---|---|---|
| ACCURACY | | | | | |
| Resolution | All | 8 | 8 | Bits | |
| Relative Accuracy | JN, AD | ±1 7/8 | ±1 7/8 max | LSB | |
| | KN, BD | ±3/4 | ±3/4 max | LSB | |
| | LN, CD | ±1/2 | ±1/2 max | LSB | |
| Differential Nonlinearity | JN, AD | ±1 7/8 | ±1 7/8 max | LSB | |
| | KN, BD | ±7/8 | ±7/8 max | LSB | |
| | LN, CD | ±3/4 | ±3/4 max | LSB | |
| Offset Error[2] | JN, AD | 200 | 200 max | mV | Adjustable to zero, see Figure 7a. |
| | KN, BD | 80 | 80 max | mV | |
| | LN, CD | 50 | 50 max | mV | |
| Gain Error | | | | | |
| Worst Channel | JN, AD | ±3 | ±6 max | LSB | Adjustable to zero, see Figure 7a. |
| | KN, BD | ±2 | ±4 max | LSB | Gain Error is Measured After Offset |
| | LN, CD | ±1 | ±2 max | LSB | Calibration. Max Full Scale Change for Any Channel from +25°C to $T_{min}$ or $T_{max}$ is ±2LSB. |
| Gain Match Between Channels | JN, AD | 2 | 3 max | LSB | Adjustable to zero, see Figure 7a. |
| | KN, BD | 1 1/2 | 2 max | LSB | |
| | LN, CD | 1 | 1 max | LSB | |
| $B_{OFS}$ Gain Error | All | -2 1/2 | – | LSB | |
| ANALOG INPUTS | | | | | |
| Input Resistance | | | | | |
| At $V_{REF}$ (pin 10) | All | 10/20/30 | 10/20/30 | kΩ min/typ/max | |
| At $B_{OFS}$ (pin 1)[3] | All | 10/20/30 | 10/20/30 | kΩ min/typ/max | |
| At Any Analog Input (pins 2-9) | All | 10/20/30 | 10/20/30 | kΩ min/typ/max | |
| $V_{REF}$ (For Specified Performance) | All | -10 | -10 | V | ±5% |
| $V_{REF}$ Range[4] | All | -5 to -15 | -5 to -15 | V | |
| Nominal Analog Input Range | | | | | |
| Unipolar Mode | All | 0 to $+V_{REF}$, 0 to $-V_{REF}$ | 0 to $+V_{REF}$ 0 to $-V_{REF}$ | V V | See Figure 7 and 8. |
| Bipolar Mode | All | $-VB_{OFS} \leq VA_{IN} \leq \lvert V_{REF}\rvert - VB_{OFS}$ | | | See Figure 9 |
| DIGITAL INPUTS | | | | | |
| $\overline{CS}$ (pin 13), ALE (pin 16), $A_0$ - $A_2$ (pins 17-19) CLK (pin 15) | | | | | |
| $V_{INH}$ Logic HIGH Input Voltage | All | +2.2 | +2.4 min | V | |
| $V_{INL}$ Logic LOW Input Voltage | All | +0.4 | +0.8 max | V | |
| $I_{IN}$ Input Current | All | 0.01 | 1 max | μA | $V_{IN}$ = 0V, $V_{DD}$ |
| $C_{IN}$ Input Capacitance[5] | All | 4 | 5 max | pF | |
| DIGITAL OUTPUTS | | | | | |
| $\overline{STAT}$ (pin 12), $DB_7$ to $DB_0$ (pins 20-27) | | | | | |
| $V_{OH}$ Output HIGH Voltage | All | +4.8 | +4.5 min | V | $I_{SOURCE}$ = 40μA |
| $V_{OL}$ Output LOW Voltage | All | +0.4 | +0.6 max | V | $I_{SINK}$ = 1.6mA |
| $I_{LKG}$ $DB_7$ to $DB_0$ Floating State Leakage | All | 0.3 | 10 max | μA | |
| Floating State Output Capacitance ($DB_7$ - $DB_0$) | All | 5 | 10 max | pF | $V_{OUT}$ = 0V to $V_{DD}$ |
| Output Code | All | Unipolar Binary Figure 7<br>Complementary Binary Figure 8<br>Offset Binary Figure 9 | | | |
| POWER REQUIREMENTS | | | | | |
| $V_{DD}$ | All | +5 | +5 | V | |
| $I_{DD}$ - Static | All | 3 typ | 5 max | mA | |
| $I_{DD}$ - Dynamic | All | 3 typ | 8 max | mA | $f_{CLK}$ = 1MHz |

Notes:
[1] Temperature range as follows: JN, KN, LN (0 to +70°C), AD, BD, CD (-25°C to +85°C).
[2] Typical offset temperature coefficient is ±150μV/°C.
[3] $R_{BOFS}/R_{AIN}$ (0-7) mismatch causes transfer function rotation about positive full scale. The effect is an offset and a gain term when using the circuits of Figure 8a, page 6 and Figure 9a, page 7.
[4] Typical value, not guaranteed or subject to test.
[5] Guaranteed but not tested.
[6] Typical change in $B_{OFS}$ gain from +25°C to $T_{min}$ to $T_{max}$ is ±2 LSB's.

Specifications subject to change without notice.

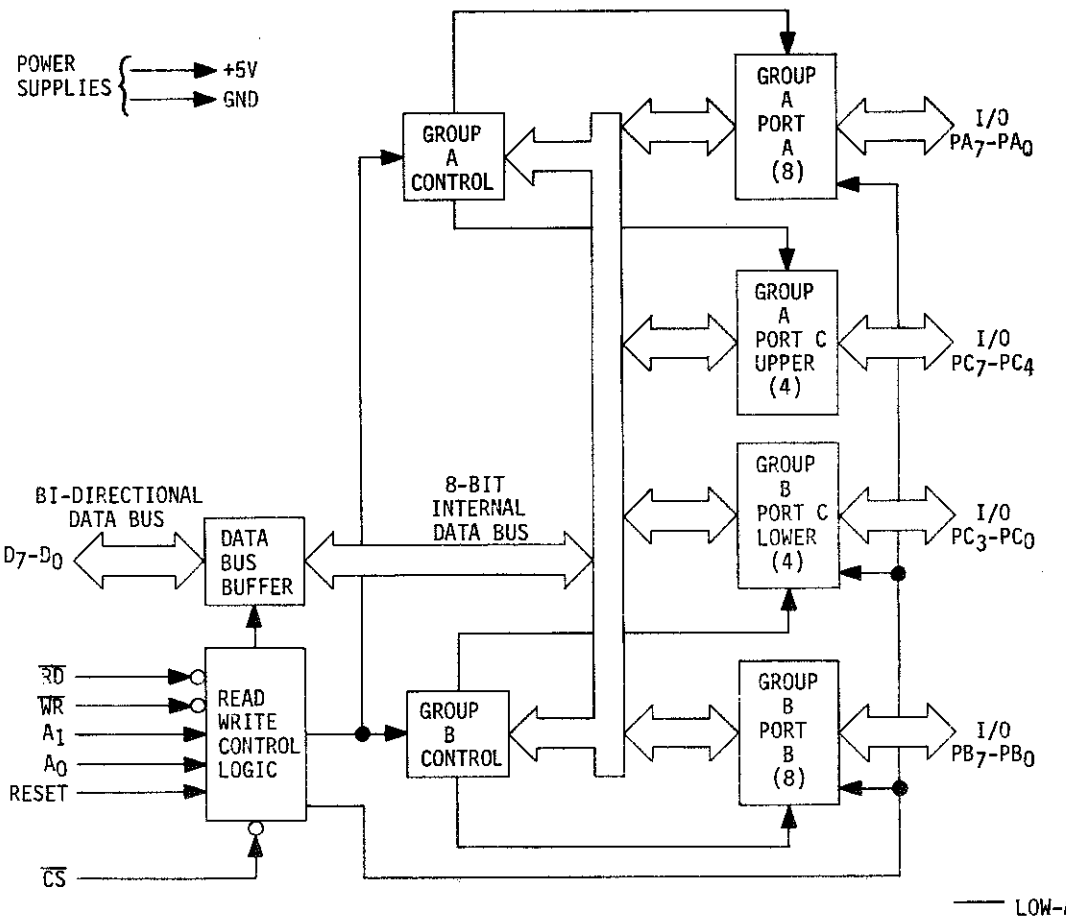



FIGURE 1. 8255A BLOCK DIAGRAM

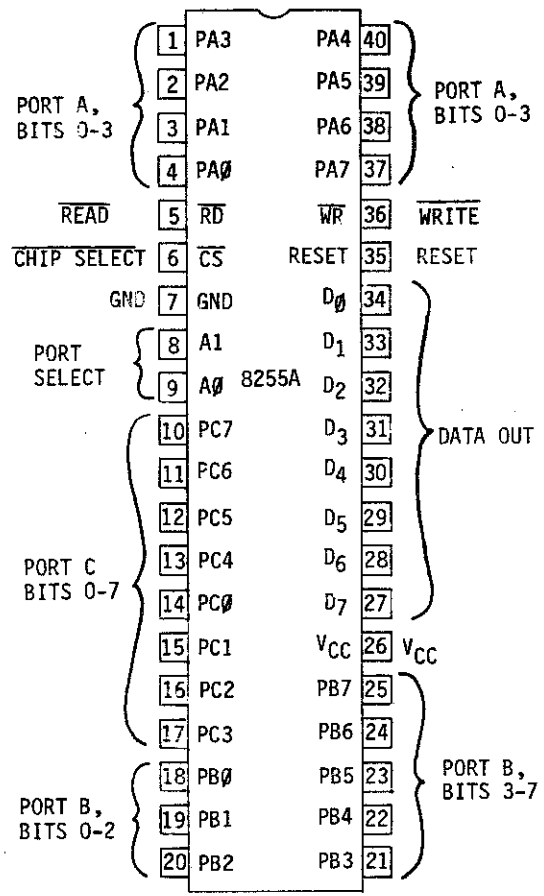



FIGURE 2. PIN CONFIGURATION

The Intel 8255A is a general purpose programmable I/O device designed for use with Intel microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

597-0036-30

**DALLAS SEMICONDUCTOR**

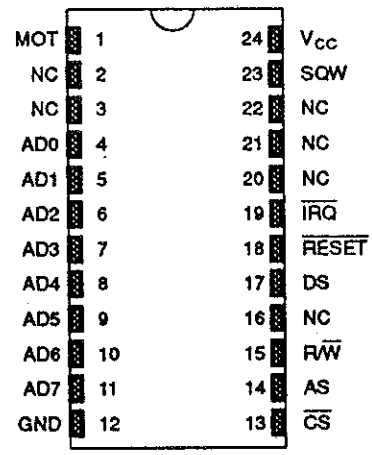
# DS1287
## Real Time Clock

6

### FEATURES

- Drop-in replacement for IBM AT computer clock/calendar
- Pin compatible with the MC146818A
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz, and support circuitry
- Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap year compensation
- Binary or BCD representation of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 64 RAM locations
  - 14 bytes of clock and control registers
  - 50 bytes of general purpose RAM
- Programmable square wave output signal
- Bus-compatible interrupt signals ($\overline{IRQ}$)
- Three interrupts are separately software-maskable and testable
  - Time-of-day alarm once/second to once/day
  - Periodic rates from 122 µs to 500 ms
  - End of clock update cycle

### PIN ASSIGNMENT




24 PIN ENCAPSULATED PACKAGE

### PIN DESCRIPTION

| | | |
|---|---|---|
| AD0–AD7 | - | Multiplexed address/data bus |
| NC | - | No connection |
| MOT | - | Bus type selection |
| $\overline{CS}$ | - | Chip select |
| AS | - | Address strobe |
| R/$\overline{W}$ | - | Read/write input |
| DS | - | Data strobe |
| $\overline{RESET}$ | - | Reset input |
| $\overline{IRQ}$ | - | Interrupt request output |
| SQW | - | Square wave output |
| $V_{CC}$ | - | +5 volt supply |
| GND | - | Ground |

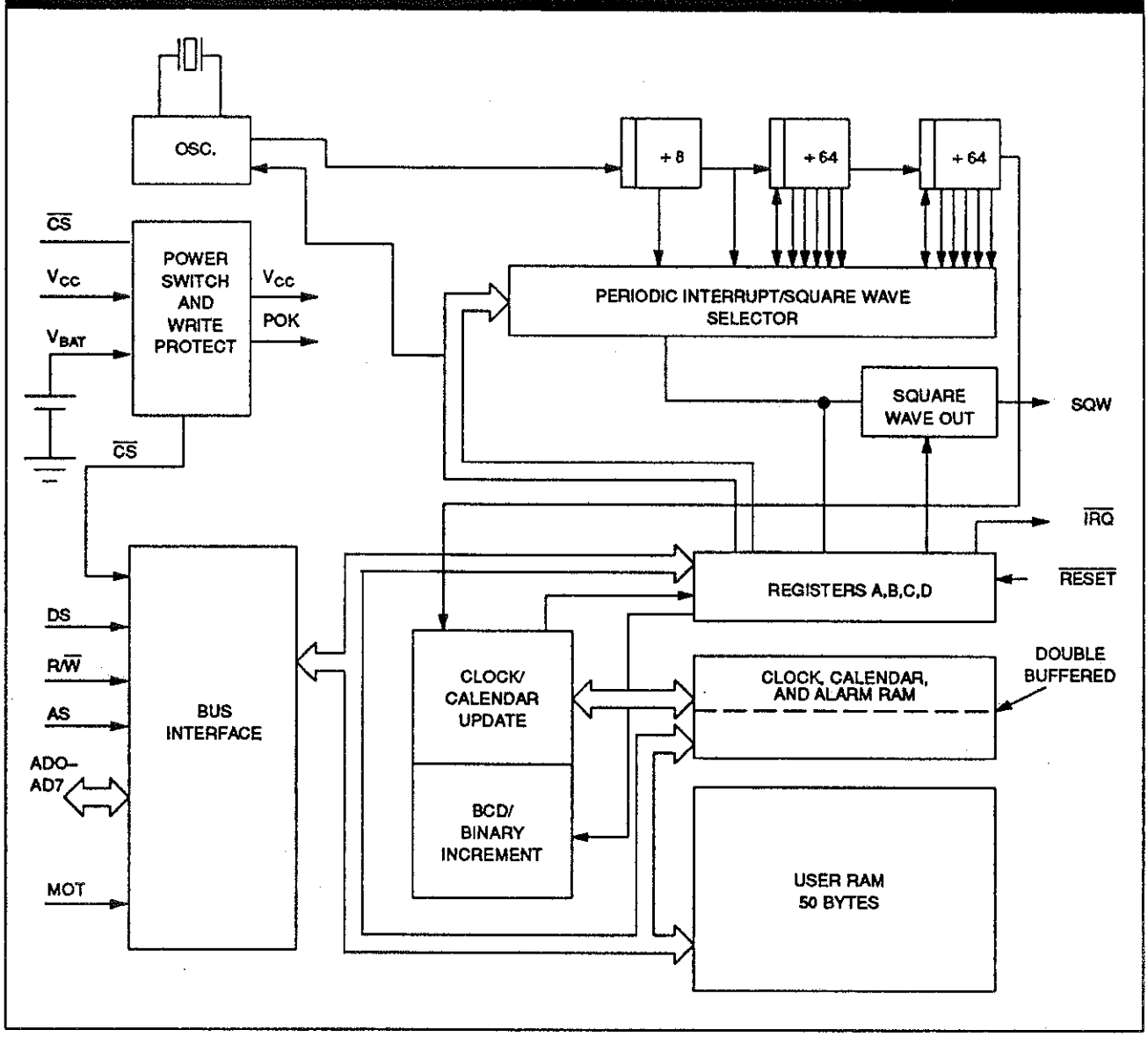
### DESCRIPTION

The DS1287 Real Time Clock is designed to be a direct replacement for the MC146818A. A lithium energy source, quartz crystal, and write-protection circuitry are contained within a 24-pin dual in-line package. As such, the DS1287 is a complete subsystem replacing 16 components in a typical application. The functions include a nonvolatile time-of-day clock, an alarm, a one-hundred-year calendar, programmable interrupt, square wave generator, and 50 bytes of nonvolatile static RAM. The real time clock is distinctive in that time-of-day and memory are maintained even in the absence of power.

## OPERATION

The block diagram in Figure 1 shows the pin connections with the major internal functions of the DS1287. The following paragraphs describe the function of each pin.

**FIGURE 1: BLOCK DIAGRAM DS1287**




## POWER-DOWN/POWER-UP CONSIDERATIONS

The Real Time Clock function will continue to operate and all of the RAM, time, calendar, and alarm memory locations remain nonvolatile regardless of the level of the $V_{CC}$ input. When $V_{CC}$ is applied to the DS1287 and reaches a level of greater than 4.25 volts, the device becomes accessible after 100 ms, provided that the oscillator is running and the oscillator countdown chain is not in reset (see Register A). This time period allows the system to stabilize after power is applied. When $V_{CC}$ falls below 4.25 volts, the chip select input is internally forced to an inactive level regardless of the value of $\overline{CS}$ at the input pin. The DS1287 is, therefore, write-protected. When the DS1287 is in a write-protected state, all inputs are ignored and all outputs are in a high impedance state. When $V_{CC}$ falls below a level of approximately 3 volts, the external $V_{CC}$ supply is switched off and an internal lithium energy source supplies power to the Real Time Clock and the RAM memory.

# TABLE OF CONTENTS


| PARAGRAPH | | PAGE NO. |
|---|---|---|
| **SECTION I** | **GENERAL INFORMATION** | |
| 1–1 | Introduction | 1–1 |
| 1–3 | Related Publications | 1–1 |
| 1–5 | System Description | 1–1 |
| 1–13 | System Configurations | 1–2 |
| 1–15 | Options and Accessories | 1–3 |
| 1–17 | System Specifications | 1–4 |
| **SECTION II** | **INSTALLATION** | |
| 2–1 | Introduction | 2–1 |
| 2–3 | Unpacking | 2–1 |
| 2–7 | Transmitter Site Installation | 2–1 |
| 2–9 | Communication Equipment Connections | 2–1 |
| 2–12 | Configuration A | 2–1 |
| 2–14 | Configuration B | 2–1 |
| 2–16 | Configuration C | 2–7 |
| 2–18 | Configuration D | 2–7 |
| 2–19 | Configuration E | 2–7 |
| 2–21 | Programming Dial–Up Modems | 2–7 |
| 2–23 | Programming 4–Wire Modems | 2–8 |
| 2–25 | Programming 2–Wire Modems | 2–9 |
| 2–27 | Memory Circuit Board Installation | 2–10 |
| 2–29 | Switch and Jumper Programming Check | 2–10 |
| 2–30 | MVDS Memory Circuit Board | 2–10 |
| 2–32 | MVDS CPU Circuit Board | 2–10 |
| 2–34 | Selecting Baud Rates | 2–10 |
| 2–35 | Communication Baud Rate | 2–10 |
| 2–37 | Local Logging Baud Rate | 2–14 |
| 2–38 | Enabling Remote Control | 2–14 |
| 2–42 | Configuration/Definition Password | 2–14 |
| 2–44 | Remote Control Password | 2–14 |
| 2–45 | Studio Site Installation | 2–15 |
| 2–46 | System Operating Program Installation | 2–15 |
| 2–48 | Computer Terminology | 2–15 |
| 2–50 | DOS | 2–15 |
| 2–51 | Keyboard | 2–15 |
| 2–52 | Floppy Disk | 2–15 |
| 2–53 | Disk Drive | 2–16 |
| 2–54 | Accessing The READ.ME File | 2–16 |
| 2–56 | Installation Requirements | 2–16 |
| 2–59 | Single Floppy Disk Drive System | 2–17 |
| 2–65 | Dual Floppy Disk Drive System | 2–18 |
| 2–71 | Floppy and Hard Disk Drive System | 2–19 |
| 2–74 | Installation Procedure | 2–20 |
| 2–119 | Initial Checkout | 2–31 |
| 2–123 | Dial–Up System | 2–32 |
| 2–124 | Direct Connect System | 2–32 |
| 2–125 | 2–Wire Modem System | 2–32 |

| PARAGRAPH | | PAGE NO. |
|---|---|---|
| 2–126 | 4–Wire Modem System | 2–32 |
| 2–127 | Studio Logging Printer Setup | 2–32 |
| **SECTION III** | **OPERATION** | |
| 3–1 | Introduction | 3–1 |
| 3–3 | Operation | 3–1 |
| 3–5 | Keyboard | 3–1 |
| 3–7 | Caps Lock Key Function | 3–1 |
| 3–8 | Contact Operations | 3–1 |
| 3–11 | Dial Operation | 3–1 |
| 3–90 | Wait Operation | 3–11 |
| 3–92 | Got Operation | 3–12 |
| 3–94 | RSALERT Screen | 3–12 |
| 3–96 | External Alarms | 3–13 |
| 3–98 | System Messages | 3–13 |
| 3–100 | TSR Programs | 3–13 |
| 3–102 | Quick Reference Guides | 3–13 |
| **SECTION IV** | **PARTS LIST** | |
| 4–1 | Introduction | 4–1 |
| **SECTION V** | **DRAWINGS** | |
| 5–1 | Introduction | 5–1 |


## LIST OF TABLES


| TABLE NO. | DESCRIPTION | PAGE NO. |
|---|---|---|
| 1–1 | System Characteristics | 1–4 |
| 1–2 | System Requirements | 1–5 |
| 3–1 | RC–1 Keyboard Commands | 3–2 |
| 3–2 | Customer Configuration Screen | 3–6 |
| 3–3 | System Messages | 3–13 |
| 4–1 | Replacement Parts List Index | 4–1 |


## LIST OF ILLUSTRATIONS


| FIGURE NO. | DESCRIPTION | PAGE NO. |
|---|---|---|
| 2–1 | Configuration A. RC–1 MVDS Remote Control Periodic or Constant Communication | 2–2 |
| 2–2 | Configuration B. RC–1 MVDS Remote Control RF Link Constant Communication | 2–3 |
| 2–3 | Configuration C. RC–1 MVDS Remote Control SCA/RF Link Constant Communication | 2–4 |
| 2–4A | Configuration D. RC–1 MVDS Remote Control Direct Connect Constant Communication | 2–5 |
| 2–4B | Configuration E. RC–1 MVDS Remote Control Leased Line Constant Communication | 2–6 |
| 2–5 | Controller Cabinet | 2–11 |
| 2–6 | 64K Memory Circuit Board Jumper Programming | 2–12 |

## LIST OF ILLUSTRATIONS (CONT'D.)


| | | |
|---|---|---|
| 2–7 | CPU Circuit Board Switch Programming | 2–12 |
| 2–8 | Input/Output Circuit Board Jumper Programming | 2–13 |
| 2–9 | Customer Configuration Screen | 2–15 |
| 2–10 | Computer Terminology | 2–16 |
| 2–11 | Installation Screen | 2–20 |
| 2–12 | Installation Screen | 2–21 |
| 2–13 | Installation Screen | 2–22 |
| 2–14 | Installation Screen | 2–22 |
| 2–15 | Installation Screen | 2–23 |
| 2–16 | Installation Screen | 2–24 |
| 2–17 | Installation Screen | 2–25 |
| 2–18 | Installation Screen | 2–26 |
| 2–19 | Installation Screen | 2–26 |
| 2–20 | Installation Screen | 2–27 |
| 2–21 | Installation Screen | 2–28 |
| 2–22 | Installation Screen | 2–28 |
| 2–23 | Installation Screen | 2–29 |
| 2–24 | Installation Screen | 2–30 |
| 3–1 | Sign–On Screen | 3–3 |
| 3–2 | Normal Display Screen | 3–4 |
| 3–3 | Customer Configuration Screen | 3–5 |
| 3–4 | RSALERT Screen | 3–12 |


## PROPRIETARY AND CONFIDENTIAL INFORMATION


This subject matter contains proprietary information of Broadcast Electronics which is to be maintained confidential, is not to be duplicated or distributed to others without written permission or used in any way detrimental to the interests of Broadcast Electronics and must be returned upon demand.


This equipment is a Class A (or Class B) digital apparatus which complies with the Radio Interference Regulations, CRC c.1374.


® HAYES is a registered trademark of Hayes Microcomputer Products, Inc.

® IBM is a registered trademark of International Business Machines.

® VEN–TEL is a registered trademark of Ven–Tel, Inc.

# SECTION I
# GENERAL INFORMATION

## 1–1. INTRODUCTION.

1–2. Information presented in this section provides a general description of the Broadcast Electronics RC–1 MVDS remote control system. System specifications and requirements are also listed in this section.

### 1–3. RELATED PUBLICATIONS.

1–4. The MVDS section of this manual provides information for equipment associated with the RC–1 remote control system.

## 1–5. SYSTEM DESCRIPTION.

1–6. The RC–1 MVDS remote control system is specifically designed to allow remote control and monitoring of any Broadcast Electronics FM transmitter equipped with a microprocessor video diagnostic system (MVDS). The remote control system consists of a modified MVDS memory circuit board and a remote control system program. Remote control and monitoring of transmitter operations and parameters can be implemented with any 100% IBM–PC compatible personal computer and a remote communications link. A second personal computer can also be used to control the transmitter if required.

1–7. Access to the transmitter MVDS is protected by a customer generated password consisting of 8 alphanumeric characters. This password must be received and recognized by the MVDS before the MVDS will establish contact with a remote site.

1–8. The RC–1 will present the MVDS customer configuration and normal display screens on the remote computer monitor. Selection of transmitter operating limits are entered into the transmitter MVDS through a computer keyboard.

1–9. Remote control of transmitter operations such as plate voltage on/off, filament voltage on/off, and raise/lower output power can only be accessed after entering a special transmitter control mode. For increased protection, a transmitter control function must be entered within a 30 second time frame.

1–10. The RC–1 will provide logging of information presented on the remote computer monitor screen. If a printer is connected to the computer, a hard copy of the MVDS configuration screen and normal display screen can be obtained. In addition, transmitter logs may be requested at the computer keyboard or provided automatically at regular intervals by system programming.

1–11. The remote control system features automatic contact of the remote site by the transmitter at regular intervals depending on system programming. If automatic contact is enabled, intervals ranging from once a day to once every three minutes may be selected. In addition, the transmitter will automatically contact the remote site in the event of a transmitter failure.

1–12. The RC–1 MVDS remote control system is designed to operate with Hayes or Hayes compatible telephone modems and telephone lines. The RC–1 will also operate with 4–wire modems and SCA or STL RF communications equipment. If the distance between the transmitter and personal computer is within 500 feet, the modems can be eliminated by utilizing an RS–232 communications link (direct connect).

## 1–13. SYSTEM CONFIGURATIONS.

1–14. The RC–1 MVDS remote control system may be ordered in the following configurations:

| MODEL NO. | PART NUMBER | DESCRIPTION |
|---|---|---|
| RC–1 | 909–0122–014 | OPTIONAL MVDS REFMOTE CONTROL SYSTEM, FACTORY INSTALLATION, FM–30B TRANSMITTER. |
| RC–1 | 909–0122–024 | OPTIONAL MVDS REMOTE CONTROL SYSTEM, FACTORY INSTALLATION, FM–3.5B TRANSMITTER. |
| RC–1 | 909–0122–034 | OPTIONAL MVDS REMOTE CONTROL SYSTEM, FACTORY INSTALLATION, FM–5B TRANSMITTER. |
| RC–1 | 909–0122–054 | OPTIONAL MVDS REMOTE CONTROL SYSTEM, FACTORY INSTALLATION, FM–10B TRANSMITTER. |
| RC–1 | 909–0122–064 | OPTIONAL MVDS REMOTE CONTROL SYSTEM, FACTORY INSTALLATION, FM–35B TRANSMITTER. |
| RC–1 | 909–0122–074 | OPTIONAL REMOTE MVDS CONTROL SYSTEM, FACTORY INSTALLATION, FM–20B TRANSMITTER. |
| RC–1 | 909–0122–094 | OPTIONAL REMOTE MVDS CONTROL SYSTEM, FACTORY INSTALLATION, FM–5BS TRANSMITTER. |

**FIELD INSTALLATION KITS**

| MODEL NO. | PART NUMBER | DESCRIPTION |
|---|---|---|
| RC–1 | 909–0128–014 | OPTIONAL MVDS REMOTE CONTROL SYSTEM, FIELD INSTALLATION KIT, FM–30B TRANSMITTER. |
| RC–1 | 909–0128–024 | OPTIONAL MVDS REMOTE CONTROL SYSTEM, FIELD INSTALLATION KIT, FM–3.5B TRANSMITTER. |
| RC–1 | 909–0128–034 | OPTIONAL MVDS REMOTE CONTROL SYSTEM, FIELD INSTALLATION KIT, FM–5B TRANSMITTER. |
| RC–1 | 909–0128–054 | OPTIONAL MVDS REMOTE CONTROL SYSTEM, FIELD INSTALLATION KIT, FM–10B TRANSMITTER. |
| RC–1 | 909–0128–064 | OPTIONAL MVDS REMOTE CONTROL SYSTEM, FIELD INSTALLATION KIT, FM–35B TRANSMITTER. |
| RC–1 | 909–0128–074 | OPTIONAL MVDS REMOTE CONTROL SYSTEM, FIELD INSTALLATION KIT, FM–20B TRANSMITTER. |
| RC–1 | 909–0128–094 | OPTIONAL MVDS REMOTE CONTROL SYSTEM, FIELD INSTALLATION KIT, FM–5BS TRANSMITTER. |

| PART NUMBER | DESCRIPTION |
|---|---|
| 979–0122–014 | KIT OF 25 EPROMS WHICH CONTAIN THE MVDS REMOTE CONTROL SOFTWARE INSTRUCTIONS FOR THE FM–30B TRANSMITTER. |
| 979–0122–024 | KIT OF 25 EPROMS WHICH CONTAIN THE MVDS REMOTE CONTROL SOFTWARE INSTRUCTIONS FOR THE FM–3.5B TRANSMITTER. |
| 979–0122–034 | KIT OF 25 EPROMS WHICH CONTAIN THE MVDS REMOTE CONTROL SOFTWARE INSTRUCTIONS FOR THE FM–5B TRANSMITTER. |
| 979–0122–054 | KIT OF 25 EPROMS WHICH CONTAIN THE MVDS REMOTE CONTROL SOFTWARE INSTRUCTIONS FOR THE FM–10B TRANSMITTER. |
| 979–0122–064 | KIT OF 25 EPROMS WHICH CONTAIN THE MVDS REMOTE CONTROL SOFTWARE INSTRUCTIONS FOR THE FM–35B TRANSMITTER. |
| 979–0122–074 | KIT OF 25 EPROMS WHICH CONTAIN THE MVDS REMOTE CONTROL SOFTWARE INSTRUCTIONS FOR THE FM–20B TRANSMITTER. |
| 979–0122–094 | KIT OF 25 EPROMS WHICH CONTAIN THE MVDS REMOTE CONTROL SOFTWARE INSTRUCTIONS FOR THE FM–5BS TRANSMITTER. |

## 1–15. OPTIONS AND ACCESSORIES.

1–16. The following is a list of the available options for the RC–1 MVDS remote control system.

| MODEL NO. | PART NUMBER | DESCRIPTION |
|---|---|---|
| MT–3 | 909–0127–004 | OPTIONAL MULTIPLE TRANSMITTER INTERFACE FOR RC–1 MVDS REMOTE CONTROL SYSTEM. |
| —— | 979–0082–004 | 100% SEMICONDUCTOR SPARE PARTS KIT, NO EPROMS. |
| —— | 979–0083–004 | RECOMMENDED SEMICONDUCTOR SPARE PARTS KIT, NO EPROMS. |
| EC202–8 | 809–4059 | VEN–TEL 4–WIRE, FULL DUPLEX MODEM, FOR REMOTE LINK USING RF EQUIPMENT. COMPATIBLE WITH BELL 202T STANDARD. |
| EC1200–1 | 809–4060 | VEN–TEL 2–WIRE, FULL DUPLEX MODEM, FOR REMOTE LINK USING LEASED TELEPHONE LINE. COMPATIBLE WITH BELL 212A STANDARD. |

## 1–17. SYSTEM SPECIFICATIONS.

1–18. Refer to Table 1–1 for the RC–1 MVDS remote control system characteristics and Table 1–2 for system requirements.

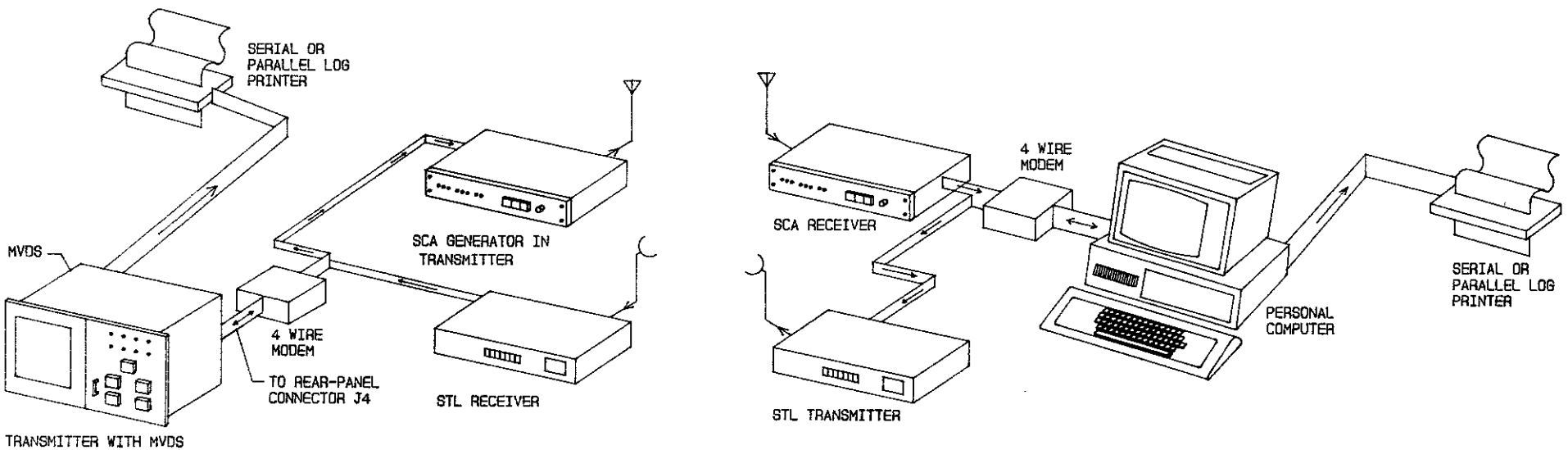
**TABLE 1–1. SYSTEM CHARACTERISTICS**

| PARAMETER | SPECIFICATIONS |
|---|---|
| COMMUNICATIONS PORT | RS–232 serial port on the transmitter controller rear–panel. |
| MEMORY: | |
| RAM | 2 K bytes volatile. General use.<br>2 K bytes non–volatile. Storage of the customer specified telephone number and configuration screen. |
| ROM | 58 K bytes. Storage of remote control system and MVDS operating programs. |
| CONTACT INITIATION: | |
| REMOTE (Studio) | Keyboard entered command line includes a customer generated 8–digit password. |
| LOCAL (Transmitter) | Automatic for the following conditions:<br>1. Transmitter overloads.<br>2. System time intervals.<br>3. Forward power increases above 105%.<br>4. External alarm activates. |
| REACTION TIME | Duration between the entry and the execution of a command is 5 seconds maximum at 1200 baud rate and 4.77 MHz computer operating frequency. |
| FAILSAFE (Constant Communications Mode – Refer to ENABLING REMOTE CONTROL in SECTION II) | RF output power is terminated if contact is not established within 3 hours or 3 minutes as previously selected at the transmitter MVDS. |
| CONTACT SEQUENCE (Periodic Mode – Refer to ENABLING REMOTE CONTROL in SECTION II) | Initiates three contact attempts at 3 minute intervals with 10 rings each. Terminates output power (defeatable) if contact is not established and forward power is greater than 105% on the third attempt. |
| COMMUNICATION ERROR DETECTION | Checksums (generated at source and destination) are compared. |

**TABLE 1–2. SYSTEM REQUIREMENTS**

| PARAMETER | SPECIFICATIONS |
|---|---|
| REMOTE SITE (Studio) | |
| COMPUTER | One 100% IBM–PC compatible personal computer with PC–DOS or MS–DOS (version 3.1 or later) and 256 K bytes minimum of RAM memory. |
| DISK DRIVE | Single 5 1/4 inch or 3 1/2 inch floppy disk drive. |
| MODEM (Determined by Application): | |
| DIAL–UP TELEPHONE LINK | Hayes or Hayes compatible modem* with the following features:<br>1. Automatic answering.<br>2. Automatic dialing.<br>3. 300 or 1200 baud rate selectable. |
| RF LINK | Ven–Tel 4–wire full duplex modem, model EC202–8 or equivalent. |
| LEASED LINE LINK | Ven–Tel 2–wire full duplex modem, model EC1200–1 or equivalent. |
| LOCAL SITE (Transmitter) | |
| MODEM (Determined by Application): | |
| DIAL–UP TELEPHONE LINK | External Hayes or Hayes compatible modem with the following features:<br>1. Automatic answering.<br>2. Automatic dialing.<br>3. 300 or 1200 baud rate selectable. |
| RF LINK | Ven–Tel 4–wire full duplex modem, model EC202–8 or equivalent. |
| LEASED LINE LINK | Ven–Tel 2–wire full duplex modem, model EC1200–1 or equivalent. |

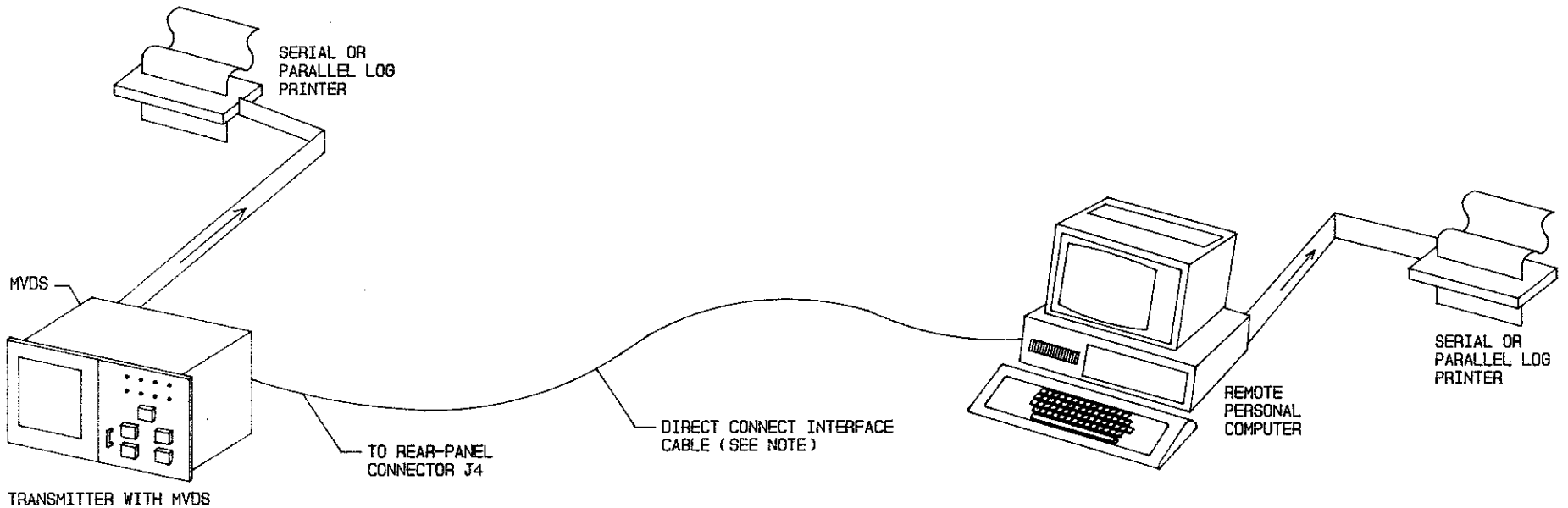
* The studio modem can be internal or external to the computer system.




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597-0122-6

**FIGURE 2-3. CONFIGURATION C.**
**RC-1 COMPUTER REMOTE CONTROL SCA/RF LINK CONSTANT COMMUNICATION**

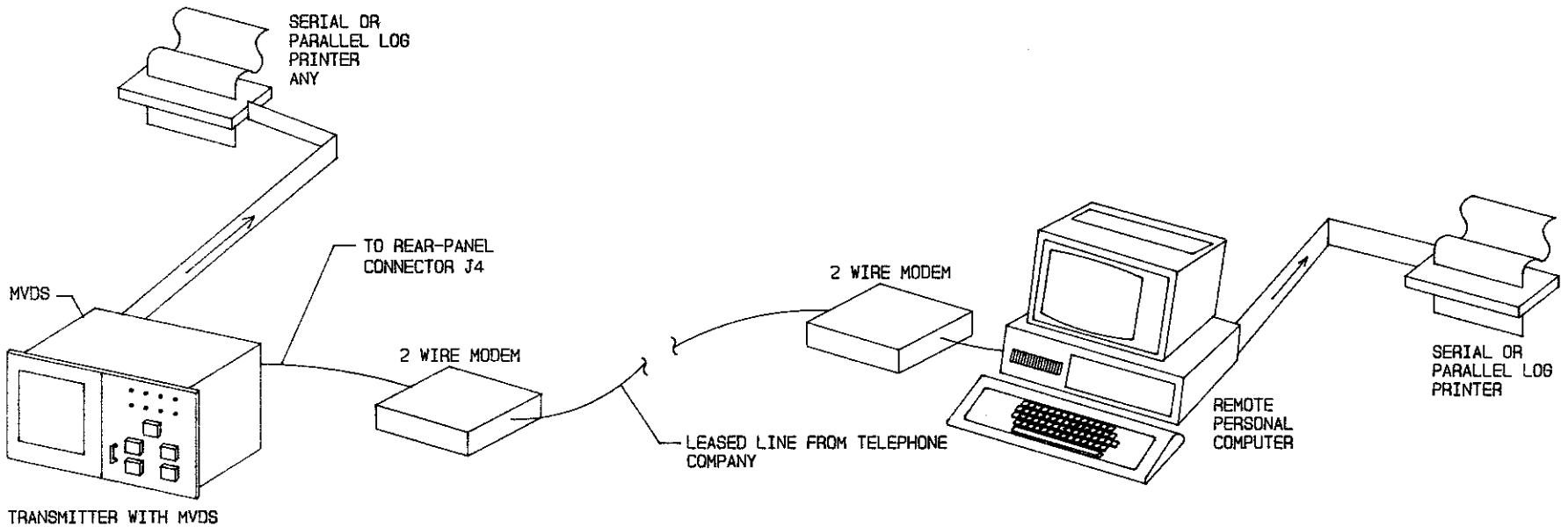



NOTE:
THE DIRECT CONNECT INTERFACE CABLE CAN BE USED WHEN THE DISTANCE BETWEEN THE MVDS AND COMPUTER IS WITHIN 500 FEET.

COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597-0122-7A

**FIGURE 2–4A. CONFIGURATION D.**
**RC–1 MVDS REMOTE CONTROL DIRECT CONNECT CONSTANT COMMUNICATION**




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597-0122-7B

**FIGURE 2-4B. CONFIGURATION E.**
**RC-1 MVDS REMOTE CONTROL LEASED LINE CONSTANT COMMUNICATION**

2–15. To install a 4–wire modem at the studio site, refer to Figure 5–7 in SECTION V, DRAWINGS and fabricate an interface cable as indicated. Connect this cable between the appropriate PC communications port and the modem.

2–16. **CONFIGURATION C.** This communication system incorporates a 4–wire modem and SCA/STL equipment installed at the transmitter and studio sites. To install a 4–wire modem at the transmitter site, refer to Figure 5–3 in SECTION V, DRAWINGS, and construct an interface cable as indicated. Connect this cable between serial port J4 on the rear–panel of the transmitter controller cabinet and the appropriate receptacle on the modem.

2–17. To install a 4–wire modem at the studio site, refer to Figure 5–7 in SECTION V, DRAWINGS and fabricate an interface cable as indicated. Connect this cable between the appropriate PC communications port and the modem.

2–18. **CONFIGURATION D.** This configuration incorporates a direct connect (RS–232) system which can be implemented when the distance between the MVDS and computer is within 500 feet. To install the direct connect system, refer to Figure 5–6 in SECTION V, DRAWINGS, and fabricate an interface cable as shown. Connect this cable between serial port J4 on the rear–panel of the transmitter controller cabinet and the appropriate receptacle on the computer system.

2–19. **CONFIGURATION E.** This configuration incorporates 2–wire modems and a leased line from a telephone company. To install a 2–wire modem at the transmitter site, refer to Figure 5–3 in SECTION V, DRAWINGS, and construct an interface cable as indicated. Connect this cable between serial port J4 on the rear–panel of the transmitter controller and the appropriate receptacle on the modem.

2–20. To install a modem at the studio site, refer to Figure 5–7 in SECTION V, DRAWINGS, and construct an interface cable as indicated. Connect this cable between the appropriate PC communications port and the modem.

2–21. **PROGRAMMING DIAL-UP MODEMS.**

2–22. If dial–up modems are selected for the communication system between the local and remote sites, Hayes or Hayes compatible equipment must be implemented. The modem configuration switches must be programmed to operate with the remote control system software. To program the modems, refer to the manufacturers instruction manual and the following information.

**TRANSMITTER SITE MODEM FOR DIAL–UP TELEPHONE LINK**

| PARAMETER | CONDITION |
|---|---|
| 1. Data terminal ready (DTR) | True |
| 2. Result code type | Not applicable |
| 3. Result code | No result code |
| 4. Echo command code | No echo |
| 5. Automatic answer | Enabled |
| 6. Carrier detect | True carrier |
| 7. Telephone line type | Single or multiple (as required) |
| 8. Modem command recognition | Enabled |

2–22. In addition to the programming information presented in the preceding text, the modem must be: 1) programmed with a specific configuration code and 2) the configuration code stored in profile 0. The following text presents the configuration code to be used. Refer to the modem instruction manual and program the modem with the following code. If the code does not work with the modem, contact the Broadcast Electronics Customer Service Department.

**AT F*n* &W0**

**F*n*** = F4 – 1200 bps
F5 – 2400 bps
F6 – 4800 bps
F7 – 7200 bps
F8 – 9600 bps

**W0** = Save the configuration code in profile 0.

**STUDIO SITE MODEM**
**FOR DIAL–UP TELEPHONE LINK**

| | PARAMETER | CONDITION |
|---|---|---|
| 1. | Data terminal ready (DTR) | Not applicable |
| 2. | Result code type | Not applicable |
| 3. | Result code | Enabled |
| 4. | Echo command code | No echo |
| 5. | Automatic answer | Enabled |
| 6. | Carrier detect | True carrier |
| 7. | Telephone line type | Single or multiple (as required) |
| 8. | Modem command recognition | Enabled |

## 2–23. PROGRAMMING 4–WIRE MODEMS.

2–24. If 4–wire modems are selected for the communications system, the modem configuration switches must be programmed to operate with the remote control system software. To program the modems, refer to the manufacturers instruction manual and the following information.

**TRANSMITTER SITE 4–WIRE FULL DUPLEX**
**FOR RF COMMUNICATIONS LINK**

| | PARAMETER | CONDITION |
|---|---|---|
| 1. | Test switch(es) | Disabled |
| 2. | Signal ground and chassis ground | Common |
| 3. | Data terminal ready (DTR) | Enabled |
| 4. | Local echo | Disabled |
| 5. | Carrier detect response | Not applicable |
| 6. | Receiver squelch | Disabled |
| 7. | Turn around delay | Not applicable |
| 8. | Soft carrier turn–off | Disabled |
| 9. | Requests to send (RTS) delay | N/A |
| 10. | Clear to send (CTS) delay | N/A |
| 11. | 2–wire/4–wire configuration | 4–wire |
| 12. | Constant carrier | Enabled |
| 13. | Receiver sensitivity level | Adjust as required |

| | |
|---|---|
| 14. Transmit level | Adjust as required |
| 15. Baud rate | 1200 bps |

**STUDIO SITE 4–WIRE FULL DUPLEX FOR RF COMMUNICATIONS LINK**

| PARAMETER | CONDITION |
|---|---|
| 1. Test switch(es) | Disabled |
| 2. Signal ground and chassis ground | Common |
| 3. Data terminal ready (DTR) | Disabled |
| 4. Local echo | Disabled |
| 5. Carrier detect response | Not applicable |
| 6. Receiver squelch | Disabled |
| 7. Turn around delay | Not applicable |
| 8. Soft carrier turn–off | Disabled |
| 9. Requests to send (RTS) delay | N/A |
| 10. Clear to send (CTS) delay | N/A |
| 11. 2–wire/4–wire configuration | 4–wire |
| 12. Constant carrier | Enabled |
| 13. Receiver sensitivity level | Adjust as required |
| 14. Transmit level | Adjust as required |
| 15. Baud rate | 1200 bps |

## 2–25. PROGRAMMING 2–WIRE MODEMS.

2–26. If 2–wire modems are selected for the communications system, the modem configuration switches must be programmed to operate with the remote control system software. To program the modems, refer to the manufacturers instruction manual and the following information.

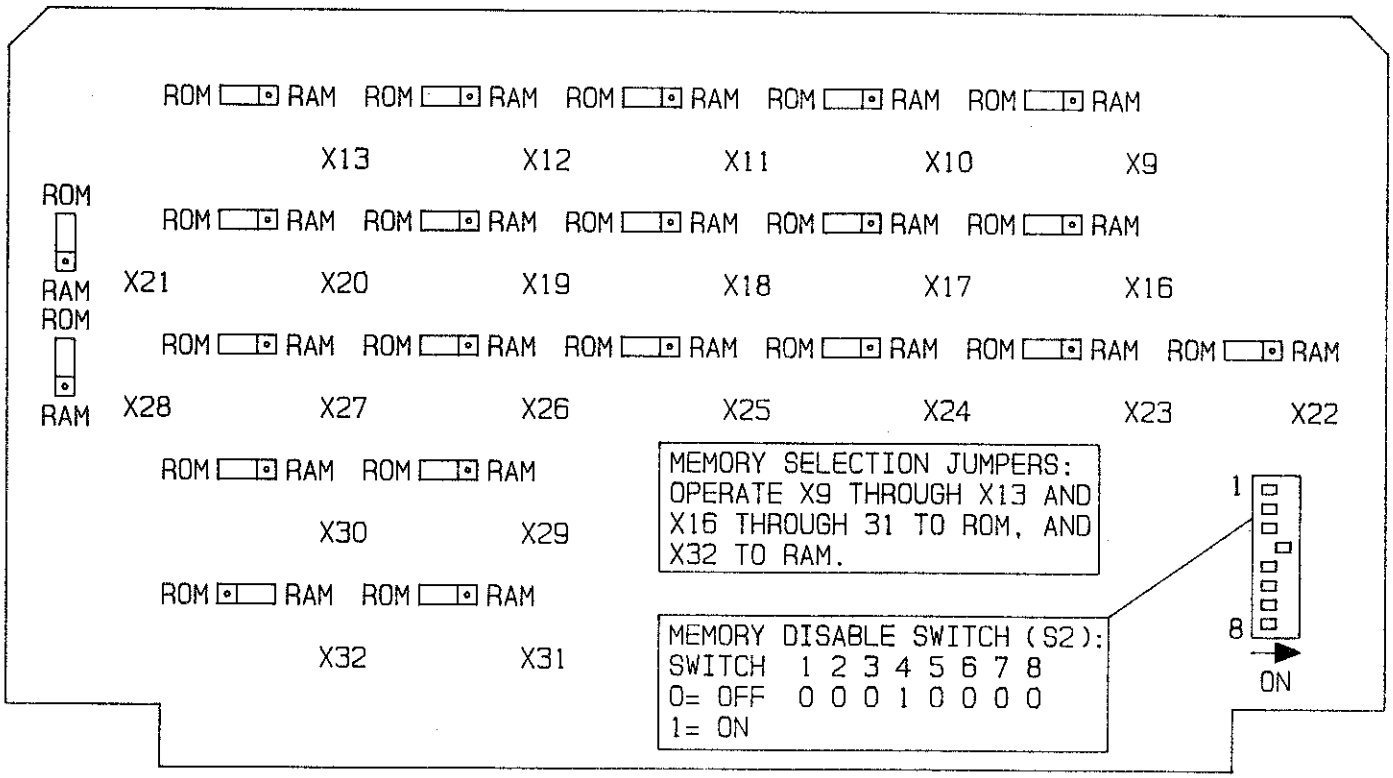
***NOTE***

***NOTE***

***THE TRANSMITTER SITE MODEM MUST BE OPERATED IN THE ANSWER MODE.***

**TRANSMITTER SITE 2–WIRE FULL DUPLEX FOR LEASED LINE LINK**

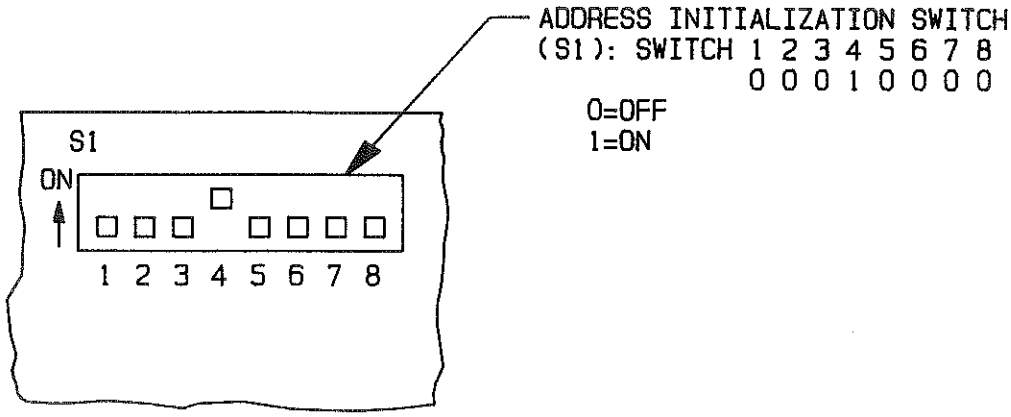
| PARAMETER | CONDITION |
|---|---|
| 1. Test switch(es) | Disabled |
| 2. Signal ground and chassis ground | Common |
| 3. Data terminal ready (DTR) | Enabled |
| 4. Initiate analog loopback test | Disabled |
| 5. Character length | 10 bits |
| 6. Leased line/dial–up | Leased line |
| 7. Synchronous/asynchronous | Asynchronous |
| 8. Answer on ring detect | Disabled |
| 9. Ring indication | Not applicable |
| 10. 2–wire/4–wire configuration | 2–wire |
| 11. Baud Rate | 1200 bps |
| 12. Forced answer/voice answer/data | Voice/answer |




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

**597-0122-1**

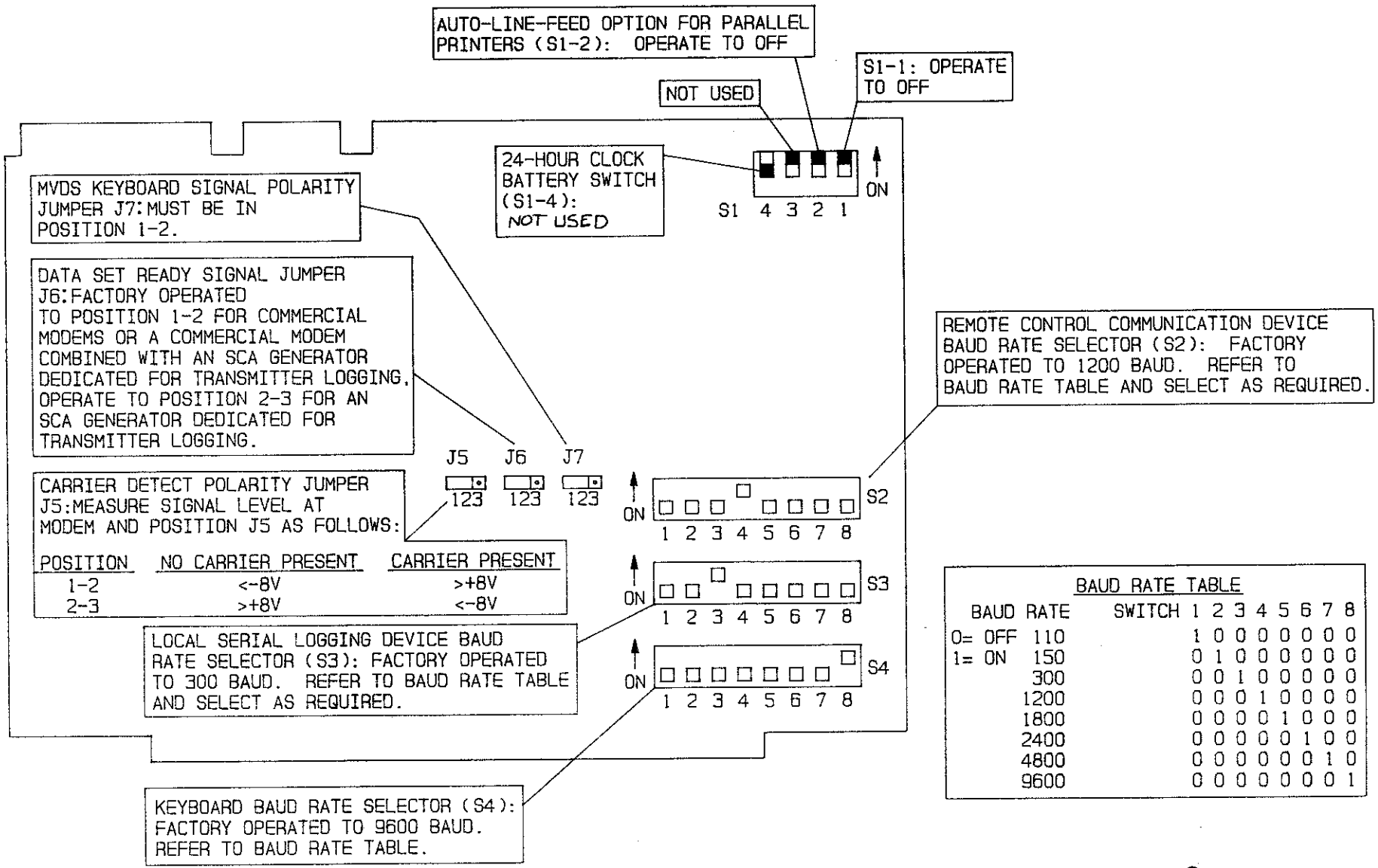
**FIGURE 2–6. 64K MEMORY CIRCUIT BOARD JUMPER PROGRAMMING**




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

**597-0122-2**

**FIGURE 2–7. CPU CIRCUIT BOARD SWITCH PROGRAMMING**




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597-0122-3

**FIGURE 2-8. INPUT/OUTPUT CIRCUIT BOARD JUMPER PROGRAMMING**

2–36. Switch S2 must be operated to 9600 baud when an MT–3 multiple transmitter interface is connected to the MVDS. S2 is factory operated to 1200 baud prior to shipping. If an alternate baud rate is required, refer to the following information and Figure 2–8 and select the appropriate baud rate.

| APPLICATION | BAUD RATE |
|---|---|
| Dial–Up Modem | 300 to 9600 (Modem dependent) |
| RS–232 Direct Connect | 110 to 9600 |
| 4–Wire Modem/RF Link | 1200 |
| 2–Wire Modem/Leased Line | 1200 |

2–37. **LOCAL LOGGING BAUD RATE.** Switch S3 on the input/output circuit board selects the baud rate for a serial logging device at the transmitter site. Switch S3 is factory operated to 300 baud prior to shipping. If an alternate baud rate is required, refer to Figure 2–8 and select the appropriate baud rate.

2–38. **ENABLING REMOTE CONTROL.**

2–39. The transmitter MVDS must be instructed to accept remote control operations. Refer to Figure 2–9 and advance the cursor to the MVDS REMOTE CONTROL field using the ⇓ key.

2–40. The RC–1 can be operated in a periodic mode or a constant mode. When operated in the periodic mode, the transmitter MVDS will contact the studio by dialing. When operated in the constant mode, contact is permanently established; therefore, the dialing process is eliminated.

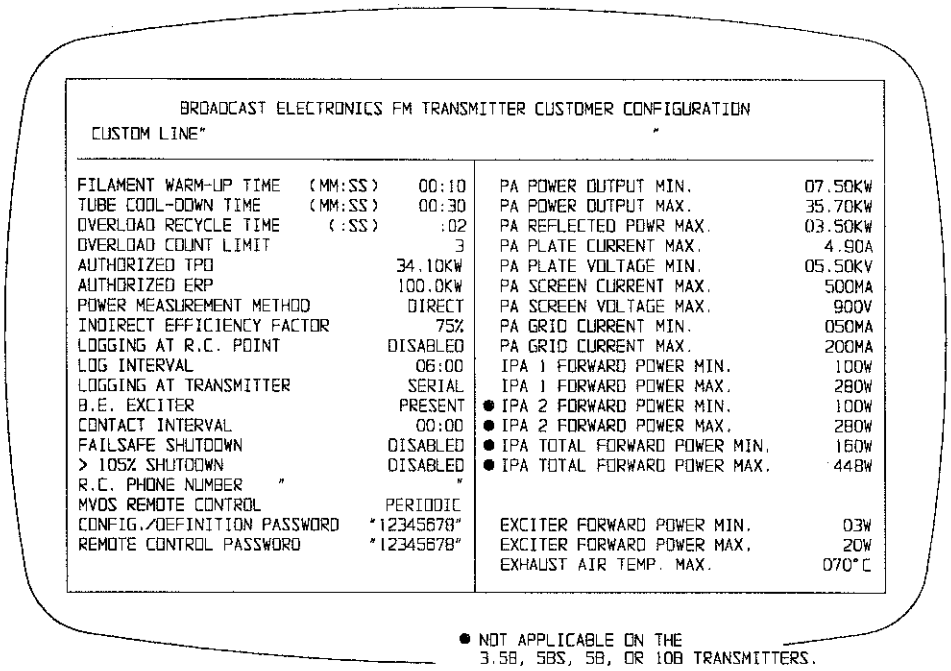
2–41. To enable remote control, enter P for periodic or C for constant as determined from the following information.

| COMMUNICATION LINK | TYPE |
|---|---|
| Dial–Up Modem | Periodic |
| 4–Wire Modem and STL or SCA RF Equipment | Constant |
| 2–Wire Modem and Leased Line | Constant |
| RS–232 Direct Connection | Constant |

2–42. **CONFIGURATION/DEFINITION PASSWORD.** The configuration/definition password is a customer generated eight character password which authorizes access to the MVDS customer configuration screen and a definition screen for MT–3 if installed. This password will replace the factory default password 12345678.

2–43. Refer to Figure 2–9 and advance the cursor to the CONFIG./DEFINITION PASSWORD field using the ⇓ key. Enter the CONFIG./DEFINITION PASSWORD. If the password cannot be recalled in the future, contact the Broadcast Electronics Customer Service Department for assistance.

2–44. **REMOTE CONTROL PASSWORD.** The remote control password is an eight character customer generated password which authorizes MVDS remote control. This password will replace the factory default password 12345678. Refer to Figure 2–9 and advance the cursor to the REMOTE CONTROL PASSWORD field using the ⇓ key. Enter the remote control password.




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597-0122-61

**FIGURE 2-9. CUSTOMER CONFIGURATION SCREEN**

## 2-45. STUDIO SITE INSTALLATION.

### 2-46. SYSTEM OPERATING PROGRAM INSTALLATION.

2-47. The system operating program will be installed at the studio site. Prior to installing the program, ensure that the communication equipment is connected at the studio site (refer to the COMMUNICATION EQUIPMENT CONNECTIONS section in the preceding text).

### 2-48. COMPUTER TERMINOLOGY.

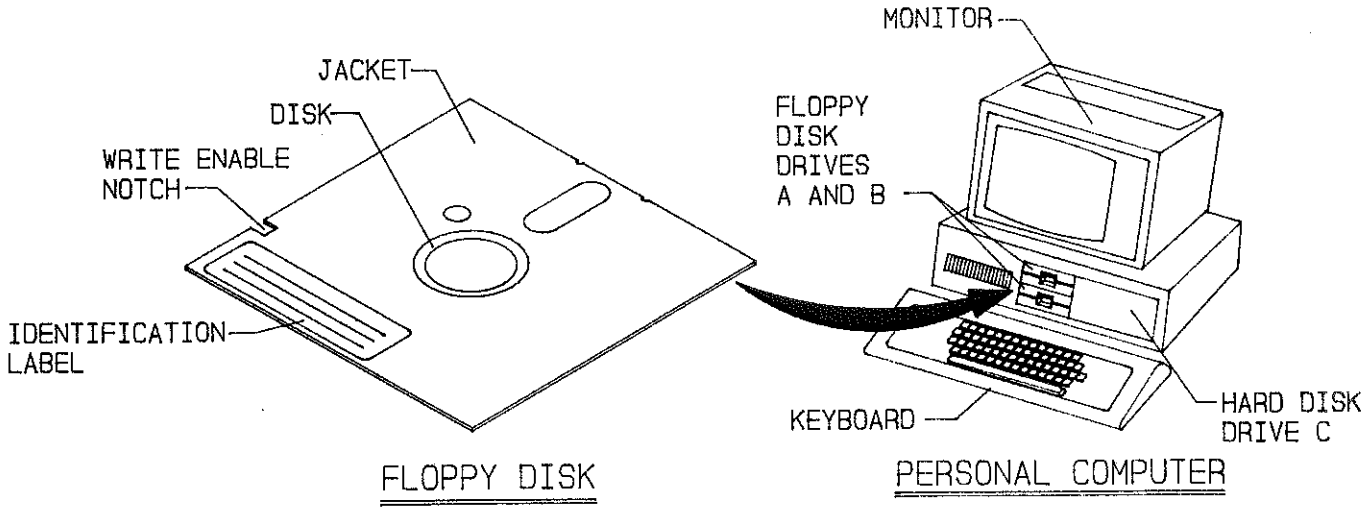
2-49. To install the RC-1 remote control operating program, an understanding of computer terminology is required. The proceeding text will describe the basic concepts for the following terms: 1) DOS, 2) keyboard, 3) floppy disk, and 4) disk drive. For detailed information, refer to the DOS manual supplied with the personal computer system.

2-50. **DOS.** A disk operating system for a computer is referred to as the DOS. The DOS is a software program which directs the transfer of information between the computer and disk drive. In addition, the DOS accepts and processes commands entered from the keyboard.

2-51. **KEYBOARD.** A keyboard is an input device which is used by the operator to generate commands to the computer (refer to Figure 2-10). When a valid DOS command is entered by depressing the appropriate key(s),the computer will execute the command. With the proper software, the keyboard can also be used to enter commands which will remotely control transmitter operations.

2-52. **FLOPPY DISK.** A floppy disk (or diskette) is a flexible magnetic disk used for storing digital information (refer to Figure 2-10). Floppy disks are available in 5 1/4 inch and 3 1/2 inch sizes. The 5 1/4 inch disk is protected by an outer cardboard jacket. The 3 1/2 inch disk is protected by a molded plastic case.

2–53. **DISK DRIVE.** A disk drive is a device which directs the storage and retrieval of digital information on the floppy disk. A computer system may consist of a single floppy disk drive, a dual floppy disk drive, or a floppy disk drive and hard disk drive combination (refer to Figure 2–10). Each disk drive is identified by capital letter A, B, or C. The magnetic disk(s) in a hard disk drive cannot be removed by the operator.




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597–0122–60

**FIGURE 2–10. COMPUTER TERMINOLOGY**

***IMPORTANT*** ***CURRENT INSTALLATION INFORMATION IS AVAILABLE IN THE READ.ME FILE.***

***IMPORTANT***

2–54. **ACCESSING THE READ.ME FILE.**

2–55. The contents of the READ.ME file contains information regarding current software modifications which effect the operation of the RC–1 remote control system. This file can be accessed as follows.

A. Insert the DOS system diskette into disk drive A (not required for hard disk drive systems). Apply power to the computer. After a short duration, the A > prompt or C > prompt will be displayed on the monitor screen. Remove the diskette.

B. Insert the RC–1 remote control diskette into disk drive A.

C. Enter A: to log onto drive A. Depress the RETURN key.

D. Enter the following DOS command.

TYPE READ.ME | MORE

E. Depress the RETURN key. The information will be displayed on the monitor screen. Press any key to continue to display the next screen of information.

2–56. **INSTALLATION REQUIREMENTS.**

2–57. During the installation program, specific information is requested regarding the system. To begin installation, determine the following information:

1. Computer communication port number.
2. Transmitter modem baud rate.
3. Transmitter modem telephone number (not required for constant mode of operation).
4. IBM Graphics compatibility of studio printer.

2–58. The RC–1 remote control program can be installed using a computer with a single floppy disk drive, a dual floppy disk drive, or a floppy disk drive in combination with a hard disk drive system. Installation instructions for each disk drive system will be discussed in the following text.

2–59. **SINGLE FLOPPY DISK DRIVE SYSTEM.**

2–60. It is recommended that a back–up copy of the RC–1 remote control diskette be generated. When completed, 1) the original RC–1 remote control diskette should be stored and used only if the back–up copy is inadvertently destroyed, 2) the back–up copy will be referred to as the RC–1 diskette. Refer to the DOS manual and the following information to generate a back–up copy.

A. Insert the DOS diskette into the disk drive and apply power to the computer. After a short duration, the monitor will display the A > prompt.

B. Enter the following command.

DISKCOPY A: A:

C. Depress the RETURN key.

D. Remove the DOS disk and follow the on–screen prompts. The source diskette refers to the original RC–1 remote control diskette. The target diskette refers to an unformatted diskette.

E. When the process is completed, the monitor will display the following message.

Copy another diskette (Y/N)?

F. Enter N and remove the back–up copy (RC–1 diskette). The monitor will display the A > prompt.

2–61. The COMMAND.COM file on the DOS system diskette must be copied to the RC–1 diskette. The file is copied to the RC–1 diskette as follows.

A. Insert the DOS system diskette into the disk drive and enter the following command.

COPY A:COMMAND.COM B:

B. Depress the RETURN key.

C. Remove the DOS system diskette and follow the on–screen prompts. The diskette for drive B refers to the RC–1 diskette. The diskette for drive A refers to the DOS diskette.

D. When the process is completed, the monitor will display the A > prompt. Remove the RC–1 diskette.

2–62. A diskette must be formatted to receive the DOS system files. The format and copy processes are simultaneously accomplished as follows. When completed, this diskette will be referred to as the installation diskette.

A. Insert the DOS system diskette into the disk drive and enter the following command.

FORMAT A:/S

B. Depress the RETURN key.

C. Remove the DOS system diskette and follow the on–screen prompts.

D. When the process is completed, the monitor will display the following message.

Format another (Y/N)?

E. Enter N and remove the installation diskette. The monitor will display the A > prompt.

2–63. The ANSI.SYS file must also be copied to the installation diskette. The ANSI.SYS file is copied as follows.

A. Insert a DOS diskette containing the ANSI.SYS file into the disk drive and enter the following command.

COPY A:ANSI.SYS B:

B. Depress the RETURN key.

C. Remove the DOS diskette and follow the on–screen prompts. The diskette for drive B refers to the installation diskette. The diskette for drive A refers to the DOS diskette.

D. When the process is completed, the monitor will display the A > prompt.

2–64. The preparations for a single floppy disk drive system are completed. Therefore, refer to the INSTALLATION PROCEDURE in the following text. The RC–1 diskette and installation diskette will be used when executing the RCINSTALL program.

2–65. **DUAL FLOPPY DISK DRIVE SYSTEM.**

2–66. It is recommended that a back–up copy of the RC–1 remote control diskette be generated. When completed, 1) the original RC–1 remote control diskette should be stored and used only if the back–up copy is inadvertently destroyed, 2) the back–up copy will be referred to as the RC–1 diskette. Refer to the DOS manual and the following information to generate a back–up copy.

A. Insert the DOS system diskette into disk drive A and apply power to the computer. After a short duration, the monitor will display the A > prompt.

B. Enter the following command.

DISKCOPY A: B:

C. Depress the RETURN key.

D. Remove the DOS system diskette and follow the on–screen prompts. The source diskette refers to the original RC–1 remote control diskette. The target diskette refers to an unformatted diskette.

E. When the process is completed, the monitor will display the following message.

Copy another diskette (Y/N)?

F. Enter N and the monitor will display the A > prompt. The back–up copy (RC–1 diskette) is in disk drive B.

2–67. The COMMAND.COM file on the DOS system diskette must be copied to the RC–1 diskette. The file is copied to the RC–1 diskette as follows.

A. Insert the DOS system diskette into disk drive A and enter the following command.

COPY A:COMMAND.COM B:

B. Depress the RETURN key.

C. When the process is completed, the monitor will display the A > prompt. Remove the RC–1 diskette.

2–68. A diskette must be formatted to receive the DOS system files. The format and copy processes are simultaneously accomplished as follows. When completed, this diskette will be referred to as the installation diskette.

A. Insert the DOS system diskette into disk drive A and enter the following command.

FORMAT B:/S

B. Depress the RETURN key and follow the on–screen prompts.

C. When the process is completed, the monitor will display the following message.

Format another (Y/N)?

D. Enter N and the monitor will display the A > prompt.

2–69. The ANSI.SYS file must also be copied to the installation diskette. The ANSI.SYS file is copied as follows.

A. Insert the DOS system diskette into disk drive A and enter the following command.

COPY ANSI.SYS B:

B. Depress the RETURN key.

C. When the process is completed, the monitor will display the A > prompt.

2–70. The preparations for a dual floppy disk drive system are completed. Therefore, refer to the INSTALLATION PROCEDURE in the following text. The RC–1 diskette and installation diskette will be used when executing the RCINSTALL program.

2–71. **FLOPPY AND HARD DISK DRIVE SYSTEM.**

2–72. It is recommended that a back–up copy of the RC–1 remote control diskette be generated. When completed, 1) the original RC–1 remote control diskette should be stored and used only if the back–up copy is inadvertently destroyed, 2) the back–up copy will be referred to as the RC–1 diskette. Refer to the DOS manual and the following information to generate a back–up copy.

A. Ensure the hard disk drive is properly formatted before proceeding. If the hard disk drive is not formatted, refer to the DOS instruction manual and format the hard drive.

B. Insert the RC–1 remote control diskette into disk drive A and apply power to the computer. After a short duration, the monitor will display the C > prompt.

C. Enter the following command.

DISKCOPY A: A:

D. Depress the RETURN key.

E. Remove the RC–1 remote control diskette and follow the on–screen prompts. The source diskette refers to the original RC–1 remote control diskette. The target diskette refers to an unformatted diskette.

F. When the process is completed, the monitor will display the following message.

Copy another diskette (Y/N)?

G. Enter N and the monitor will display the C > prompt.

2–73. The preparations for a floppy and hard disk drive system are completed. Therefore, refer to the INSTALLATION PROCEDURE in the following text. The RC–1 diskette will be used when executing the RCINSTALL program.

2–74. **INSTALLATION PROCEDURE.**

2–75. To facilitate installation, the RC–1 diskette includes an installation utility program. Upon completion, this program will automatically generate all necessary remote control system operating files. The MVDS remote control operating system is installed as follows:

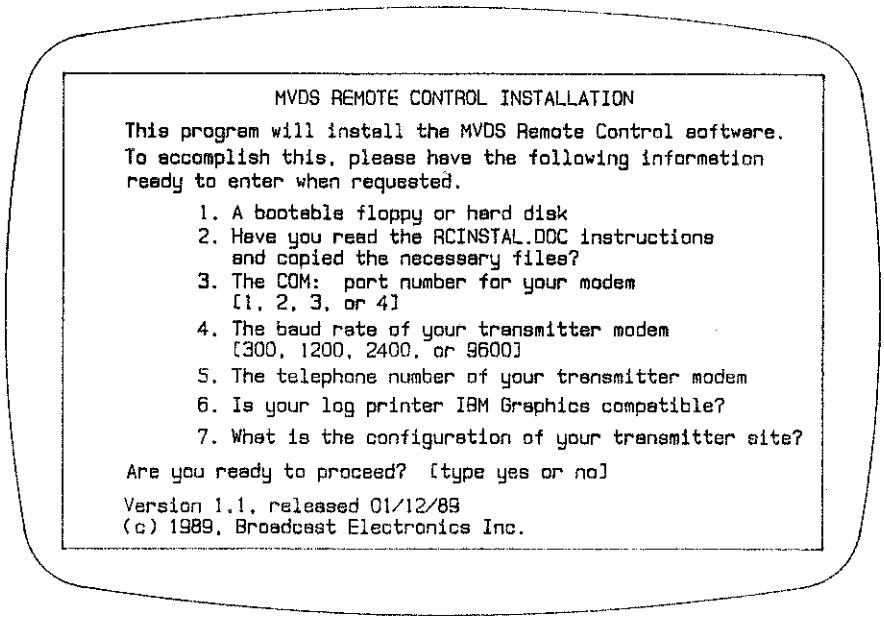
2–76. Insert the RC–1 diskette into disk drive A.

2–77. For a dual floppy disk drive system, insert the installation diskette in drive B.

2–78. Enter A: to log onto drive A. Depress the RETURN key.

2–79. Enter RCINSTAL and depress the RETURN key. The monitor will display information as shown in Figure 2–11.

2–80. Enter YES in response to the ARE YOU READY TO PROCEED prompt.

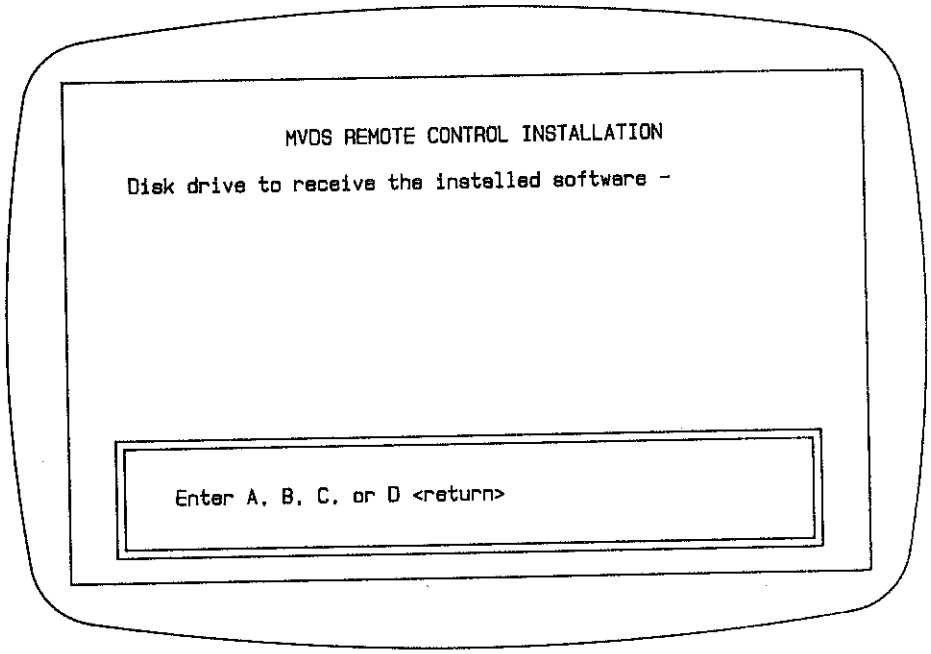



COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

**FIGURE 2–11. INSTALLATION SCREEN** **597–0122–8**

2–81. Depress the RETURN key. The monitor will display information as shown in Figure 2–12.

2–82. Enter A, B, C, or D to select the disk drive on which the operating system files will be stored. For single and dual disk drive systems, enter B. For a hard disk drive system, enter C.

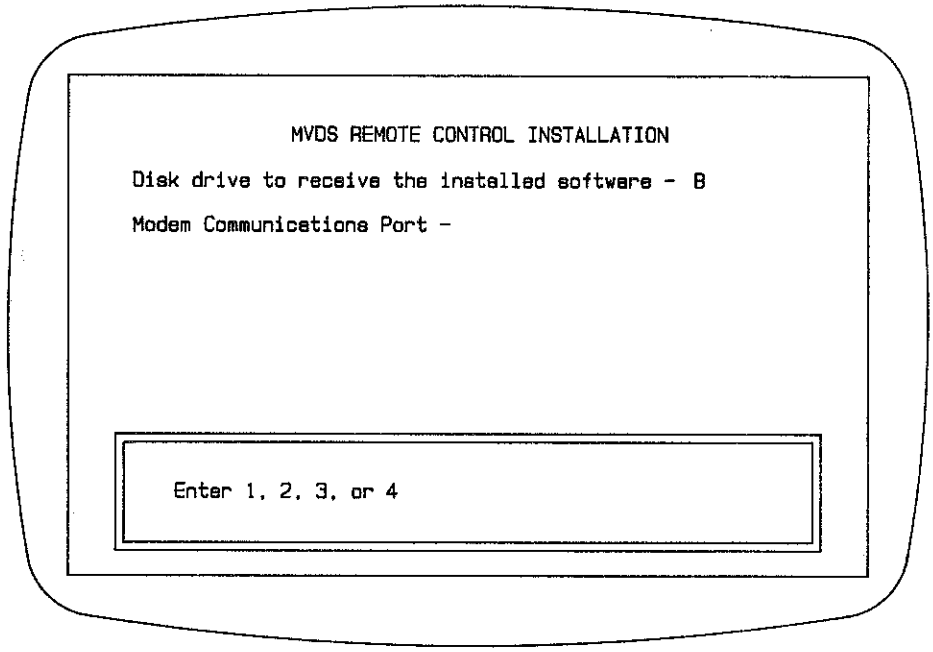



COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597–0122–9

**FIGURE 2–12. INSTALLATION SCREEN**

2–83. Depress the RETURN key. The monitor will display information as shown in Figure 2–13.

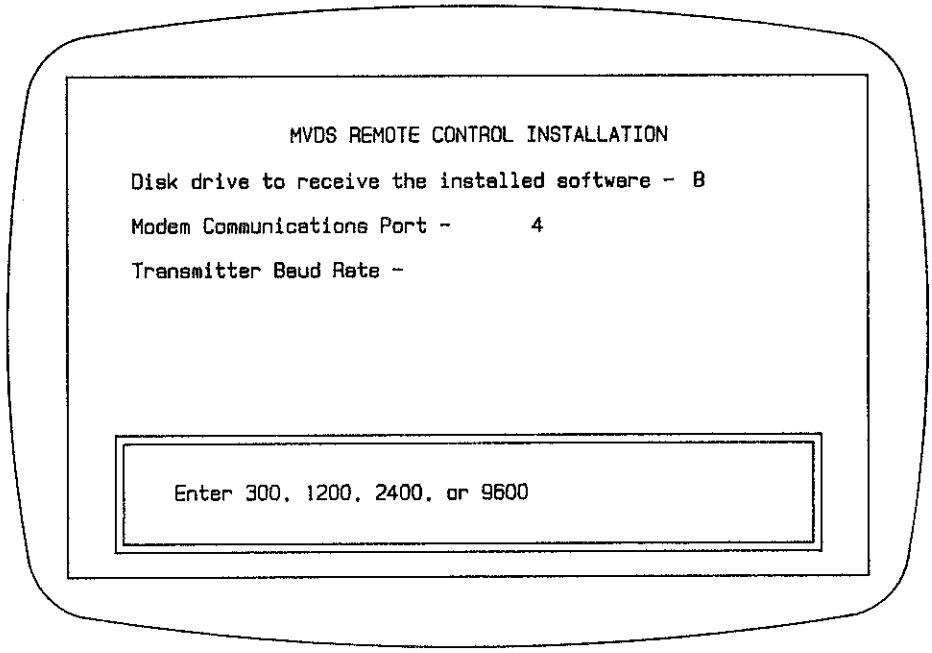



COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC
597-0122-10

**FIGURE 2–13. INSTALLATION SCREEN**

2–84. Enter 1, 2, 3, or 4 to select the modem communication port.

2–85. Depress the RETURN key. The monitor will display information as shown in Figure 2–14.



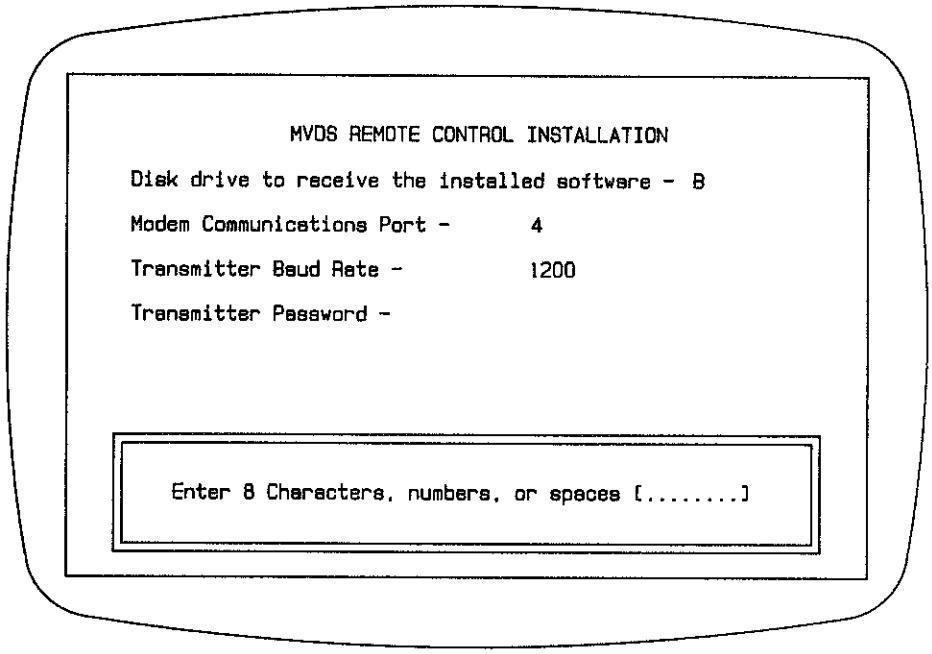

COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC
597-0122-11

**FIGURE 2–14. INSTALLATION SCREEN**

2–86. Enter 300, 1200, 2400, or 9600 to select the transmitter baud rate.

2–87. Depress the RETURN key. The monitor will display information as shown in Figure 2–15.

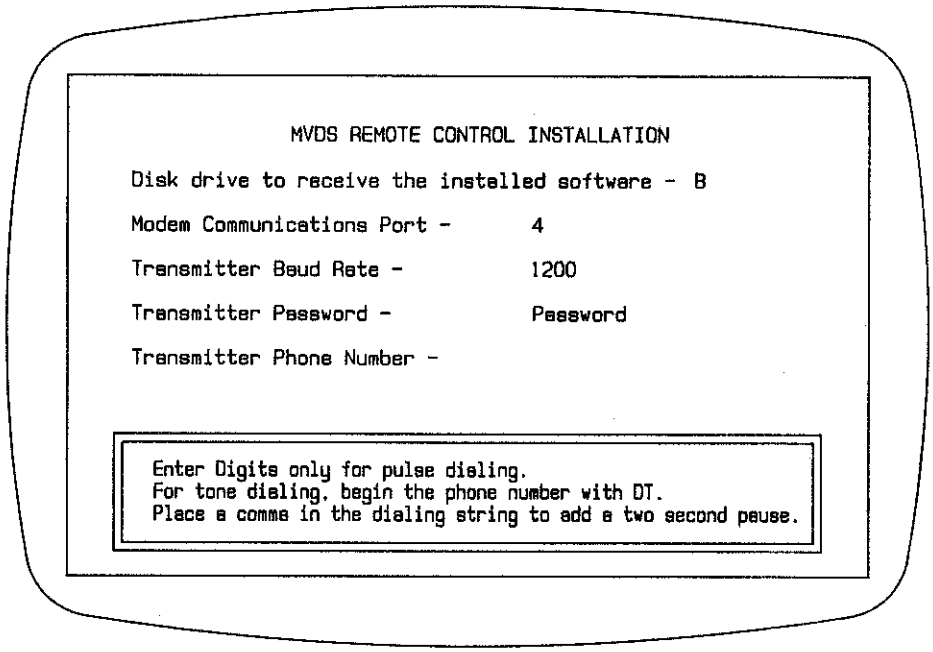
2–88. Enter the 8 character transmitter MVDS password.




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

**FIGURE 2–15. INSTALLATION SCREEN** 597-0122-12

2–89. Depress the RETURN key. The monitor will display information as shown in Figure 2–16.




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

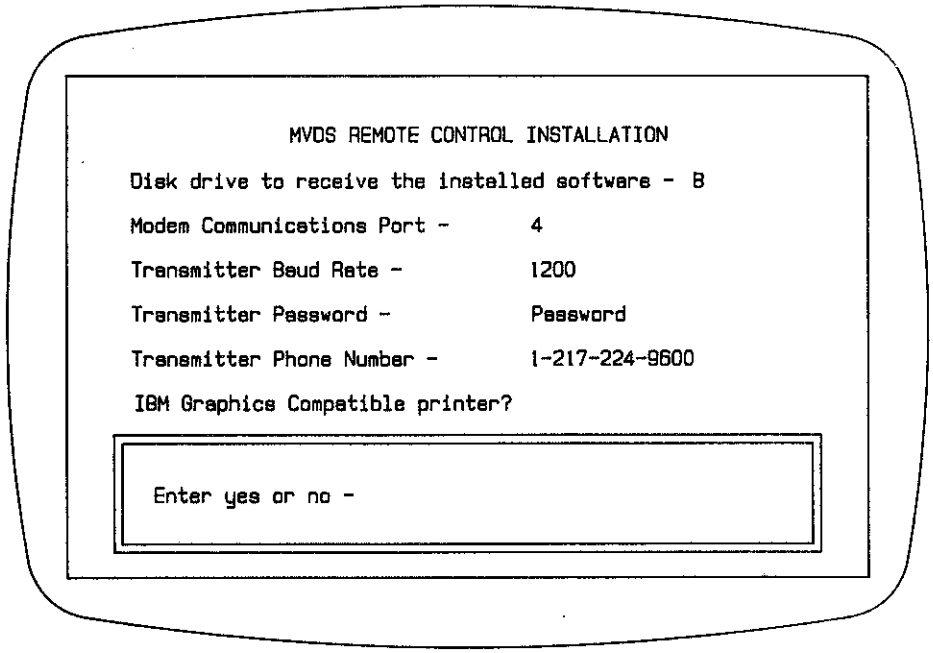
597-0122-13

**FIGURE 2-16. INSTALLATION SCREEN**

2-90. For a modem communication link, enter the transmitter telephone number. A maximum of 36 digits will be accepted. If touch tone dialing is required, enter modem command code DT. In addition, commas may be inserted into the telephone number string to provide a two second pause per comma.

2-91. For an RF communication link or direct connect, omit the transmitter telephone number.

2-92. Depress the RETURN key. The monitor will display information as shown in Figure 2-17.




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC
597-0122-14

**FIGURE 2–17. INSTALLATION SCREEN**

2–93. Enter YES (or NO) if the remote printer is IBM Graphics compatible.

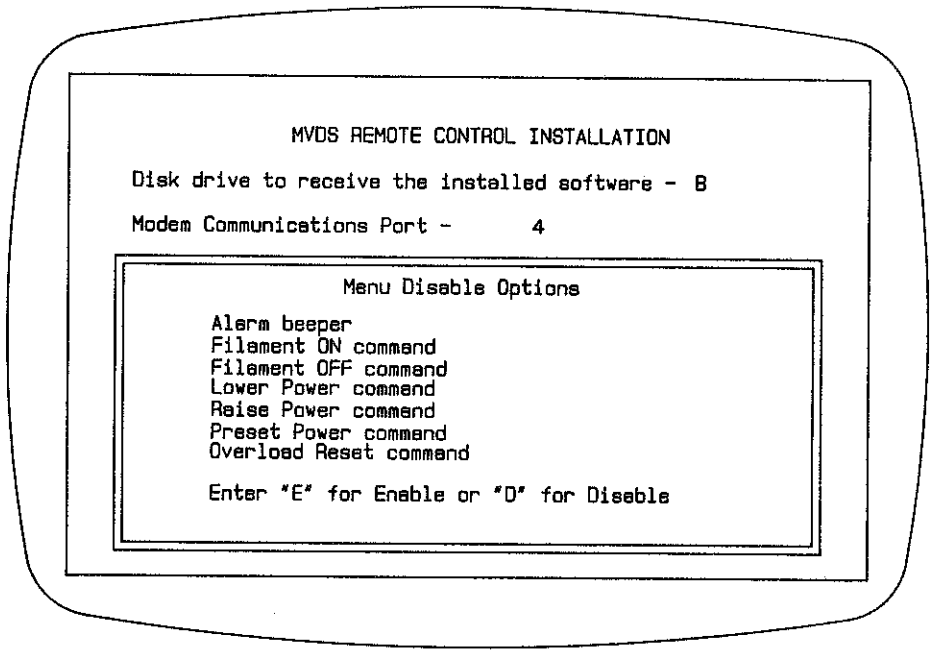
2–94. Depress the RETURN key. The monitor will display information as shown in Figure 2–18.

2–95. Six major remote control transmitter operations are assigned to keyboard function keys. The options menu (refer to Figure 2–18) allows the operator to select which transmitter operation(s) are to be disabled or enabled. In addition, a computer internal alarm can be disabled or enabled.

2–96. Enter E to enable the operation or D to disable.

2–97. When the final option is selected, the monitor will display the following message.

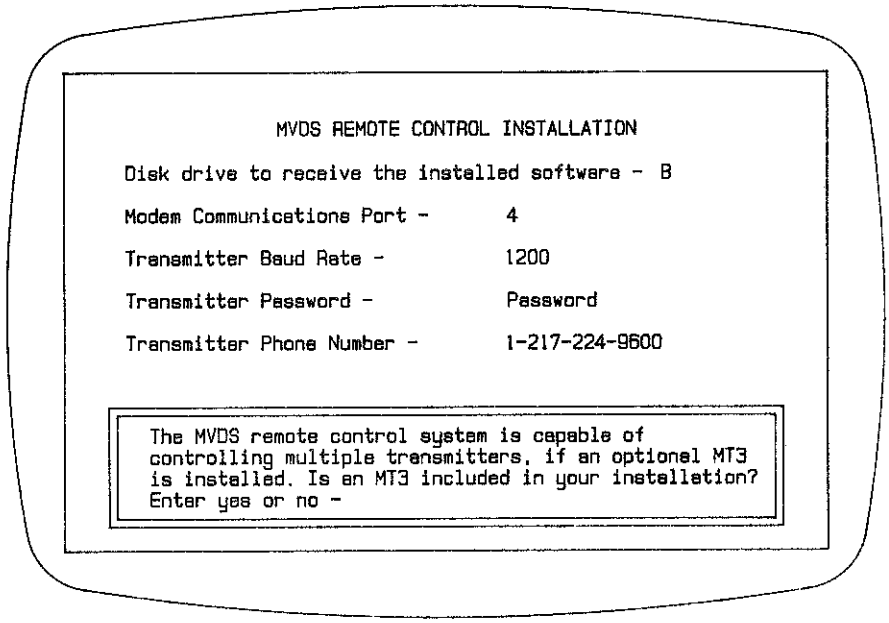
Enter 'A' to accept or 'R' to re–enter.




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC
597–0122–15

**FIGURE 2–18. INSTALLATION SCREEN**

2–98. Enter A to accept or R to modify the information. When A is entered, the monitor will display information as shown in Figure 2–19.

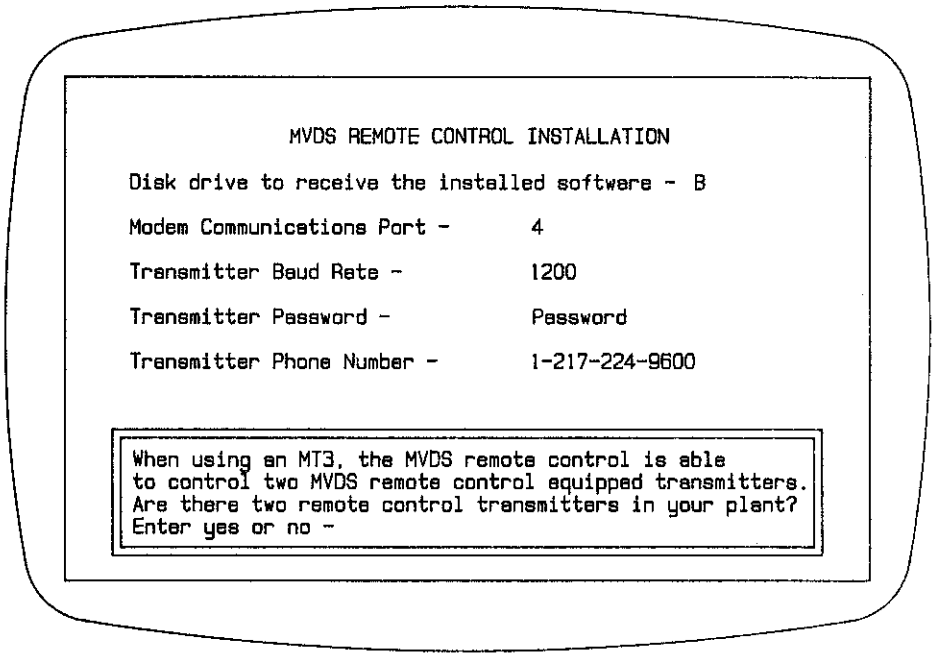



COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC
597–0122–37

**FIGURE 2–19. INSTALLATION SCREEN**

2–99. Enter NO (or YES) if an optional MT–3 multiple transmitter interface is installed.

2–100. Depress the RETURN key. The monitor will display information as shown in Figure 2–20.



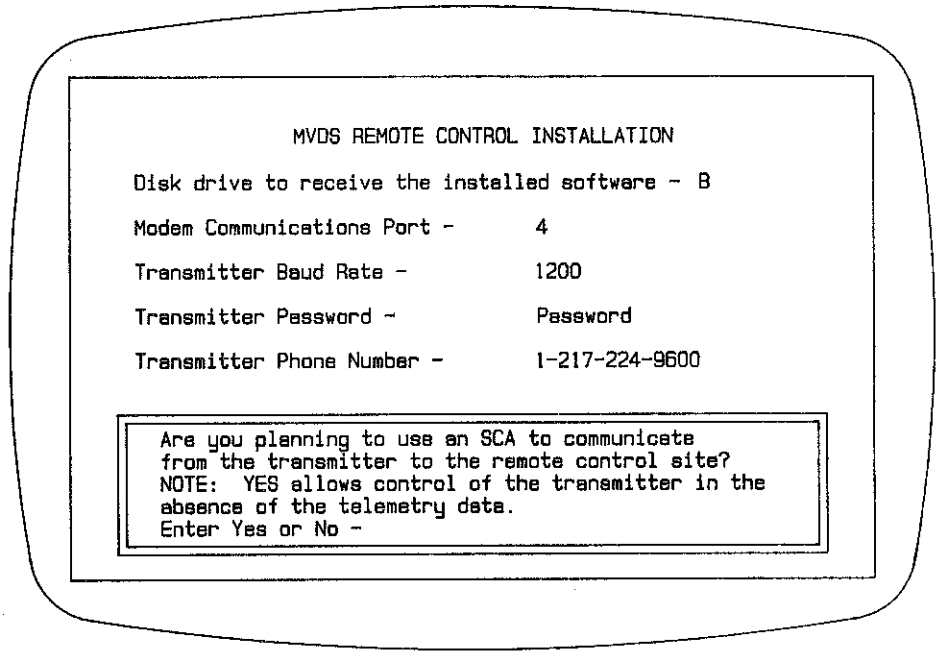

COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC
597–0122–38

**FIGURE 2–20. INSTALLATION SCREEN**

2–101. Enter YES (or NO) if the MT–3 will control two MVDS equipped transmitters.

2–102. Depress the RETURN key. The monitor will display information as shown in Figure 2–21.

2–103. Enter YES (or NO) if SCA communications equipment for transmitting RC–1 control data is installed at the transmitter site.

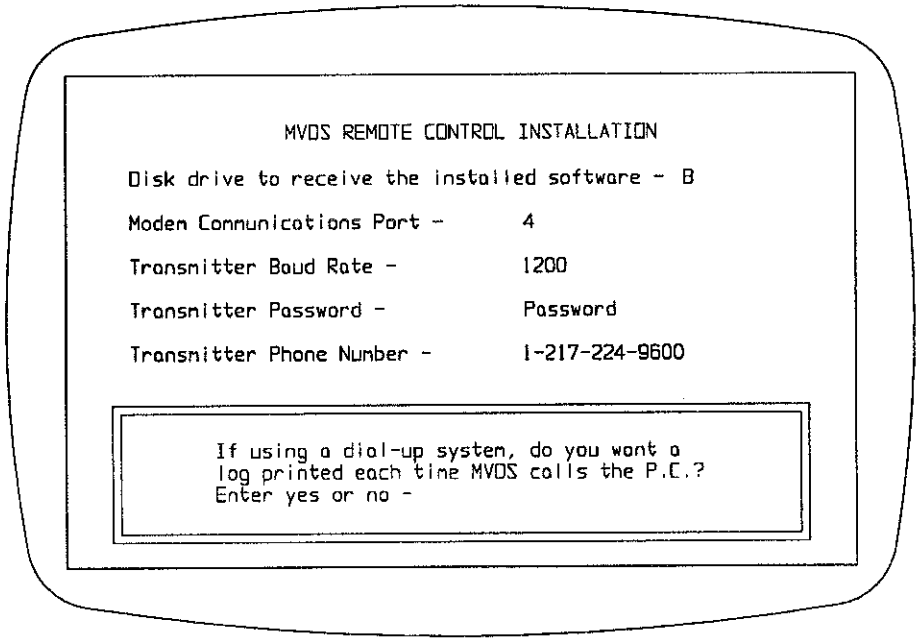



COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

**597-0122-39**

**FIGURE 2–21. INSTALLATION SCREEN**

2–104. Depress the RETURN key. The monitor will display information as shown in Figure 2–22.



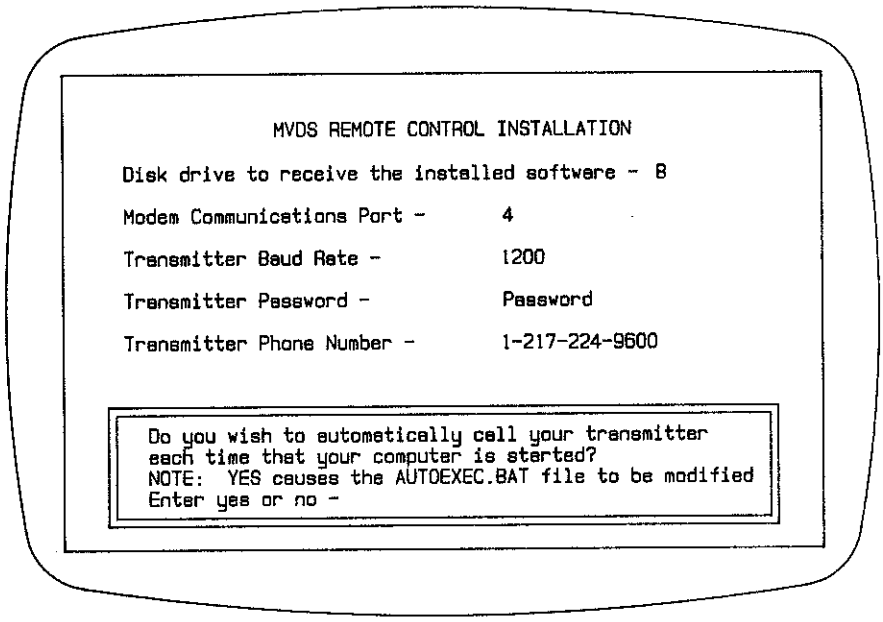

COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

**597-0122-43**

**FIGURE 2–22. INSTALLATION SCREEN**

2–105. Enter YES (or NO) if a log is to be printed each time the MVDS contacts the personal computer in a dial–up system.

2–106. Depress the RETURN key. The monitor will display information as shown in Figure 2–23.

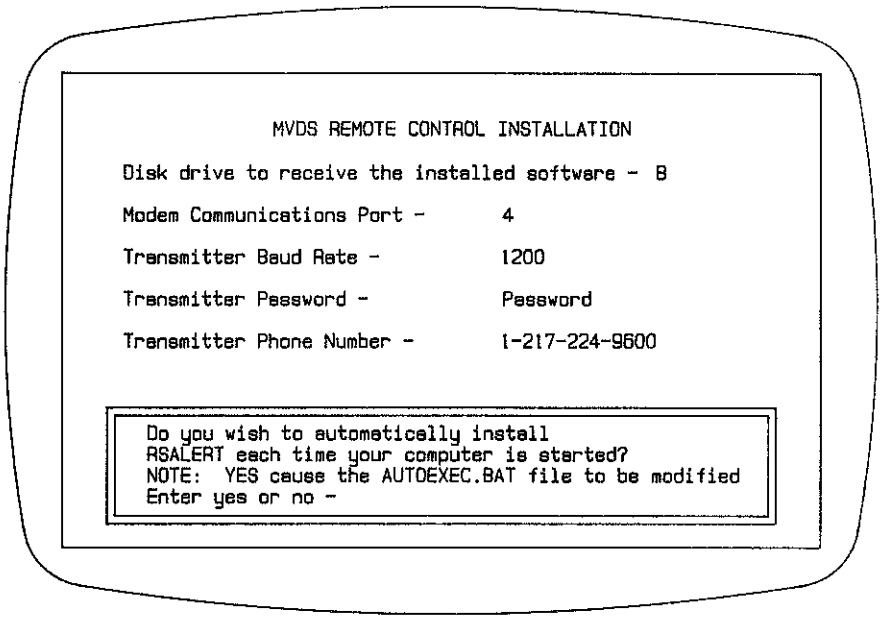



COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC
597–0122–16

**FIGURE 2–23. INSTALLATION SCREEN**

2–107. Enter YES (or NO) to provide automatic transmitter contact by the computer each time the computer power is energized.

2–108. Depress the RETURN key. The monitor will display information as shown in Figure 2–24.




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

**597-0122-17**

**FIGURE 2-24. INSTALLATION SCREEN**

2-109. RSALERT is a program which will generate a flashing alert message on the monitor when the transmitter initiates contact with the computer (refer to Figure 2-24).

2-110. Enter YES (or NO) to provide a flashing alert message.

2-111. Depress the RETURN key.

2-112. The following messages will be displayed.

CREATING NECESSARY FILES PLEASE STAND BY

2-113. For a single floppy disk drive system, remove the RC-1 diskette and follow the on-screen prompts. The diskette for drive B refers to the installation diskette. The diskette for drive A refers to the RC-1 diskette.

2-114. When the installation process is completed, the following message will be displayed.

SOFTWARE INSTALLED SUCCESSFULLY

2-115. The installation diskette will be used to operate the RC-1 remote control system. For floppy disk drive systems, this diskette will contain the necessary operating files. For hard disk drive systems, the hard disk will contain the operating files. The disk contents (directory) can be displayed to view the following files.

| FILE NAME | EXTENSION |
|---|---|
| COMMAND | COM |
| WAIT | BAT |
| DIAL | BAT |
| AUTOEXEC | BAT |
| CONFIG | SYS |
| MVDS | DIR |

2–116. The directory for a hard disk drive system is displayed as follows.

A. Enter C: and depress the RETURN key to log onto drive C.

B. Enter DIR and depress the RETURN key.

C. The disk directory will be displayed on the monitor screen.

2–117. The directory for a floppy disk drive system is displayed as follows.

A. Insert the installation diskette into disk drive A.

B. Enter A: and depress the RETURN key to log onto drive A.

C. Enter DIR and depress the RETURN key.

D. The disk directory will be displayed on the monitor screen.

2–118. If an error occurs during installation, the following messages will be displayed. To facilitate installation, examine the contents of the RCINSTAL.DOC file on the original RC–1 remote control diskette, or contact Broadcast Electronics field service for further assistance.

SOFTWARE INSTALLATION WAS NOT SUCCESSFUL
CONSULT YOUR INSTRUCTION MANUAL IF YOU NEED ASSISTANCE

## 2–119. INITIAL CHECKOUT.

2–120. The following checklist is recommended to assure proper operation of any RC–1 remote control system installation. Check off each item in the list prior to operation.

[ ] Ensure the PC–DOS or MS–DOS software is version 3.1 or greater.

[ ] Ensure the CONFIG.SYS file in the root directory includes DEVICE= ANSI.SYS.

[ ] Ensure the MVDSRC.SET file exists in the MVDS sub–directory.

[ ] Ensure the MVDSRC.SET file contains the required communication port number and transmission baud rate.

[ ] If an MT–3 is installed, ensure baud rate selector S2 on the MVDS I/O circuit board is operated to 9600.

[ ] If an MT–3 is installed, ensure S1A in the MT–3 is operated for the appropriate baud rate between the MT–3 and studio site.

2–121. Interface cables for the dial–up modem, the 2–wire modem, and the 4–wire modem systems are not interchangeable at the studio site. Furthermore, the direct connect interface cable will not operate as a modem cable. Therefore, ensure the appropriate cable is constructed and installed for the required system.

2–122. The following checklist is divided into four main system configurations. Select the appropriate type of configuration and check off each item prior to operating the system.

2–123. **DIAL–UP SYSTEM.** To assure the proper operation of a dial–up system, perform the following checkout.

[ ] Ensure the periodic mode is specified at the transmitter MVDS.

[ ] Ensure a Hayes or Hayes compatible modem is installed at the transmitter and studio sites.

[ ] Ensure the modem switches are properly operated.

[ ] Ensure the proper cables are installed at the studio and transmitter sites.

2–124. **DIRECT CONNECT SYSTEM.** To assure the proper operation of a direct connect system, perform the following checkout.

[ ] Ensure the constant mode is specified at the transmitter MVDS.

[ ] Ensure the direct connect cable is properly constructed and installed.

2–125. **2–WIRE MODEM SYSTEM.** To assure the proper operation of a 2–wire modem system, perform the following checkout.

[ ] Ensure the constant mode is specified at the transmitter MVDS.

[ ] Ensure the 2–wire modem switches are properly operated.

[ ] Ensure the proper cables are installed at the studio and transmitter sites.

[ ] Ensure a leased telephone line is installed.

2–126. **4–WIRE MODEM SYSTEM.** To assure the proper operation of 4–wire modem system, perform the following checkout.

[ ] Ensure the constant mode is specified at the transmitter MVDS.

[ ] Ensure the modem switches are properly operated.

[ ] Ensure the proper interface cables are installed at the studio and transmitter sites.

[ ] Ensure the audio cables between the 4–wire modem and the RF equipment are properly connected.

2–127. **STUDIO LOGGING PRINTER SETUP.**

2–128. The RC–1 remote control system will operate with a parallel or serial logging printer at the studio. Refer to a DOS reference guide for the proper DOS mode command and preset the printer for the desired type of installation.

*CAUTION* ***WHEN EXECUTING A DOS MODE COMMAND, THE CHARACTER P MUST NOT APPEAR IN THE ARGUMENT FIELD OF THE COMMAND TO PREVENT CONTINUOUS TESTING OF THE PRINTER READY STATUS.***

*CAUTION*

# SECTION III
# OPERATION

## 3–1. INTRODUCTION.

3–2. This section provides initial entry and standard operating procedures for the Broadcast Electronics RC–1 MVDS remote control system.

## 3–3. OPERATION.

3–4. The RC–1 MVDS remote control system is designed to control an MVDS equipped transmitter from a remote (studio) site. Therefore, the following RC–1 operating procedures are presented as viewed from the studio site.

### 3–5. KEYBOARD.

3–6. The keyboard provides communication between the operator and the RC–1 MVDS remote control system. Refer to Table 3–1 and learn the basic keyboard commands and special key functions.

3–7. **CAPS LOCK KEY FUNCTION.** The RC–1 remote control system requires the CAPS LOCK key on the keyboard to be activated when operating the system. Therefore, depress the CAPS LOCK key for upper case character entry. The **CAPS LOCK** indicator will illuminate.

*NOTE* ***THE FOLLOWING PROCEDURE ASSUMES THAT THE RC–1 IS COMPLETELY INSTALLED AND THE TRANSMITTER MVDS IS OPERATIONAL.***

*NOTE*

### 3–8. CONTACT OPERATIONS.

3–9. The command line syntax for contacting any transmitter equipped with MVDS must contain: 1) the filename of the remote control program, 2) the transmitter MVDS password, and 3) the transmitter site telephone number if required. The format and example of the command are as follows.

| | | |
|---|---|---|
| PERIODIC | FORMAT: | MVDSRC password telephone number |
| | EXAMPLE: | MVDSRC XMTRSITE 2249600 |
| CONSTANT | FORMAT: | MVDSRC password |
| | EXAMPLE: | MVDSRC XMTRSITE |

3–10. The RC–1 remote control program also provides three contact operations which utilize the files generated by the installation program. These operations will establish communication between the studio and a specific MVDS equipped transmitter. The purpose of each contact operation will be discussed in the following order.

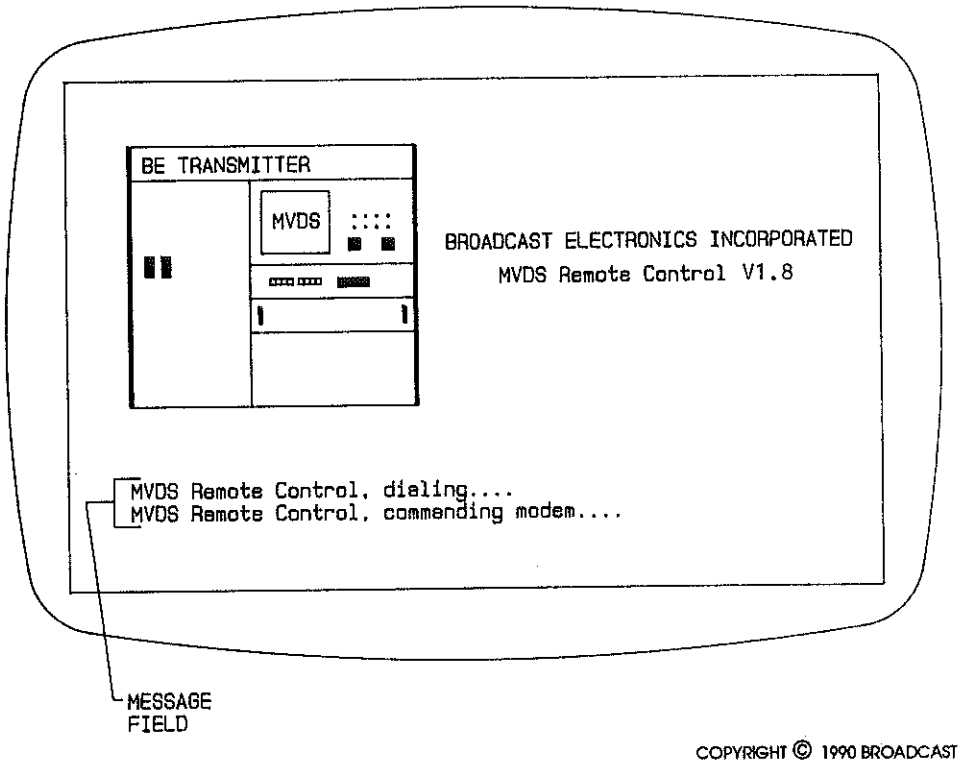
A. DIAL Operation.
B. WAIT Operation.
C. GOT Operation.

3–11. **DIAL OPERATION.** The dial operation will establish contact with the transmitter MVDS from the remote site at any time. To execute the dial operation, proceed as follows:

3–12. Enter DIAL and depress the return key. (If termination during the dialing process is desired, depress any key.) The computer monitor will display a sign–on screen with appropriate messages in the message field as shown in Figure 3–1.

TABLE 3–1. RC–1 KEYBOARD COMMANDS

| KEY | DESCRIPTION |
|---|---|
| ESC | When depressed, accesses the prompt which assures the termination of program and disconnection of communication link is the desired operation. If the Y key is depressed, the operation is completed.<br>If in the CLOCK SET mode, will terminate the mode and access the normal display screen when depressed.<br>If in the configuration screen mode, configuration data will be transmitted to the MVDS when depressed. |
| 3 | Accesses the customer configuration screen when depressed. |
| I | Accesses the MT–3 multiple transmitter interface screen when depressed (active if a multiple transmitter interface is present). |
| P | Terminates program with communication link connected when depressed. |
| L | Requests a log of the screen display on the studio printer when depressed. |
| T | Accesses the transmitter control mode when depressed. |
| C | Accesses the CLOCK SET mode when depressed (CLOCK SET is only accessible from the normal display screen). |
| A | Accesses the normal screen for the alternate MVDS transmitter when depressed (the key is only active when a multiple transmitter interface and two MVDS equipped transmitters are present). |
| F1 | Operates the transmitter high voltage circuitry to ON when depressed (one button start). |
| F2 | Operates the transmitter high voltage circuitry to OFF when depressed. |
| F3 | Operates the transmitter filament circuitry to ON when depressed. |
| F4 | Operates the transmitter filament circuitry to OFF when depressed (one button power–down). |
| F5 | Operates the transmitter lower output power function when depressed. |
| F6 | Operates the transmitter raise output power function when depressed. |
| F7 | Toggles the transmitter APC preset power function between ON and OFF when depressed. |
| F8 | Resets the transmitter overload circuitry and clears an external alarm when depressed. |




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

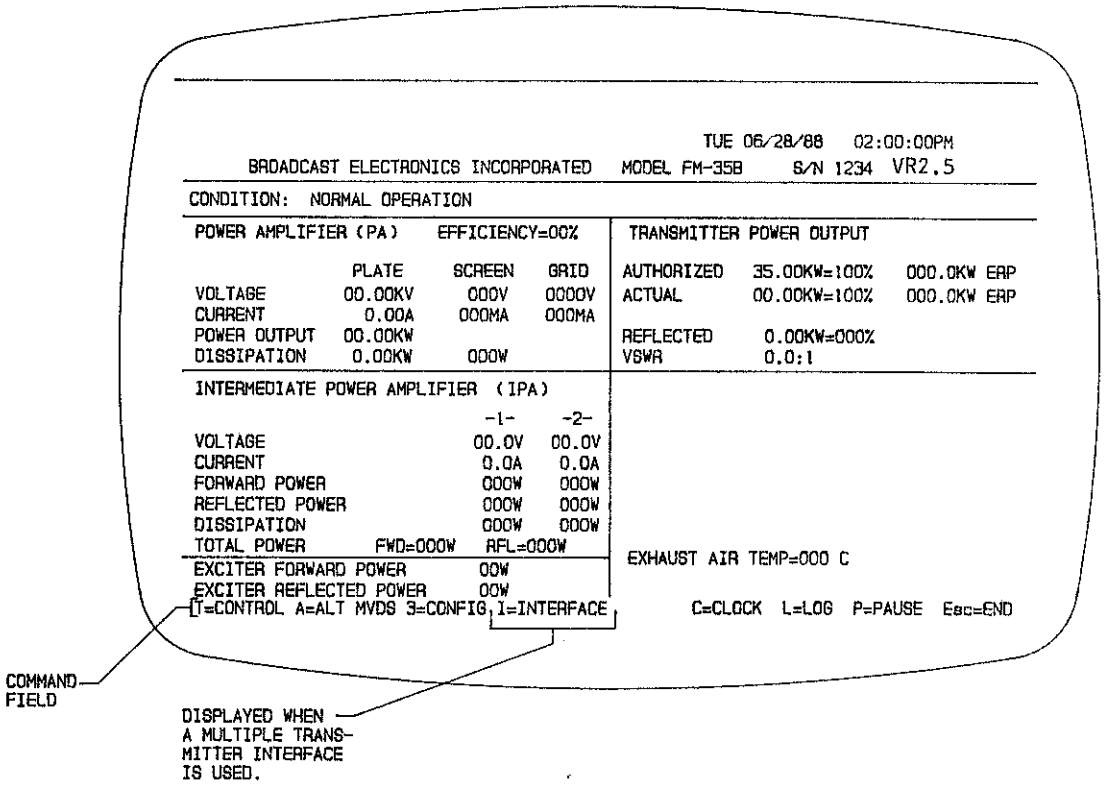
597-0122-18

**FIGURE 3-1. SIGN-ON SCREEN**

3-13. When contact is established, the computer monitor will briefly display the following message, then present the normal display screen as shown in Figure 3-2.

Getting MVDS static data

3-14. Figure 3-2 presents the normal display screen for MVDS with the RC-1 installed. A command field is included in the normal display screen. The operation of these commands will be described in the following text.




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

**597-0122-19**

**FIGURE 3–2. NORMAL DISPLAY SCREEN**

3–15. **Clock Set Operation.** To access and program the 24–hour clock, proceed as follows:

***NOTE***

***NOTE***

***DISPLAY OF CLOCK SET OPERATIONS WILL BE DELAYED 3 – 4 SECONDS DUE TO PROCESS TIME.***

A. Depress the C key. The clock set commands will be displayed at the bottom of the screen in reverse video.

B. Depress the CAPS LOCK key for upper case character entry. The **CAPS LOCK** indicator will illuminate.

C. Operate the NUM LOCK key to extinguish the **NUM LOCK** indicator.

D. Depress the C key (CLOCK SET will appear on the lower right–hand corner of the screen).

E. Depress the DELETE key (resets the 24–hour clock).

F. Depress key 1 until the correct day–of–the–week appears on the 24–hour clock.

G. Depress key 2 until the correct month appears on the 24–hour clock.

H. Depress key 3 until the correct day appears on the 24–hour clock.

I. Depress key 4 until the correct year appears on the 24–hour clock.

J. Depress key 5 until the correct hour appears on the 24–hour clock.

K. Depress key 6 until the correct minutes appears on the 24–hour clock.

L. Depress key 7 until the correct seconds appears on the 24–hour clock.

M. Depress key 8 to convert the 24–hour clock into military time (example 18:30:00) or depress 8 again for normal civilian time (example 06:30:00PM).

N. Depress key 9 to manually start (or stop) the 24–hour clock.

O. Depress the ESC key (CLOCK SET will disappear from the display and the 24–hour clock will automatically start).

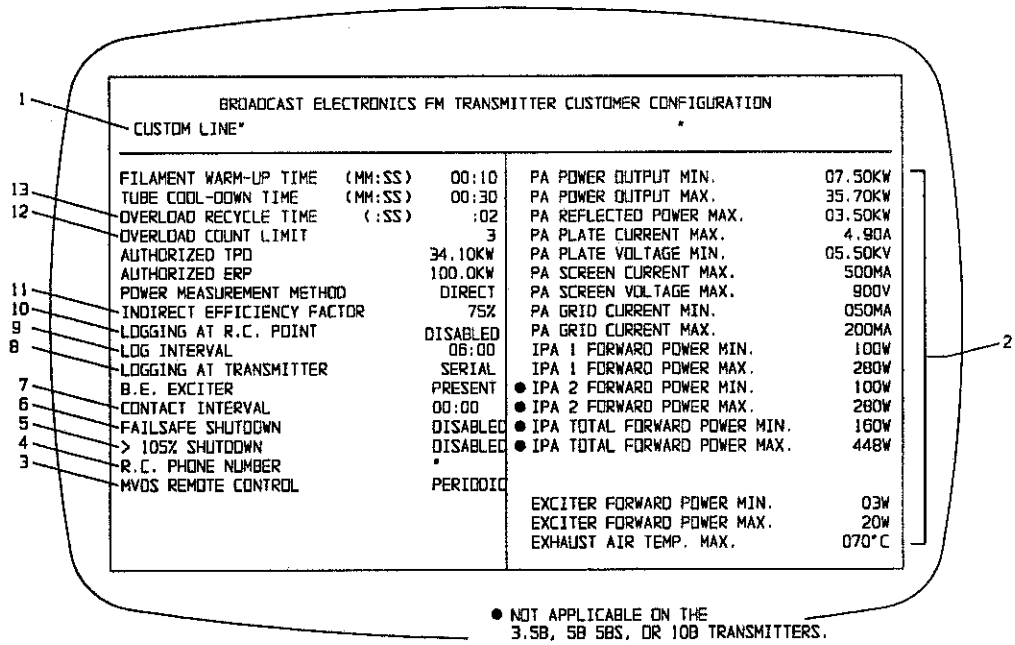
3–16. **Customer Configuration Screen Operation.** The customer configuration screen for the MVDS with RC–1 installed is presented in Figure 3–3. The following transmitter operating parameters cannot be modified remotely. Refer to Figure 3–3 and Table 3–2 for a description of the customer configuration screen.

A. AUTHORIZED TPO

B. AUTHORIZED ERP

C. INDIRECT EFFICIENCY FACTOR

D. B.E. EXCITER




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

**597–0122–70**

**FIGURE 3–3. CUSTOMER CONFIGURATION SCREEN**

## TABLE 3–2. CUSTOMER CONFIGURATION SCREEN

| INDEX NUMBER | DESCRIPTION |
|---|---|
| 1 | An operator entered message which has a maximum length of 40 characters (example: WBEI–FM 103.3 MHz) and no effect on transmitter parameters. |
| 2 | Operator minimum and maximum limits for transmitter parameters (values displayed on the screen are factory default limits). The operator entered limits must be at or below the maximum factory assigned operating levels or the cursor will not advance to the next field of entry. A limit below the minimum factory–set operating limit may be entered if required. |
| 3 | Type of communication employed by RC–1 computer remote control system. |
| 4 | An 18 digit telephone number which allows the MVDS to contact a remote site. This number can include any Hayes modem commands. |
| 5 | Condition to terminate RF output power if contact is not established with a periodic remote communication system. |
| 6 | Terminates RF output power if contact is not established within 3 hours or 3 minutes with a constant remote communication system. |
| 7 | Length of time between remote site contacts by the MVDS. (Example: 00:10 – MVDS will contact the remote site every 10 minutes.) |
| 8 | Defines the type of logging printer at the transmitter site. |
| 9 | The length of time between log printouts (example: 00:10 – a log will print every 10 minutes). |
| 10 | Enables or disables logging at the studio. |
| 11 | The indirect efficiency factor is an efficiency value which is calculated and entered at the factory and displayed on the PA section of the normal display screen (if the indirect power measurement method is selected). The indirect efficiency factor must be updated as required to reflect the changes in transmitter efficiency. |
| 12 | The number of overloads the transmitter will accept before the trans–mitter will deenergize and must be manually reset. |
| 13 | The length of time the transmitter remains off–the–air after an overload to allow the condition that prompted the overload to dissipate. |

3–17. To access and program the customer configuration screen for remote control operation, refer to Figure 3–3 and proceed as follows:

3–18. Depress the 3 key. The following message will be displayed.

ENTER PASSWORD: "  "

3–19. After the password is entered, the following message will be displayed.

Getting MVDS configuration data.

3–20. Enter any desired message on the CUSTOM LINE (40 characters maximum).

3–21. Depress the ⇓ key.

3–22. Enter the FILAMENT WARM–UP TIME. The factory operating limits are:

| | Maximum | Minimum |
|---|---|---|
| All Models | 59:59 | 00:10 |

3–23. Depress the ⇓ key.

3–24. Enter the TUBE COOL–DOWN TIME. The factory operating limits are:

| | Maximum | Minimum |
|---|---|---|
| All Models | 59:59 | 00:30 |

3–25. Depress the ⇓ key.

3–26. Enter the OVERLOAD RECYCLE TIME. The factory operating limits are:

| | Maximum | Minimum |
|---|---|---|
| All Models | 00:59 | 00:01 |

3–27. Depress the ⇓ key.

3–28. Enter the OVERLOAD COUNT LIMIT. The factory operating limits are:

| | Maximum | Minimum |
|---|---|---|
| All Models | 9 | 0 |

3–29. Depress the ⇓ key.

3–30. Enter the POWER MEASUREMENT METHOD.

D= DIRECT
I= INDIRECT

3–31. Depress the ⇓ key.

3–32. Enable the logging printer at the studio site. If studio logging is not required, enter DISABLED.

D= DISABLED
E= ENABLED

3–33. Depress the ⇓ key.

3–34. Enter the LOG INTERVAL. If no periodic logging is required, enter 00:00.

3–35. Depress the ⇓ key.

3–36. Enter the type of logging printer at the transmitter site.

S= SERIAL
P= PARALLEL
D= DISABLED

3–37. Depress the ⇓ key.

3–38. Enter the CONTACT INTERVAL. If a contact interval is not required, enter 00:00.

3–39. Depress the ⇓ key.

3–40. Enter the FAILSAFE SHUTDOWN timer. If failsafe operation is not required, enter DISABLED.

D= DISABLED
H= 3 HOURS
M= 3 MINUTES

3–41. Depress the ⇓ key.

3–42. Enter the 105% SHUTDOWN condition.

E= ENABLED
D= DISABLED

3–43. Depress the ⇓ key.

3–44. Enter the RC PHONE NUMBER and any Hayes modem commands.

3–45. Depress the ⇓ key.

3–46. Enter MVDS REMOTE CONTROL.

P= PERIODIC
C= CONSTANT

3–47. Depress the ⇓ key.

3–48. Enter the PA POWER OUTPUT MIN. The factory minimum limits are:

| FM–3.5B | FM–5B/5BS | FM–10B | FM–20B | FM–30B | FM–35B |
|---|---|---|---|---|---|
| 01.35KW | 02.00KW | 04.00KW | 07.50KW | 07.50KW | 07.50KW |

3–49. Depress the ⇓ key.

3–50. Enter the PA POWER OUTPUT MAX. The factory maximum limits are:

| FM–3.5B | FM–5B/5BS | FM–10B | FM–20B | FM–30B | FM–35B |
|---|---|---|---|---|---|
| 04.00KW | 05.75KW | 11.50KW | 22.00KW | 31.00KW | 36.75KW |

3–51. Depress the ⇓ key.

3–52. Enter the PA REFLECTED POWER MAX. The factory maximum limits are:

| FM–3.5B | FM–5B/5BS | FM–10B | FM–20B | FM–30B | FM–35B |
|---|---|---|---|---|---|
| 00.35KW | 00.40KW | 00.80KW | 01.80KW | 03.00KW | 03.00KW |

3–53. Depress the ⇓ key.

3–54. Enter the PA PLATE CURRENT MAX. The factory maximum limits are:

| FM–3.5B | FM–5B/5BS | FM–10B | FM–20B | FM–30B | FM–35B |
|---|---|---|---|---|---|
| 1.35A | 1.50A | 2.50A | 3.60A | 4.90A | 4.90A |

3–55. Depress the ⇓ key.

3–56. Enter the PA PLATE VOLTAGE MIN. The factory minimum limits are:

| FM–3.5B | FM–5B/5BS | FM–10B | FM–20B | FM–30B | M–35B |
|---|---|---|---|---|---|
| 03.90KV | 04.80KV | 05.00KV | 06.00KV | 05.50KV | 05.50KV |

3–57. Depress the ⇓ key.

3–58. Enter the PA SCREEN CURRENT MAX. The factory maximum limits are:

| FM–3.5B | FM–5B/5BS | FM–10B | FM–20B | FM–30B | FM–35B |
|---|---|---|---|---|---|
| 150mA | 150mA | 150mA | 200mA | 500mA | 500mA |

3–59. Depress the ⇓ key.

3–60. Enter the PA SCREEN VOLTAGE MAX. The factory maximum limits are:

| FM–3.5B | FM–5B/5BS | FM–10B | FM–20B | FM–30B | FM–35B |
|---|---|---|---|---|---|
| 750V | 850V | 900V | 999V | 900V | 900V |

3–61. Depress the ⇓ key.

3–62. Enter the PA GRID CURRENT MIN. The factory minimum limits are:

| FM–3.5B | FM–5B/5BS | FM–10B | FM–20B | FM–30B | FM–35B |
|---|---|---|---|---|---|
| 020mA | 020mA | 020mA | 020mA | 025mA | 025mA |

3–63. Depress the ⇓ key.

3–64. Enter the PA GRID CURRENT MAX. The factory maximum limits are:

| FM–3.5B | FM–5B/5BS | FM–10B | FM–20B | FM–30B | FM–35B |
|---|---|---|---|---|---|
| 060mA | 060mA | 100mA | 150mA | 200mA | 200mA |

3–65. Depress the ⇓ key.

3–66. Enter the IPA 1 FORWARD POWER MIN. The factory minimum limits are:

| FM–3.5B | FM–5B/5BS | FM–10B | FM–20B | FM–30B | FM–35B |
|---|---|---|---|---|---|
| 075W | 075W | 075W | 075W | 100W | 100W |

3–67. Depress the ⇓ key.

3–68. Enter the IPA 1 FORWARD POWER MAX. The factory maximum limits are:

| FM–3.5B | FM–5B/5BS | FM–10B | FM–20B | FM–30B | FM–35B |
|---|---|---|---|---|---|
| 220W | 250W | 250W | 250W | 280W | 280W |

3–69. Depress the ⇓ key.

3–70. Enter the IPA 2 FORWARD POWER MIN (FM–20B, FM–30B, and FM–35B only). The factory minimum limit is:

| FM–20B | FM–30B | FM–35B |
|---|---|---|
| 75W | 100W | 100W |

# CUSTOMER CONFIGURATION SCREEN
# QUICK REFERENCE GUIDE

| PARAMETER | FILAMENT WARM-UP TIME | | TUBE COOL DOWN TIME | | OVERLOAD RECYCLE TIME | | OVERLOAD COUNT LIMIT | | POWER MEASUREMENT METHOD | LOGGING AT R.C. POINT | LOG INTERVAL | | LOGGING AT TRANSMITTER | CONTACT INTERVAL | | FAILSAFE SHUTDOWN | 105% SHUTDOWN | R.C. PHONE NUMBER AND |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRANSMITTER | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | D = DIRECT<br>I = INCORRECT | E = ENABLE<br>D = DISABLE | MAX | MIN | D = DISABLE<br>S = SERIAL<br>P = PARALLEL | MAX | MIN | D = DISABLE<br>H = 3 HOURS<br>M = 3 MINUTES | E = ENABLE<br>D = DISABLE | MODEM COMMAND |
| FM-1B | 59:59 | 03:00 | 59:59 | 03:00 | 00:59 | 00:01 | 9 | 0 | D OR I | E OR D | 24:00 | 00:00 | D,S OR P | 24:00 | 00:00 | D, H, OR M | E OR D | PHONE NUMBER |
| FM-1.5B | | | | | | | | | | | | | | | | | | |
| FM-3.5B | | 00:10 | | 00:30 | | | | | | | | | | | | | | |
| FM-5B/5BS | | | | | | | | | | | | | | | | | | |
| FM-10B | | | | | | | | | | | | | | | | | | |
| FM-20B | | | | | | | | | | | | | | | | | | |
| FM-30B | | | | | | | | | | | | | | | | | | |
| FM-35B | | | | | | | | | | | | | | | | | | |

| PARAMETER | MVDS REMOTE CONTROL | CONFIG/ DEFINITION PASSWORD | REMOTE CONTROL PASSWORD | PA POWER OUTPUT MIN. | PA POWER OUTPUT MAX. | PA REFLECTED POWER MAX. | PA PLATE CURRENT MAX. | PA PLATE VOLTAGE MIN | PA SCREEN CURRENT MAX | PA SCREEN VOLTAGE MAX. | PA GRID CURRENT MIN. | PA GRID CURRENT MAX. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRANSMITTER | D = DISABLE<br>P = PERIODIC<br>C = CONSTANT | 8 CHARACTERS | 8 CHARACTERS | FACTORY LIMITS | FACTORY LIMITS | FACTORY LIMITS | FACTORY LIMITS | FACTORY LIMITS | FACTORY LIMITS | FACTORY LIMITS | FACTORY LIMITS | FACTORY LIMITS |
| FM-1B | P OR C | PASSWORD | PASSWORD | 00.25 KW | 01.25 KW | 00.11 KW | 00.80 A | 02.20 KV | N/A | N/A | 000 mA | 175 mA |
| FM-1.5B | | | | 00.45 KW | 01.75 KW | 00.16 KW | 00.80 A | 02.20 KV | N/A | N/A | | |
| FM-3.5B | | | | 01.35 KW | 04.00 KW | 00.35 KW | 01.35 A | 03.90 KV | 150 MA | 750 V | 020 mA | 060 mA |
| FM-5B/5BS | | | | 02.00 KW | 05.75 KW | 00.40 KW | 01.50 A | 04.80 KV | 150 MA | 850 V | | |
| FM-10B | | | | 04.00 KW | 11.50 KW | 00.80 KW | 02.50 A | 05.00 KV | 150 MA | 900 V | | 100 mA |
| FM-20B | | | | 07.50 KW | 22.00 KW | 00.80 KW | 03.60 A | 06.00 KV | 200 MA | 999 V | | 150 mA |
| FM-30B | | | | | 31.00 KW | 03.00 KW | 04.90 A | 05.50 KV | 500 MA | 900 V | 025 mA | 200 mA |
| FM-35B | | | | | 36.75 KW | 03.00 KW | 04.90 A | 05.50 KV | 500 MA | 900 V | 025 mA | |

| PARAMETER | IPA 1 FORWARD POWER MIN. | IPA 1 FORWARD POWER MAX. | IPA 2 FORWARD POWER MIN. | IPA 2 FORWARD POWER MAX. | IPA TOTAL FORWARD POWER MIN. | IPA TOTAL FORWARD POWER MAX. | EXCITER FORWARD POWER MIN. | EXCITER FORWARD POWER MAX. | EXHAUST AIR TEMP MAX. |
|---|---|---|---|---|---|---|---|---|---|
| TRANSMITTER | FACTORY LIMITS | FACTORY LIMITS | FACTORY LIMITS | FACTORY LIMITS | FACTORY LIMITS | FACTORY LIMITS | FACTORY LIMITS | FACTORY LIMITS | FACTORY LIMITS |
| FM-1B | N/A | N/A | N/A | N/A | N/A | N/A | 08 W | 50 W | N/A |
| FM-1.5B | 025 W | 100 W | | | | | 02 W | 25 W | N/A |
| FM-3.5B | 075 W | 220 W | | | | | 05 W | | 75 DEG C |
| FM-5B/5BS | | 250 W | | | | | | 30 W | |
| FM-10B | | | | | | | | 40 W | |
| FM-20B | | | 75 W | 250 W | 130 W | 448 W | 10 W | 50 W | 95 DEG C |
| FM-30B | 100 W | 280 W | 100 W | 280 W | 160 W | | 03 W | 20 W | |
| FM-35B | | | | | | | | | |

COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597-0114-100

# SECTION IV
# PARTS LISTS

## 4–1. INTRODUCTION.

4–2. This section provides descriptions and part numbers of electrical components, assemblies, and selected mechanical parts required for maintenance of the RC–1 MVDS remote control system. Each table entry in this section is indexed by reference designators appearing on the applicable schematic diagram.

**TABLE 4–1. REPLACEABLE PARTS LIST INDEX**


| TABLE NO. | DESCRIPTION | PART NO. | PAGE |
|---|---|---|---|
| 4–2 | RC–1 MVDS REMOTE CONTROL SYSTEM | 909–0122–0XX | 4–2 |
| 4–3 | RC–1 MVDS REMOTE CONTROL SYSTEM FIELD INSTALLATION KIT | 909–0128–0XX | 4–2 |
| 4–4 | 64K MEMORY CIRCUIT BOARD ASSEMBLY | 919–0110 | 4–2 |
| 4–5 | MODEM TO MVDS CABLE ASSEMBLY | 949–0152 | 4–3 |
| 4–6 | SOFTWARE KIT , FM–30B | 979–0122–014 | 4–3 |
| 4–7 | SOFTWARE KIT, FM–3.5B | 979–0122–024 | 4–3 |
| 4–8 | SOFTWARE KIT, FM–5B | 979–0122–034 | 4–3 |
| 4–9 | SOFTWARE KIT, FM–10B | 979–0122–054 | 4–3 |
| 4–10 | SOFTWARE KIT, FM–35B | 979–0122–064 | 4–4 |
| 4–11 | SOFTWARE KIT, FM–20B | 979–0122–074 | 4–4 |
| 4–12 | SOFTWARE KIT, FM–5BS | 979–0122–094 | 4–4 |

## TABLE 4–2. RC–1 MVDS REMOTE CONTROL SYSTEM – 909–0122–0XX

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| —— | RC–1 Remote Control Software | 979–0066 | 1 |
| —— | Modem to MVDS Cable Assembly | 949–0152 | 1 |

## TABLE 4–3. RC–1 MVDS REMOTE CONTROL SYSTEM FIELD INSTALLATION KIT – 909–0128–0XX

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| —— | RC–1 Remote Control Software | 979–0066 | 1 |
| —— | Modem to MVDS Cable Assembly | 949–0152 | 1 |
| —— | 64K Memory Circuit Board Assembly | 919–0110 | 1 |

## TABLE 4–4. 64K MEMORY CIRCUIT BOARD ASSEMBLY – 919–0110 (Sheet 1 of 2)

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| C1,C2,C3 | Capacitor, Ceramic Disc, 0.01 uF ±20%, 25V | 000–1044 | 3 |
| C4 | Capacitor, Tantalum, 1.0 uF, 35V | 064–1063 | 1 |
| C8 THRU C28 | Capacitor, Ceramic Disc, 0.01 uF ±20%, 25V | 000–1044 | 21 |
| J1 THRU J24 | Programmable Jumper | 340–0004 | 24 |
| S2 | Switch, SPST, 8–Segment, 16–Pin DIP | 340–0003 | 1 |
| U1 | Resistor Network, 410A472, 4.7 k Ohm, Single–in–Line Package, 10–Pin | 226–4740 | 1 |
| U2 | Integrated Circuit, SN74LS138N, 1 of 8 Decoder, 16–Pin DIP | 228–2138 | 1 |
| U3 | Resistor Network, 410A472, 4.7 k Ohm, Single–in–Line Package, 10–Pin | 226–4740 | 1 |
| U4 | Integrated Circuit, SN74LS138N, 1 of 8 Decoder, 16–Pin DIP | 228–2138 | 1 |
| U5 | Resistor Network, 410A472, 4.7 k Ohm, Single–in–Line Package, 10–Pin | 226–4740 | 1 |
| U6,U7 | Integrated Circuit, SN74LS138N, 1 of 8 Decoder, 16–Pin DIP | 228–2138 | 2 |
| U10 | Resistor Network, 783–1–R4.7K, 4.7 k Ohm, Single–in–Line Package, 6–Pin | 226–4741 | 1 |
| U14 THRU U17 | Integrated Circuit, SN74LS244N, Octal Tri–State Bus Driver, 20–Pin DIP | 228–2244 | 4 |
| U19 | Resistor Network, 410A472, 4.7 k Ohm, Single–in–Line Package, 10–Pin | 226–4740 | 1 |
| U20 | Integrated Circuit, SN74LS20N, Dual 4–Input, Schottky, 14–Pin DIP | 228–2420 | 1 |
| U21 | Integrated Circuit, SN74LS04N, Schottky Hex Inverter, 14–Pin DIP | 228–2404 | 1 |
| X1 | Integrated Circuit, HM6116P–4, 2K x 8 RAM, CMOS, 24–Pin DIP | 229–6116 | 1 |
| X2 | Integrated Circuit, X2816AD, E2PROM 2K X 8 RAM, NMOS, 24–Pin DIP | 220–2816 | 1 |
| X3 THRU X25,X29,X30 | Integrated Circuit, AM2716B–250DC, EPROM 2K X 8, 12.5V PGM, 250 nS, 24–Pin DIP | 229–2716 | 25 |
| XU2,XU4, XU6,XU7 | Socket, 16–Pin DIP | 417–1604 | 4 |
| XU14 THRU XU17 | Socket, 20–Pin DIP | 417–2004 | 4 |

## TABLE 4–4. 64K MEMORY CIRCUIT BOARD ASSEMBLY – 919–0110 (Sheet 2 of 2)

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| XU18,XU20, XU21,XU22 | Socket, 14–Pin DIP | 417–1404 | 4 |
| XX1 THRU XX32 | Socket, 24–Pin DIP | 417–2404 | 32 |
| —— | Connector Header, 3–Pin In–line | 417–0003 | 24 |
| —— | Blank 64K Memory Circuit Board | 518–0017 | 1 |

## TABLE 4–5. MODEM TO MVDS CABLE ASSEMBLY – 949–0152

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| —— | Capacitor, Mica, 390 pF ±5%, 100V | 042–3922 | 1 |
| —— | Connector Plug, 25–Pin | 417–0251 | 2 |
| —— | Pins, Connector | 417–0142 | 10 |
| —— | Cable Shield, 3 Contact Positions | 418–0044 | 2 |
| —— | RF Choke, 4.7 uH ±10%, 430 mA, DC Resistance: 0.55 Ohms, 0.43 Amperes Maximum, Resonant at 115 MHz | 360–0022 | 1 |
| —— | RS232 Jumper Box | 417–0301 | 1 |

## TABLE 4–6. SOFTWARE KIT, FM–30B – 979–0122–014

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| X3 THRU X25,X29,X30 | Integrated Circuit, MM2716Q, EPROM, NMOS, 24–Pin DIP with RC–1 Software for FM–30B Transmitter | 229–2716 | 25 |

## TABLE 4–7. SOFTWARE KIT, FM–3.5B – 979–0122–024

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| X3 THRU X25,X29,X30 | Integrated Circuit, MM2716Q, EPROM, NMOS, 24–Pin DIP with RC–1 Software for FM–3.5B Transmitter | 229–2716 | 25 |

## TABLE 4–8. SOFTWARE KIT, FM–5B – 979–0122–034

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| X3 THRU X25,X29,X30 | Integrated Circuit, MM2716Q, EPROM, NMOS, 24–Pin DIP with RC–1 Software for FM–5B Transmitter | 229–2716 | 25 |

## TABLE 4–9. SOFTWARE KIT, FM–10B – 979–0122–054

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| X3 THRU X25,X29,X30 | Integrated Circuit, MM2716Q, EPROM, NMOS, 24–Pin DIP with RC–1 Software for FM–10B Transmitter | 229–2716 | 25 |

**TABLE 4–10. SOFTWARE KIT, FM–35B – 979–0122–064**

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| X3 THRU X25,X29,X30 | Integrated Circuit, MM2716Q, EPROM, NMOS, 24–Pin DIP with RC–1 Software for FM–35B Transmitter | 229–2716 | 25 |

**TABLE 4–11. SOFTWARE KIT, FM–20B – 979–0122–074**

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| X3 THRU X25,X29,X30 | Integrated Circuit, MM2716Q, EPROM, NMOS, 24–Pin DIP with RC–1 Software for FM–20B Transmitter | 229–2716 | 25 |

**TABLE 4–12. SOFTWARE KIT, FM–5BS – 979–0122–094**

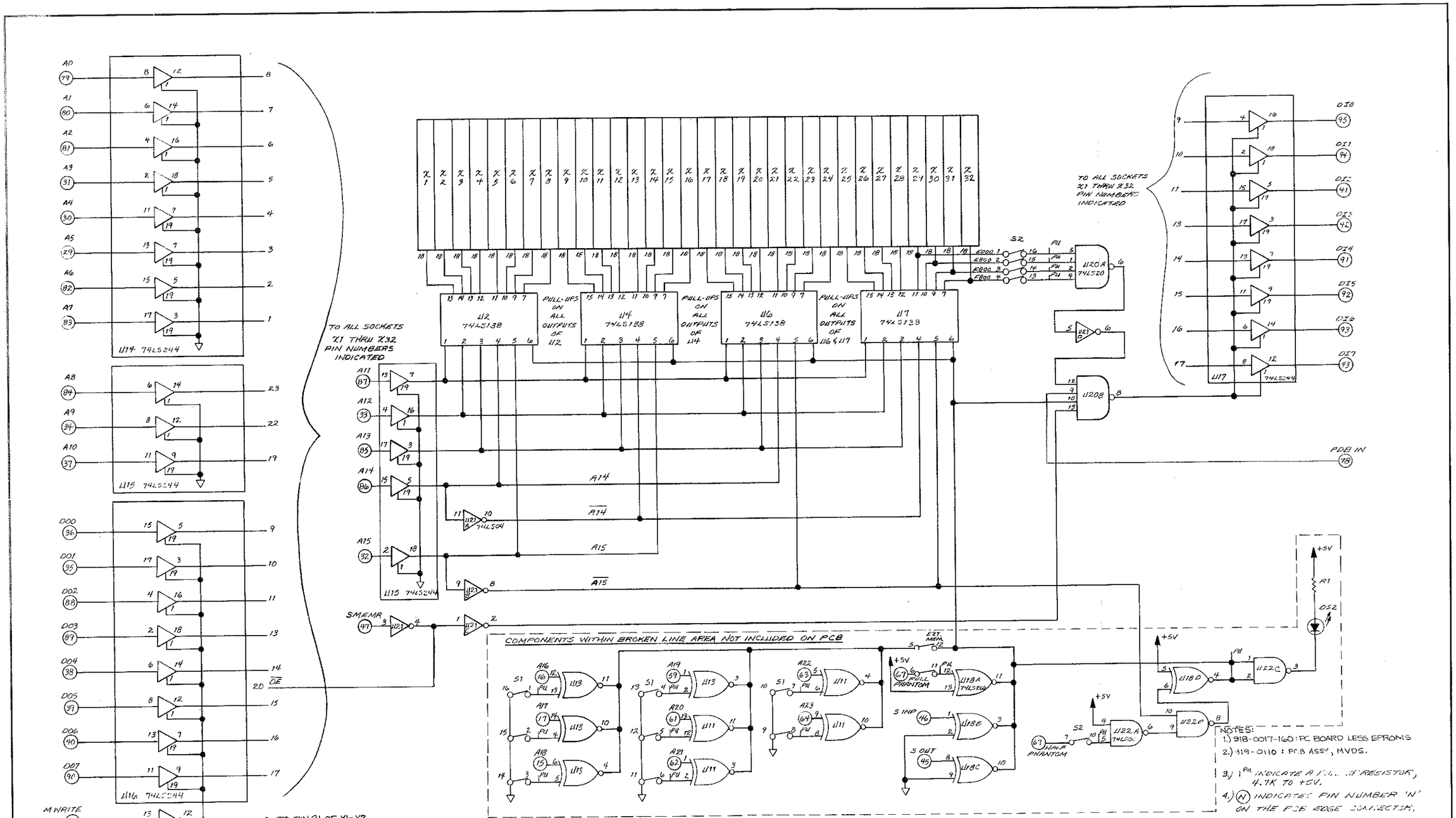
| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| X3 THRU X25,X29,X30 | Integrated Circuit, MM2716Q, EPROM, NMOS, 24–Pin DIP with RC–1 Software for FM–5BS Transmitter | 229–2716 | 25 |

# SECTION V
# DRAWINGS

## 5–1. INTRODUCTION.

5–2. This section provides assembly diagrams, schematic diagrams, and cable diagrams as listed below for the Broadcast Electronics RC–1 MVDS remote control system.

| FIGURE | TITLE | NUMBER |
|---|---|---|
| 5–1 | 64K MEMORY CIRCUIT BOARD SCHEMATIC | SD919–0110 |
| 5–2 | 64K MEMORY CIRCUIT BOARD ASSEMBLY | AC919–0110 |
| 5–3 | MODEM TO MVDS CABLE ASSEMBLY | AD949–0152 |
| 5–4 | DIRECT CONNECT COMMUNICATION CABLE ASSEMBLY | 597–0122–53 |
| 5–5 | PC TO 4–WIRE OR 2–WIRE MODEM CABLE ASSEMBLY | AB949–0173 |




NOTES:
1.) 918-0017-160: PC BOARD LESS EPROMS
2.) 919-0110: PCB ASSY, MVDS.
3.) 1 PU INDICATE A PULL UP RESISTOR, 4.7K TO +5V.
4.) (N) INDICATES PIN NUMBER 'N' ON THE PCB EDGE CONNECTOR.

COPYRIGHT © 1988 BROADCAST ELECTRONICS, INC.

COPYRIGHT © 1988 BROADCAST ELECTRONICS, INC.

PROPRIETARY RIGHTS are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE UNLESS OTHERWISE SPECIFIED
DECIMAL 2 PL=.01 3PL=.005
FRACTIONAL ±1/64
ANGULAR ± 1°
SHARP EDGES TO
BEND RADII
FILLET RADII

MATERIAL

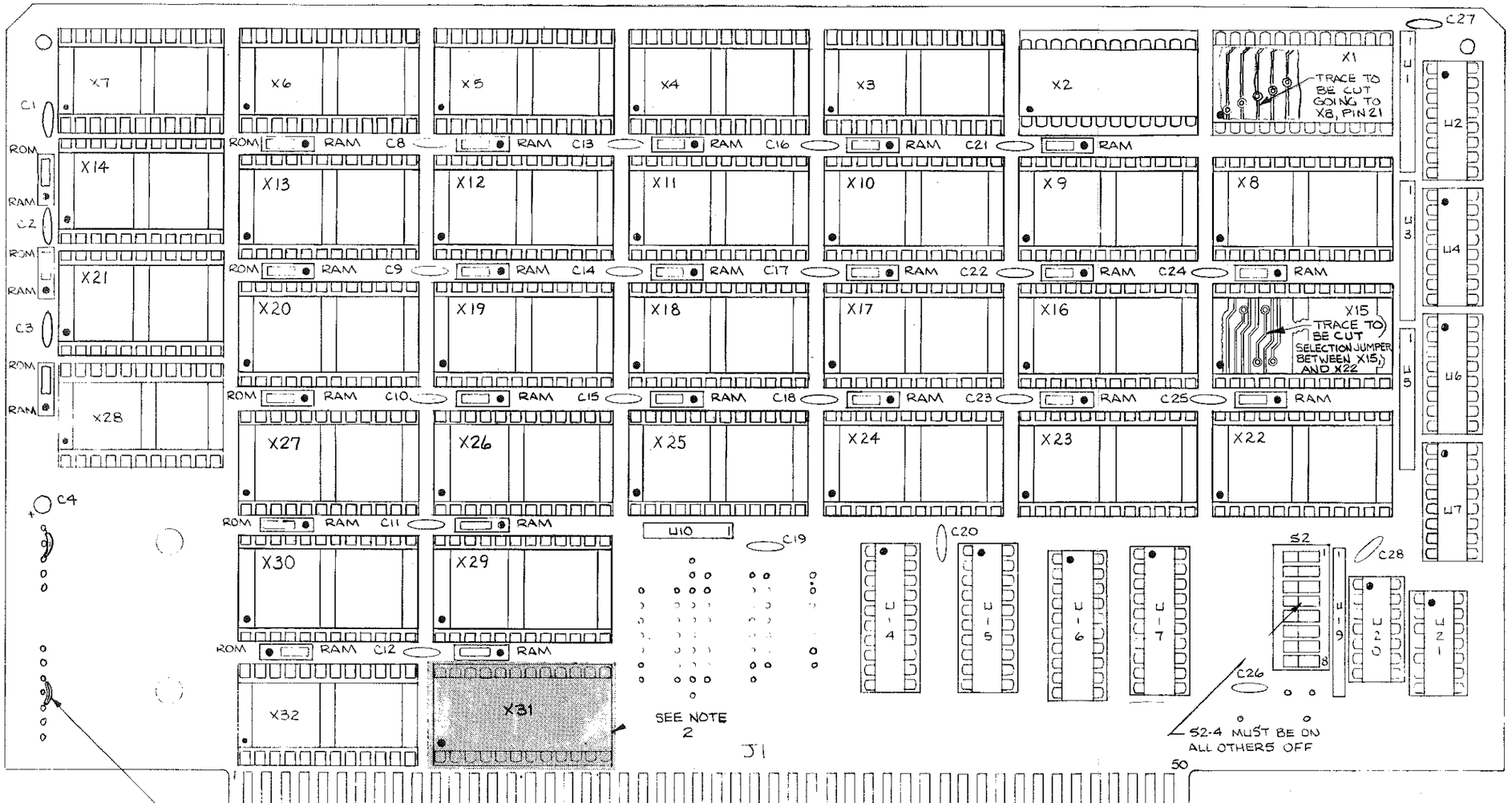
| | | |
|---|---|---|
| DRAWN BY JAH | DATE 6-14-88 | |
| CHECKED BY | DATE | |
| PROJECT ENGR. | DATE 6-29-88 | |
| APPROVED BY | | |
| TREATMENT OR FINISH | | |

**BROADCAST ELECTRONICS INC.**
—A FILMWAYS COMPANY—

TITLE SCHEM, 64K MEMORY BOARD (MVDS V2.0 & NEWER SOFTWARE)

D DWG. NO. 918-0017-160 919-0110 REV. D

SCALE NTS SHEET 1 OF 1




SEE SCHEMATIC #SD919-0110

601-0022 BUSS WIRE
693-0220 TEFLON TUBING
(2 PLCS)

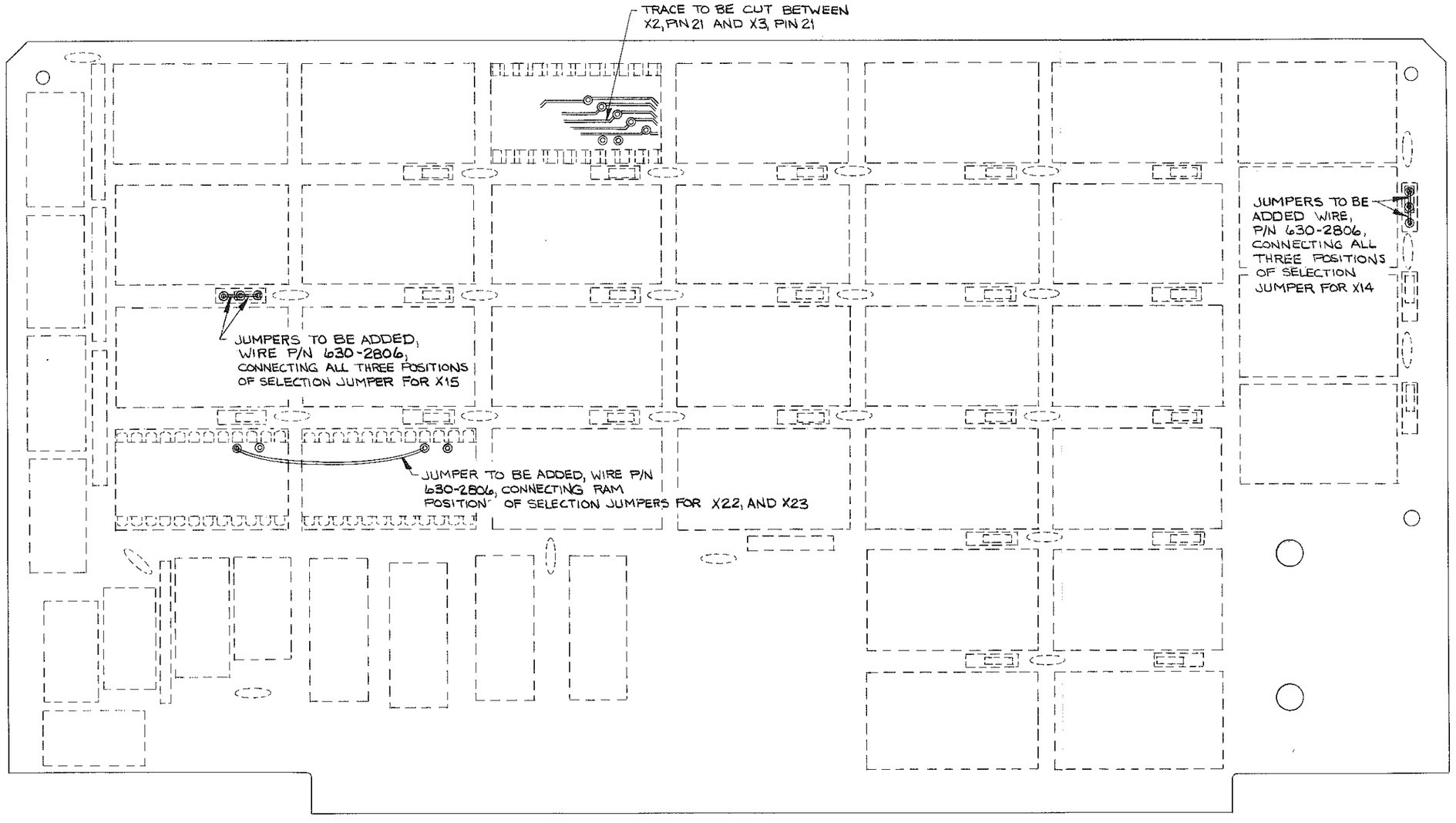
NOTE:

1. 2716 EPROM'S (X29, X30) ARE TO BE PROGRAMMED FOR FM-20B.
2. SOCKET X31, INDICATED BY SHADED AREA, TO BE FILLED WITH PROGRAMMED EPROM ONLY ON BOARDS PROGRAMMED FOR USE IN FM-30A OR FM-35A. THIS EPROM WILL BE ADDED BY TRANSMITTER TEST, IF REQUIRED.

PROPRIETARY RIGHTS are included in information disclosed hereon. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed for manufacturing for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1

| | | | |
|---|---|---|---|
| DWN. BY JAH 9-9-93 | MATERIAL SEE B/M 919-0110 | BROADCAST ELECTRONICS INC. | |
| CHKD | | 4100 N. 24TH ST., P.O. BOX 3605 QUINCY, IL 62305 217 224-9600 TELEX 250142 CABLE BROADCAST | |
| ME | FINISH | TITLE PCB ASSEMBLY, 64K MEMORY BOARD | |
| PROJ ENGR. KLC 09-09-93 | | TYPE A / SIZE C / DWG. NO. 919-0110 | REV D |
| MFG. | NEXT ASSY. | MODEL xMTR CONTROLLER / SCALE 2/1 | SHEET 1 OF 2 |




REAR VIEW OF 919-0110

PROPRIETARY RIGHTS are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY JAH 9-9-88
CHKD
ME
PROJ. ENGR. RLC 09-09-88
MFG.

MATERIAL SEE B/M 919-0110
FINISH
SEE DWG RA592-0000
NEXT ASSY.

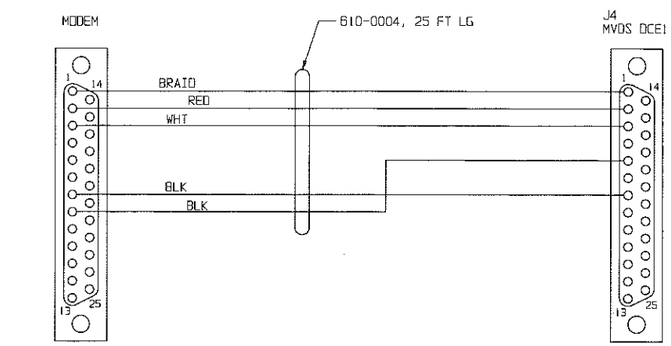
BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O.BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE PCB ASSEMBLY, 64K MEMORY BOARD

| TYPE | SIZE | DWG. NO. | REV |
|---|---|---|---|
| A | C | 919-0110 | D |

MODEL XMTR CONTROLLER | SCALE 2/1 | SHEET 2 OF 2

| WIRING OF MODEM 417-0251 | |
|---|---|
| PIN NO. | WIRE NO. |
| 1 | BRAID |
| 2 | RED |
| 3 | WHT |
| 4 | |
| 5 | |
| 6 | |
| 7 | BLK |
| 8 | BLK |
| 9 | |
| 10 | |
| 11 | |
| 12 | |
| 13 | |
| 14 | |
| 15 | |
| 16 | |
| 17 | |
| 18 | |
| 19 | |
| 20 | |
| 21 | |
| 22 | |
| 23 | |
| 24 | |
| 25 | |

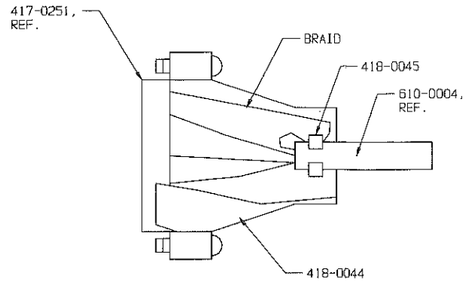



CONNECTOR - 417-0251
PINS - 417-0142 (5)

CONNECTOR - 417-0251
PINS - 417-0142 (5)

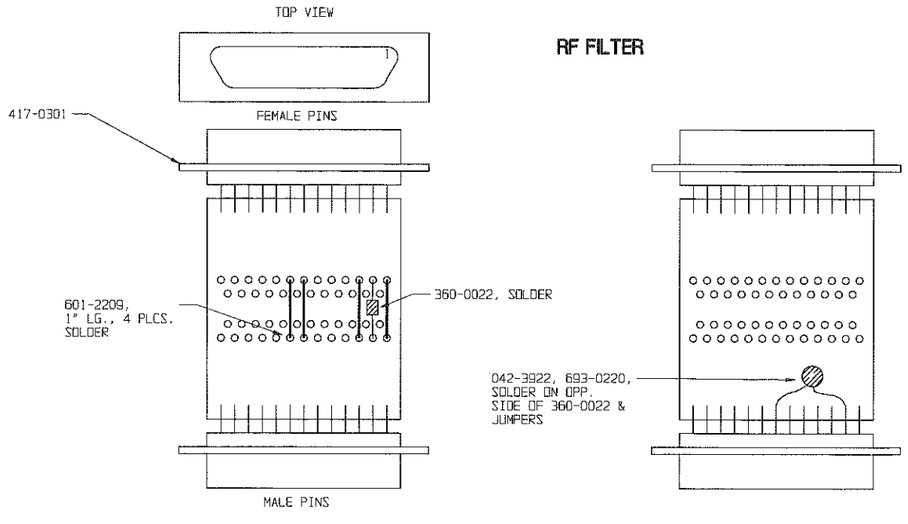
| WIRING OF J4 417-0251 | |
|---|---|
| PIN NO. | WIRE NO. |
| 1 | BRAID |
| 2 | RED |
| 3 | WHT |
| 4 | |
| 5 | BLK |
| 6 | |
| 7 | BLK |
| 8 | |
| 9 | |
| 10 | |
| 11 | |
| 12 | |
| 13 | |
| 14 | |
| 15 | |
| 16 | |
| 17 | |
| 18 | |
| 19 | |
| 20 | |
| 21 | |
| 22 | |
| 23 | |
| 24 | |
| 25 | |

NOTE:
1) TEST BOTH BLK WIRES TO MAKE SURE THEY GO TO THE CORRECT PINS.
2) CONNECT RF FILTER ASSY TO MODEM END.




DETAIL 'A'
EACH END

## RF FILTER




HARDWARE INCLUDED BUT NOT SHOWN

COPYRIGHT © 1995 BROADCAST ELECTRONICS, INC.

PROPRIETARY RIGHTS are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY MSE 2-22-88
DESIGNER(S)
PROJ. LEADER KLC 2-22-88
MFG.

MATERIAL SEE BOM 949-0152
FINISH
SEE DWG BA982-0000
NEXT ASSY.

BROADCAST ELECTRONICS INC.
4100 N.24TH ST.,P.O.BOX 3606 QUINCY,IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST FAX 217/224-9607

TITLE
ASSY, CABLE, MODEM TO MVDS

| TYPE | SIZE | DWG. NO. | REV |
|---|---|---|---|
| A | D | 949-0152 | D |

MODEL MVDS SCALE NTS SHEET 1 OF 1

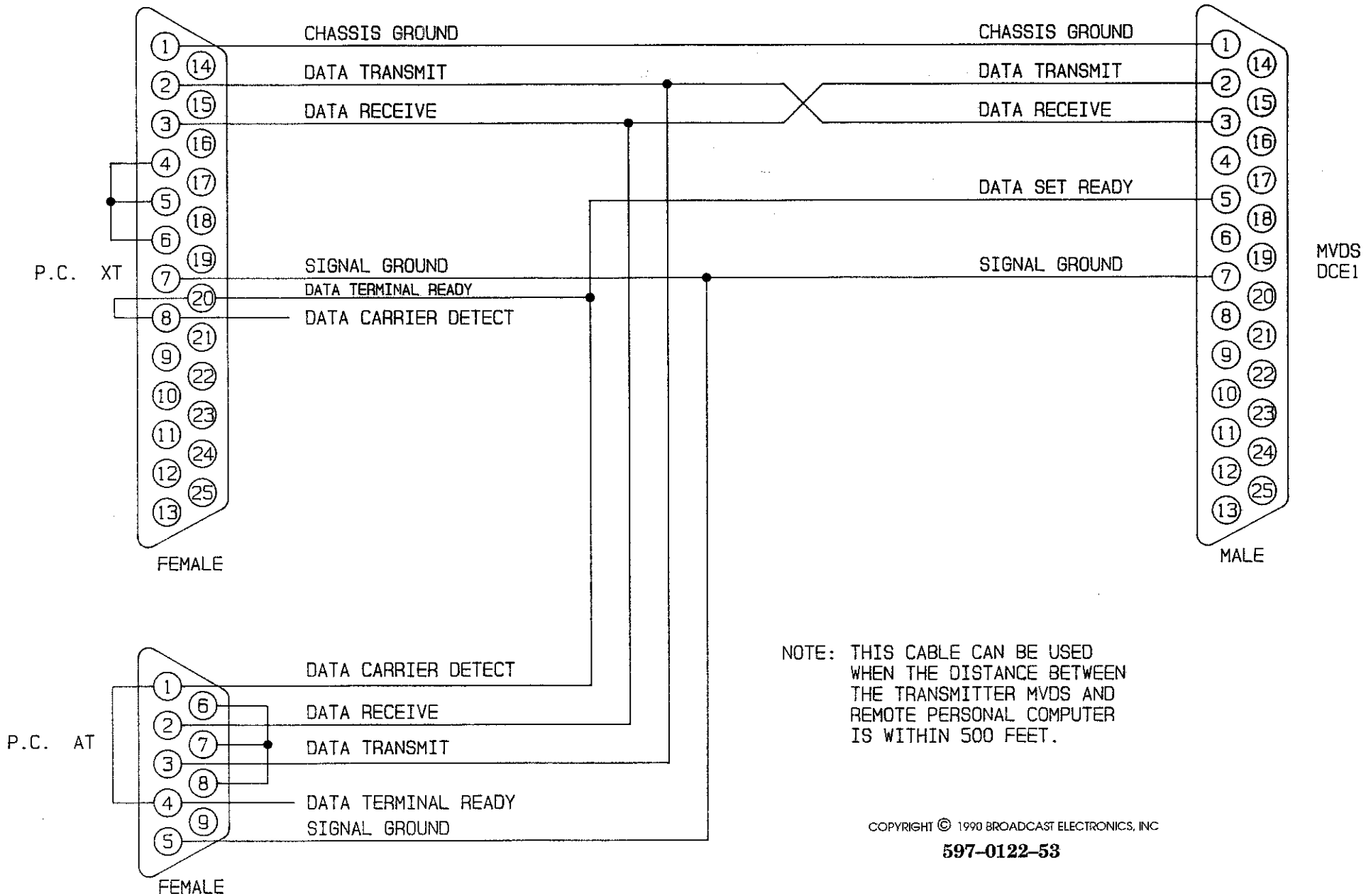
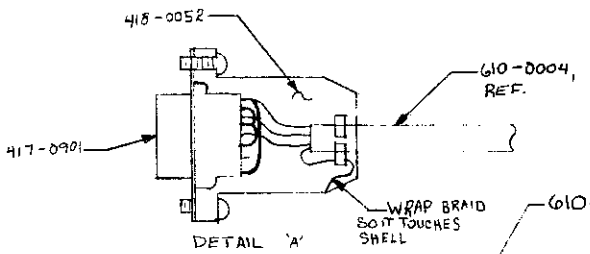
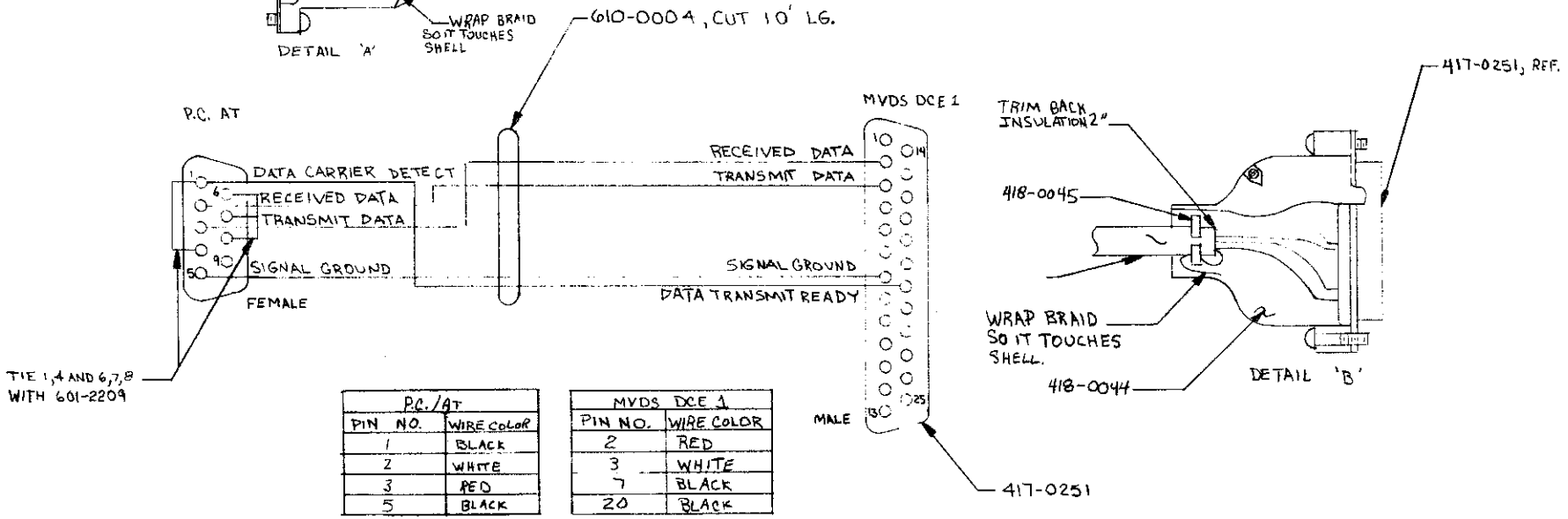



**FIGURE 5–4. DIRECT CONNECT COMMUNICATION CABLE ASSEMBLY DIAGRAM**




| P.C./AT | |
|---|---|
| PIN NO. | WIRE COLOR |
| 1 | BLACK |
| 2 | WHITE |
| 3 | RED |
| 5 | BLACK |

| MVDS DCE 1 | |
|---|---|
| PIN NO. | WIRE COLOR |
| 2 | RED |
| 3 | WHITE |
| 7 | BLACK |
| 20 | BLACK |

**PROPRIETARY RIGHTS** are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1

DWN. BY RRH 2-2-89
CHKD MH 2-17-89
ME
PROJ. ENGR.
MFG.

MATERIAL SEE B/M 949-0173
FINISH
SEE DWG RA592-0000
NEXT ASSY.

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O. BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE - ASSY -
CABLE, PC TO DUMB MODEM

| TYPE | SIZE | DWG. NO. | REV |
|---|---|---|---|
| A | B | 949-0173 | A |

MODEL MVDS REMOTE CONTROL SCALE ~ SHEET 1 OF 1

# TABLE OF CONTENTS


| PARAGRAPH | DESCRIPTION | PAGE NO. |
|---|---|---|
| **SECTION I** | **GENERAL INFORMATION** | |
| 1–1 | Introduction | 1–1 |
| 1–3 | Equipment Description | 1–1 |
| 1–8 | Options and Accessories | 1–1 |
| 1–10 | Sensing Equipment | 1–2 |
| 1–12 | Equipment Specifications | 1–2 |
| **SECTION II** | **INSTALLATION** | |
| 2–1 | Introduction | 2–1 |
| 2–3 | Unpacking | 2–1 |
| 2–7 | Installation | 2–1 |
| 2–9 | Placement | 2–1 |
| 2–12 | Communication Equipment Connections | 2–2 |
| 2–14 | Configuration A | 2–2 |
| 2–15 | Configuration B | 2–2 |
| 2–16 | Configuration C | 2–2 |
| 2–17 | Configuration D | 2–2 |
| 2–18 | Configuration E | 2–2 |
| 2–19 | Transmitter Connections | 2–2 |
| 2–21 | MVDS Equipped Transmitters | 2–2 |
| 2–22 | Non–MVDS Transmitter | 2–2 |
| 2–27 | Switch Programming Check | 2–14 |
| 2–29 | System Operation | 2–14 |
| 2–30 | Carrier Detect | 2–14 |
| 2–31 | Baud Rate | 2–14 |
| 2–32 | Programming the Modems | 2–14 |
| 2–33 | Dial–Up Modems | 2–14 |
| 2–34 | 4–Wire Modems | 2–14 |
| 2–35 | 2–Wire Modems | 2–14 |
| 2–36 | System Operating Program Installation | 2–14 |
| 2–38 | Programming the Definition Screen | 2–17 |
| **SECTION III** | **OPERATION** | |
| 3–1 | Introduction | 3–1 |
| 3–3 | MT–3 Indicators | 3–1 |
| 3–5 | Operation | 3–2 |
| 3–8 | Contact Operation | 3–2 |
| 3–10 | Selecting A Transmitter | 3–2 |
| 3–11 | MVDS Transmitter | 3–2 |
| 3–12 | Non–MVDS Transmitter | 3–2 |
| 3–13 | Interface Screen Operations | 3–3 |
| 3–15 | Interface Control Mode | 3–4 |
| 3–19 | System Messages | 3–5 |

| PARAGRAPH | | PAGE NO. |
|---|---|---|
| **SECTION IV** | **THEORY OF OPERATION** | 4–1 |
| 4–1 | Introduction | 4–1 |
| 4–3 | General Description | 4–1 |
| 4–5 | Logic Circuit Board | 4–1 |
| 4–7 | Input/Output Circuit Board | 4–1 |
| 4–9 | Relay Circuit Board | 4–1 |
| 4–11 | Power Supply | 4–1 |
| 4–13 | Detailed Description | 4–1 |
| 4–14 | Logic Circuit Board | 4–2 |
| 4–16 | CPU Circuit | 4–2 |
| 4–22 | Timing Generator Circuits | 4–5 |
| 4–26 | Device Select Decoder Circuit | 4–5 |
| 4–29 | CPU Memory Circuit | 4–5 |
| 4–33 | Status Input and Control Circuit | 4–6 |
| 4–38 | Analog Input Circuit | 4–7 |
| 4–51 | Transmitter A and Transmitter B Communication Circuits | 4–8 |
| 4–58 | Remote Communication Circuit | 4–8 |
| 4–63 | Power–Up Preset Circuit | 4–8 |
| 4–65 | Address Monitor Circuit | 4–8 |
| 4–67 | Power Supply | 4–10 |
| 4–70 | +5 Volt Supply | 4–10 |
| 4–71 | +12 Volt Supply | 4–10 |
| 4–72 | +15 Volt Supply | 4–10 |
| 4–73 | –15 Volt Supply | 4–10 |
| 4–74 | –5 Volt Supply | |
| **SECTION V** | **MAINTENANCE** | 5–1 |
| 5–1 | Introduction | 5–1 |
| 5–3 | Safety Considerations | 5–1 |
| 5–5 | First Level Maintenance | 5–1 |
| 5–7 | General | 5–1 |
| 5–9 | Electrical | 5–1 |
| 5–11 | Second Level Maintenance | 5–1 |
| 5–14 | Electrical Adjustments | 5–1 |
| 5–15 | Required Equipment | 5–2 |
| 5–16 | A/D Converter Offset and Gain Adjustments (R26 and R27) | 5–3 |
| 5–18 | Fuse Link Replacement | 5–3 |
| 5–20 | Troubleshooting | 5–6 |
| 5–23 | Component Replacement | 5–6 |
| 5–29 | Integrated Circuits | |
| **SECTION VI** | **PARTS LIST** | 6–1 |
| 6–1 | Introduction | |
| **SECTION VII** | **DRAWINGS** | 7–1 |
| 7–1 | Introduction | |

## LIST OF TABLES


| TABLE NO. | DESCRIPTION | PAGE NO. |
|---|---|---|
| 1–1 | Sensing Equipment | 1–2 |
| 1–2 | MT–3 Electrical Characteristics | 1–3 |
| 1–3 | MT–3 Physical Characteristics | 1–3 |
| 2–1 | Definition Screen | 2–20 |
| 3–1 | MT–3 Indicators | 3–2 |
| 3–2 | Interface Screen | 3–3 |
| 3–3 | Interface Commands | 3–4 |
| 3–4 | Control Mode Commands | 3–5 |
| 3–5 | System Messages | 3–6 |
| 5–1 | MT–3 Troubleshooting | 5–5 |
| 6–1 | Replaceable Parts List Index | 6–1 |


## LIST OF ILLUSTRATIONS


| FIGURE NO. | DESCRIPTION | PAGE NO. |
|---|---|---|
| 1–1 | Multiple Transmitter Interface | 1–1 |
| 2–1 | Configuration A. Telephone Line Periodic or Constant Communication | 2–3 |
| 2–2 | Configuration B. RF Link Constant Communication | 2–5 |
| 2–3 | Configuration C. RF and SCA Link Constant Communication | 2–7 |
| 2–4A | Configuration D. Direct Connection or Constant Communication | 2–9 |
| 2–4B | Configuration E. 2–Wire Modem or Constant Communication | 2–11 |
| 2–5 | Cage–Clamp Connection Installation Diagram | 2–13 |
| 2–6 | TB1 Control Relay Output Connections | 2–15 |
| 2–7 | TB2 Analog and Status Input Connections | 2–16 |
| 2–8 | Logic Circuit Board Switch Programming | 2–17 |
| 2–9 | Definition Screen | 2–18 |
| 3–1 | MT–3 Indicators | 3–1 |
| 3–2 | Interface Screen | 3–3 |
| 3–3 | Interface Control Mode Screen | 3–5 |
| 4–1 | MT–3 Simplified Schematic Diagram | 4–3 |
| 4–2 | Power Supply Simplified Schematic | 4–9 |
| 5–1 | Controls and Test Points | 5–3 |
| 5–2 | MT–3 Fuse Link Location | 5–4 |


This equipment is a Class A (or Class B) digital apparatus which complies with the Radio Interference Regulations, CRC c.1374.



BE BROADCAST ELECTRONICS INC

# SECTION I
# GENERAL INFORMATION

## 1–1. INTRODUCTION.

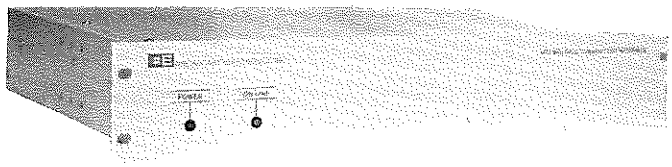
1–2. The information presented in this section provides a general description of the Broadcast Electronics MT–3 multiple transmitter interface and lists equipment specifications.

## 1–3. EQUIPMENT DESCRIPTION.

1–4. The MT–3 multiple transmitter interface is a remote transmitter control interface which operates in association with the RC–1 MVDS remote control system (refer to Figure 1–1). Designed with a Z84C00 microprocessor, the MT–3 will control two MVDS equipped transmitters and one non–MVDS transmitter.

1–5. Operation of the MT–3 is entirely controlled by a system program which eliminates the necessity for external controls. Individual transmitter control is accomplished by the operator with keyboard commands from a remote personal computer system.

1–6. The multiple transmitter interface contains a logic circuit board, an input/output circuit board, a relay circuit board, and a power supply. Ribbon cables provide interconnections between circuit boards for maximum reliability. For ease of maintenance, both the top and bottom covers are removable.



COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597–0122–20

FIGURE 1–1. MULTIPLE TRANSMITTER INTERFACE

1–7. The multiple transmitter interface is available in one configuration as follows:

| MODEL NO. | PART NUMBER | DESCRIPTION |
|---|---|---|
| MT–3 | 909–0127–004 | Multiple transmitter interface, rack mount, 120V or 240V ac, 50/60 Hz. |

## 1–8. OPTIONS AND ACCESSORIES.

1–9. The following is a list of the available accessories for the MT–3 multiple transmitter interface.

| PART NUMBER | DESCRIPTION |
|---|---|
| 979–0080–004 | 100% SEMICONDUCTOR SPARE PARTS KIT. |
| 979–0081–004 | RECOMMENDED SEMICONDUCTOR SPARE PARTS KIT. |

1–10. **SENSING EQUIPMENT.**

1–11. Refer to Table 1–1 for external sensing equipment available for interfacing with the MT–3.

**TABLE 1–1. SENSING EQUIPMENT**

| MODEL | PART NUMBER | DESCRIPTION |
|---|---|---|
| CSA–01 | 809–4032 | TFT chopper amplifier provides isolation from a floating circuit to a grounded circuit with dc gain. |
| PLC–01 | 809–4058 | TFT power to linear converter provides linear power information from a log scale to a linear scale. |
| TLK–01 | 809–4031 | TFT tower light monitor provides a sample of ac line current. |
| LVK–01 | 809–4029 | TFT line voltage monitor provides a sample of ac line voltage. |
| PVK–01 | 809–4028 | TFT plate voltage monitor provides a sample of plate voltage up to 20 kV. |
| TSK–01 | 809–4023 | TFT temperature sensing monitor provides a sample of air or component temperature. |
| MBB–01 | 809–4024 | TFT plate current monitor provides a sample of plate current or plate voltage up to 10 kV. |
| LVK–3 | 809–4055 | Moseley line voltage monitor provides a sample of ac line voltage. |
| MBB–1 | 809–4056 | Moseley universal plate circuit provides a sample of plate voltage or plate current. |
| RFK–1 | 809–4054 | Moseley transmission line monitor provides a sample of the AM RF signal. |
| RFK–2 | 809–4053 | Moseley 3 1/8 inch transmission line monitor provides a sample of the FM RF signal. |
| RFK–3 | 809–4052 | Moseley 1 5/8 inch transmission line monitor provides a sample of the FM RF signal. |
| RMK–1 | 809–4051 | Moseley reversible motor with an adjustable clutch. |
| TLK–2 | 809–4050 | Moseley tower light monitor provides a sample of ac current. |
| TSK–4 | 809–4057 | Moseley temperature sensing monitor provides a sample of air or component temperature. |

## 1–12. EQUIPMENT SPECIFICATIONS.

1–13. Refer to Table 1–2 for electrical characteristics or Table 1–3 for physical characteristics of the multiple transmitter interface.

**TABLE 1–2. MT–3 ELECTRICAL CHARACTERISTICS**

| PARAMETER | SPECIFICATIONS |
|---|---|
| POWER REQUIREMENTS | 120V or 240V ac, 50/60 Hz. |
| MEMORY: | |
| RAM MEMORY | 2 K bytes. Temporary storage for microprocessor operation. |
| ROM MEMORY | 8 K bytes. Permanent storage for system operating program. |
| COMMUNICATION PORTS | Three RS–232 ports. |
| STATUS INPUT CIRCUITS | 8 Status input channels, RFI filtered. |
| ANALOG INPUT CIRCUITS | 8 Analog input channels, EMI filtered. |
| RELAYS: | |
| CONTROL | 16 Output control relays, SPST. Contacts rated at 120V ac at 1 Ampere. |
| FAIL–SAFE | 1 Fail–safe relay, SPST. Contacts rated at 120V ac at 1 Ampere. |

**TABLE 1–3. MT–3 PHYSICAL CHARACTERISTICS**

| PARAMETER | SPECIFICATIONS |
|---|---|
| DIMENSIONS: | |
| WIDTH | 19 Inches (48.26 cm). |
| HEIGHT | 3.5 Inches (8.90 cm). |
| DEPTH | 15.875 Inches (40.32 cm). |
| WEIGHT | 14 Pounds (6.32 kg). |
| AMBIENT TEMPERATURE | +14 F to 122 F (–10 C to +50 C). |
| MAXIMUM HUMIDITY | 95% Non–condensing. |
| MAXIMUM ALTITUDE | 0 to 10,000 feet above sea level (0 to 3048 meters). |

# SECTION II
# INSTALLATION

## 2–1. INTRODUCTION.

2–2. This section contains information required for installation of the Broadcast Electronics MT–3 multiple transmitter interface.

## 2–3. UNPACKING.

2–4. The equipment becomes the property of the customer when the equipment is delivered to the carrier. Carefully unpack the following equipment:

A. MT–3 Multiple Transmitter Interface.

B. MT–3 Accessory Kit.

C. Modem Interface Cable Assembly.

2–5. Perform a visual inspection to determine that no apparent damage has been incurred during shipment. All shipping materials should be retained until it is determined that the equipment has not been damaged. Claims for damaged equipment must be promptly filed with the carrier or the carrier may not accept the claim.

2–6. The contents of the shipment should be as indicated on the packing list. If the contents are incomplete, or the equipment is damaged electrically or mechanically, notify both the carrier and Broadcast Electronics, Inc.

## 2–7. INSTALLATION.

2–8. Prior to installation of the MT–3, refer to RC–1 SECTION II, INSTALLATION, in this manual and perform the following procedures for the RC–1 MVDS remote control system as required:

A. SWITCH AND JUMPER PROGRAMMING CHECK.

B. SELECTING BAUD RATES.

C. MEMORY CIRCUIT BOARD INSTALLATION.
(For RC–1 field installation kits only.)

### 2–9. PLACEMENT.

2–10. The MT–3 requires 3.5 inches (8.90 cm) of a standard 19 inch rack cabinet and may be mounted in any convenient location within reach of control and power cables. An additional one inch of rack space above and below the unit should be provided for adequate ventilation. The unit should not be mounted directly above or below heat–generating equipment.

2–11. Placement of the MT–3 in relation to the transmitter(s) is determined by the application. If the MT–3 will control only MVDS equipped transmitters, it is recommended the unit be installed within 500 feet of either MVDS. If the MT–3 will control MVDS equipped transmitters and a non–MVDS transmitter (or other equipment), it is recommended the unit be installed near the non–MVDS equipment.

2–12. **COMMUNICATION EQUIPMENT CONNECTIONS.**

2–13. The MT–3 will operate with various remote communication systems. The following information and Figures 2–1 through 2–4 illustrate typical multiple transmitter interface installations.

2–14. **CONFIGURATION A.** The primary remote communication system incorporates a telephone line and a dial–up modem installed at the transmitter and studio sites. To install a modem at the transmitter site, connect the modem interface cable (supplied) between MT–3 rear–panel port J1 and the appropriate receptacle on the modem.

2–15. **CONFIGURATION B.** This configuration incorporates a 4–wire modem and STL equipment installed at the transmitter and studio sites. To install a 4–wire modem at the transmitter site, connect the modem interface cable (supplied) between MT–3 rear–panel port J1 and the appropriate receptacle on the modem.

2–16. **CONFIGURATION C.** This configuration incorporates a 4–wire modem and SCA/STL equipment installed at the transmitter and studio sites. To install a 4–wire modem at the transmitter site, connect the modem interface cable (supplied) between MT–3 rear–panel port J1 and the appropriate receptacle on the modem.

2–17. **CONFIGURATION D.** This configuration incorporates a direct connect (RS–232) system which can be implemented when the distance between the transmitter MVDS and computer system is within 500 feet. To install the direct connect system, refer to Figure 7–11B in SECTION VII, DRAWINGS, and fabricate a cable as shown. Connect this cable between MT–3 rear–panel port J1 and the appropriate RS–232 communication port on the computer system.

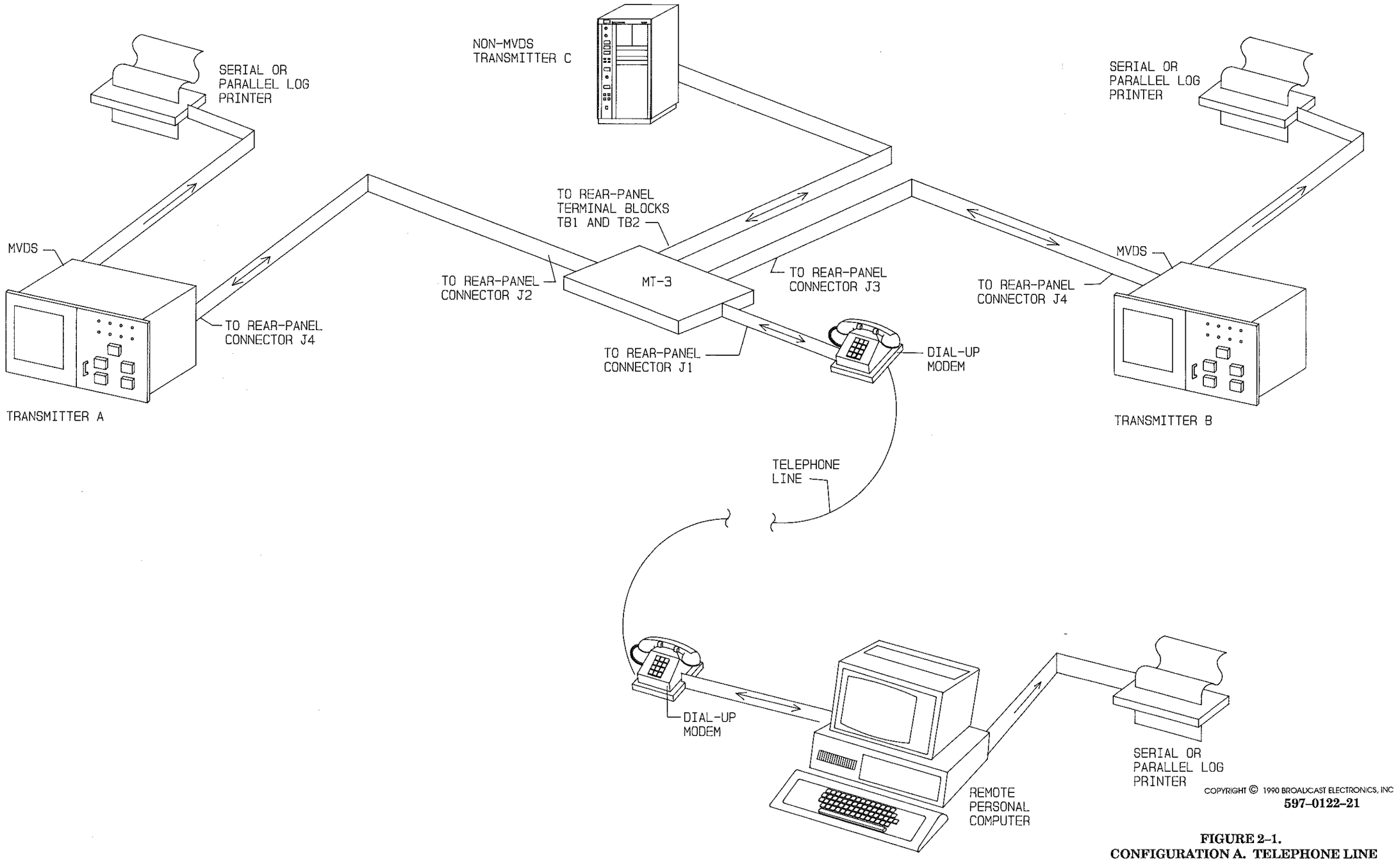
2–18. **CONFIGURATION E.** This configuration incorporates a 2–wire modem and a leased line from a telephone company. To install a 2–wire modem at the transmitter site, connect the modem interface cable (supplied) between MT–3 rear–panel port J1 and the appropriate receptacle on the modem.

2–19. **TRANSMITTER CONNECTIONS.**

2–20. The MT–3 will interface with and control two MVDS equipped transmitters and one non–MVDS transmitter. Proper operation requires the MT–3 be connected to at least one MVDS equipped transmitter.

2–21. **MVDS EQUIPPED TRANSMITTERS.** To interface the MT–3 with transmitter A or transmitter B: 1) locate the MT–3 to MVDS cable in the accessory kit and 2) refer to Figure 7–11A in SECTION VII, DRAWINGS and fabricate a MT–3 to PC interface cable if required. For transmitter A, connect a cable between port J4 on the rear–panel of the transmitter controller and MT–3 rear–panel port J2. For transmitter B, connect a cable between port J4 on the rear–panel of the transmitter controller and MT–3 rear–panel port J3.

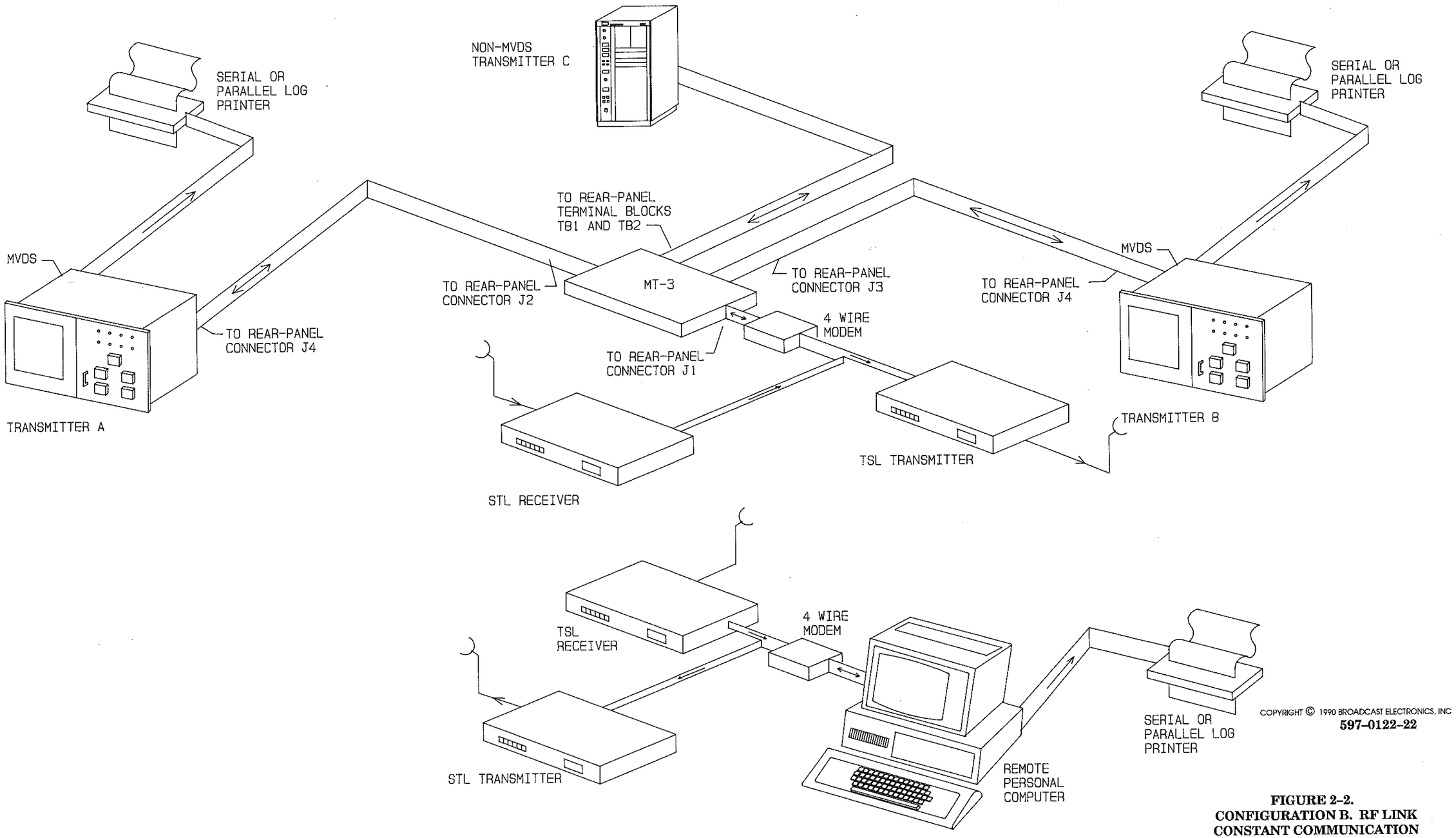
2–22. **NON–MVDS TRANSMITTER.** To connect the MT–3 to a non–MVDS transmitter, two cage–clamp terminal blocks are provided on the MT–3 rear–panel. Figure 2–5 presents installation information for connections to cage–clamp terminal blocks. Refer to Figure 2–5 as required for the following information.




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

**597-0122-21**

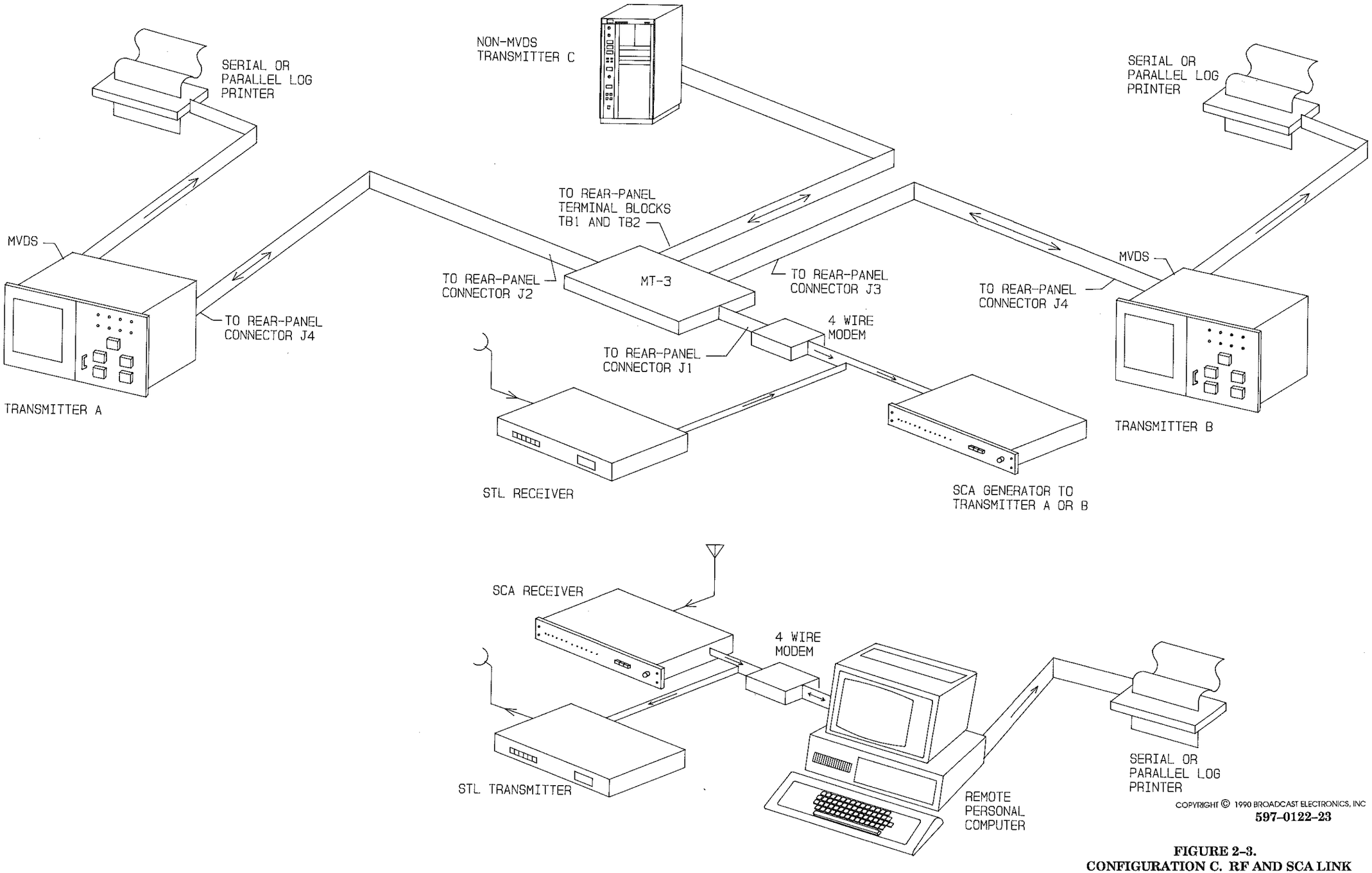
**FIGURE 2–1.**
**CONFIGURATION A. TELEPHONE LINE**
**PERIODIC OR CONSTANT COMMUNICATION**




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

**597-0122-22**

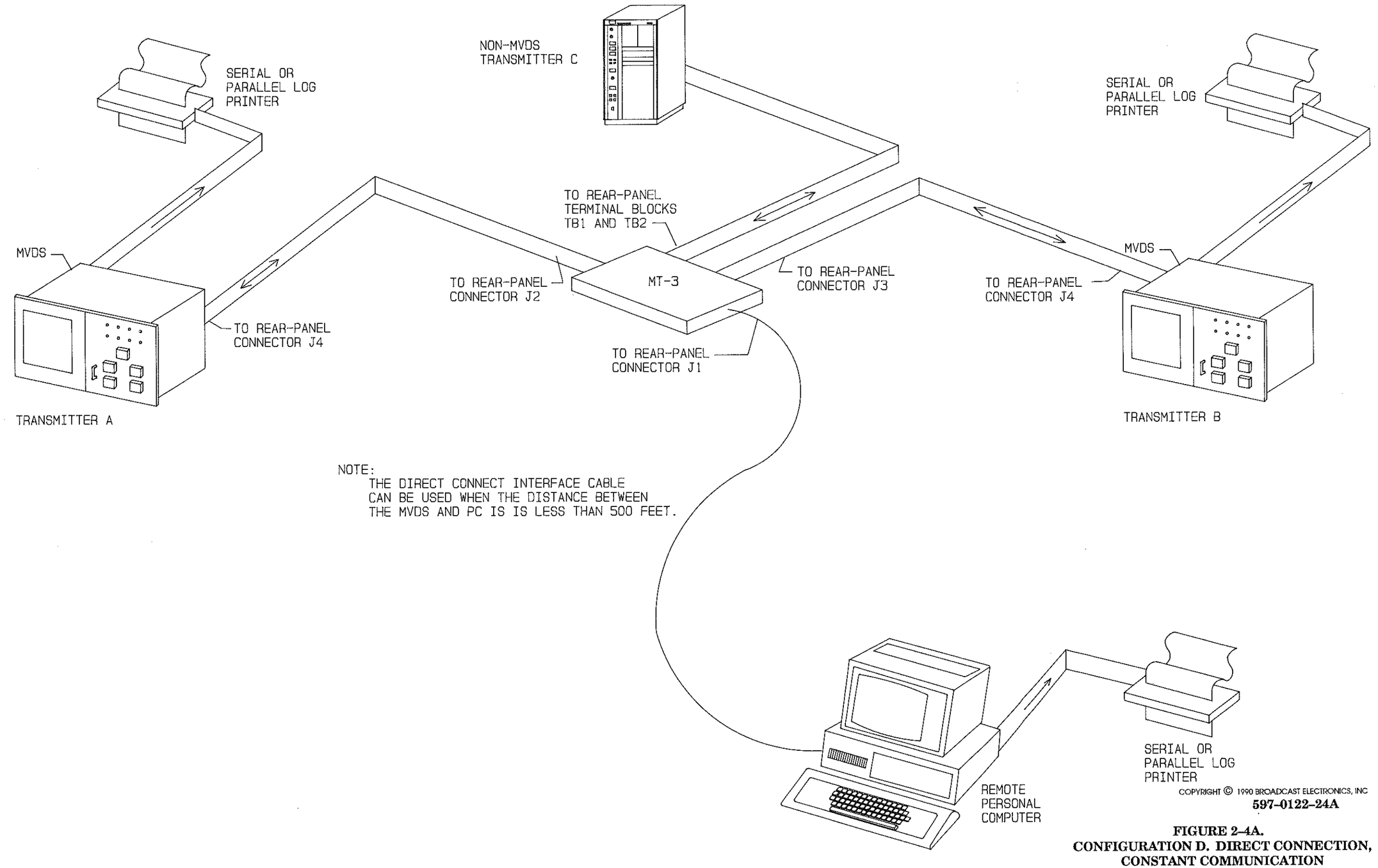
**FIGURE 2-2.**
**CONFIGURATION B. RF LINK**
**CONSTANT COMMUNICATION**




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

**597-0122-23**

**FIGURE 2–3.**
**CONFIGURATION C. RF AND SCA LINK**
**CONSTANT COMMUNICATION**

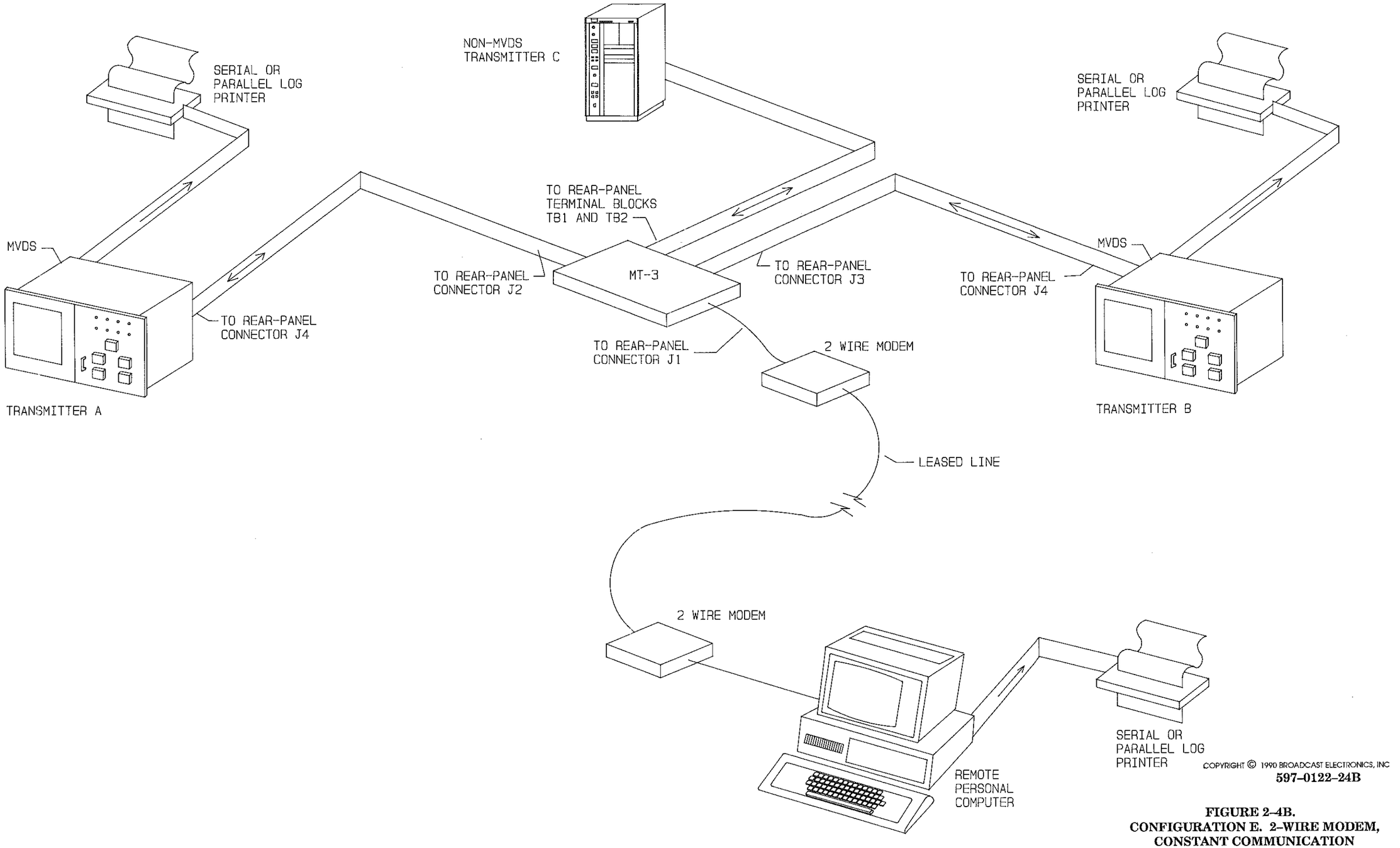



NOTE:
THE DIRECT CONNECT INTERFACE CABLE
CAN BE USED WHEN THE DISTANCE BETWEEN
THE MVDS AND PC IS IS LESS THAN 500 FEET.

COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

**597-0122-24A**

**FIGURE 2-4A.**
**CONFIGURATION D. DIRECT CONNECTION,**
**CONSTANT COMMUNICATION**



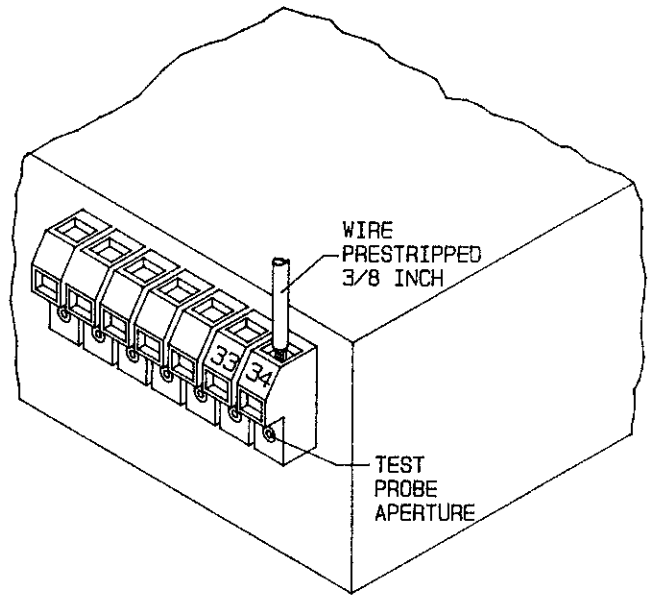

COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

**597-0122-24B**

**FIGURE 2-4B.**
**CONFIGURATION E. 2-WIRE MODEM,**
**CONSTANT COMMUNICATION**

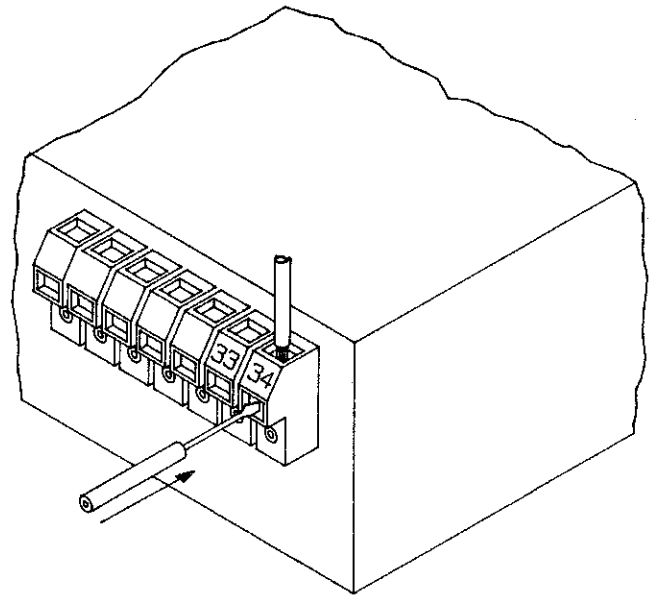
STEP 1

INSERT PRESTRIPPED WIRE INTO TERMINAL.



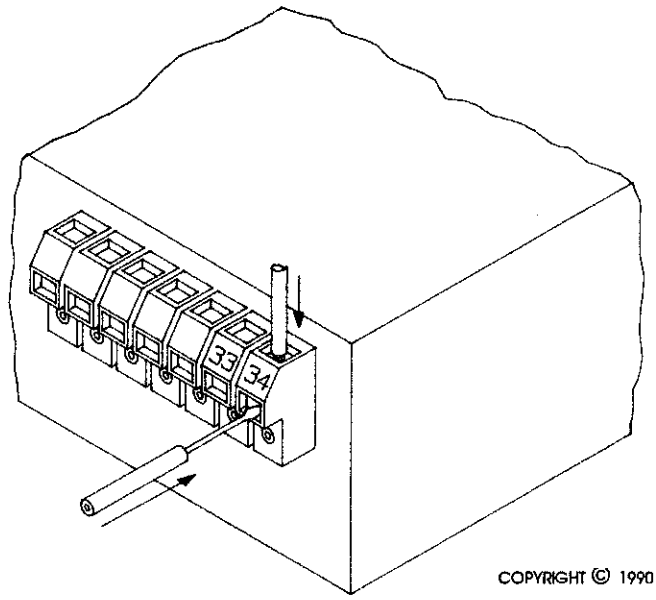

STEP 2

INSERT SCREWDRIVER AND APPLY INWARD PRESSURE.




STEP 3

PUSH WIRE INTO EXPANDED CAGE-CLAMP.




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597-0122-25

**FIGURE 2–5. CAGE-CLAMP CONNECTION INSTALLATION DIAGRAM**

2–23. MT–3 rear–panel terminal block TB1 provides 17 control relay output connections including fail–safe relay K17. The contacts of control relays K1 through K17 are rated at 120V at 1 ampere. Depending on system programming, relays K1 through K16 can be operated in the following configurations.

1. Normally open and latching.
2. Normally closed and latching.
3. Normally open and momentary.
4. Normally closed and momentary.

2–24. Control relays K8 and K16 are configured as normally closed when power is initially applied to the MT–3. Relays K1 through K7 and K9 through K15 are configured as normally opened. Refer to Figure 2–6 and connect the transmitter control circuits to TB1 as required.

2–25. MT–3 rear–panel terminal block TB2 provides connections for 8 unbalanced analog input channels which will accept an input level of –5V to +5V dc. Refer to Figure 2–7 and connect the transmitter analog input circuits to TB2 as required.

2–26. MT–3 rear–panel terminal block TB2 also provides connections for 8 status input channels. Refer to Figure 2–7 and connect the transmitter status input circuits to TB2 as required.

2–27. **SWITCH PROGRAMMING CHECK.**

2–28. Switch S1 on the logic circuit board selects the MT–3 operating parameters. To access S1, remove the bottom–panel. When programming is completed, replace the panel.

2–29. **SYSTEM OPERATION.** Refer to Figure 2–8 and ensure S1B is operated to the OFF position for system operation.

2–30. **CARRIER DETECT.** Switches S1C and S1D select the logic polarity of the carrier detect signal. For normal carrier signal, the position of these switches will be as shown in Figure 2–8. If inversion of the carrier signal is required, reverse the positions of both S1C and S1D.

2–31. **BAUD RATE.** Switch S1A selects the baud rate between the MT–3 and modem. Refer to Figure 2–8 and select the appropriate baud rate.

2–32. **PROGRAMMING THE MODEMS.**

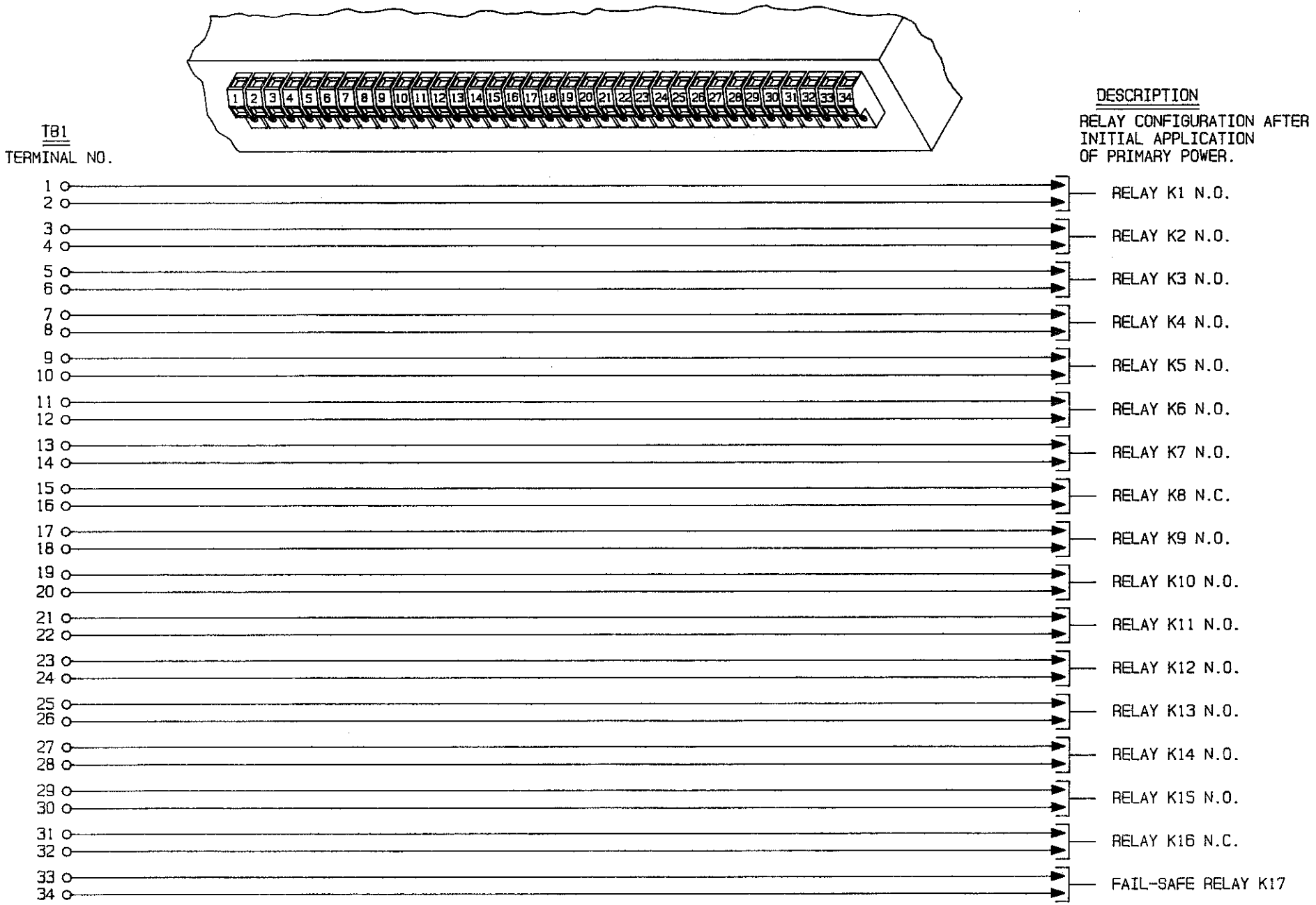
2–33. **DIAL–UP MODEMS.** To program dial–up modems, refer to PROGRAMMING DIAL–UP MODEMS in RC–1 SECTION II, INSTALLATION, in this manual.

2–34. **4–WIRE MODEMS.** To program 4–wire modems, refer to PROGRAMMING 4–WIRE MODEMS in RC–1 SECTION II, INSTALLATION, in this manual.

2–35. **2–WIRE MODEMS.** To program 2–wire modems, refer to PROGRAMMING 2–WIRE MODEMS in RC–1 SECTION II, INSTALLATION, in this manual.

2–36. **SYSTEM OPERATING PROGRAM INSTALLATION.**

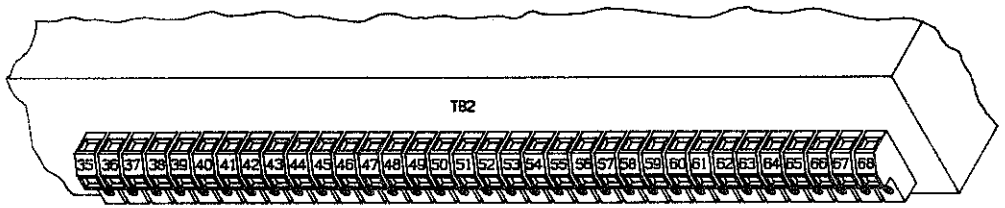
2–37. If the MT–3 is a retrofit kit, the transmitter MVDS must be instructed to accept an MT–3. Refer to RC–1 INSTALLATION, SECTION II, in this manual and perform the INSTALLATION PROCEDURE.




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

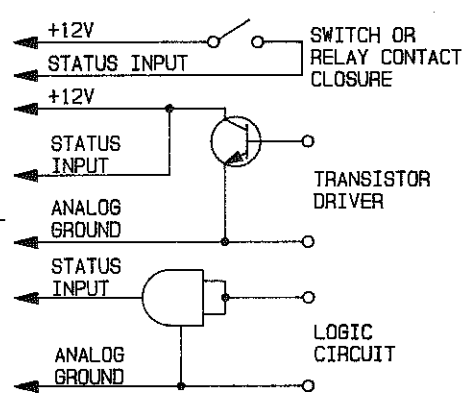
597-0122-26

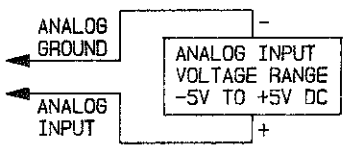
**FIGURE 2-6. TB1 CONTROL RELAY OUTPUT CONNECTIONS**




| TB2 TERMINAL NO. | DESCRIPTION |
|---|---|
| 68 | +12V |
| 67 | STATUS INPUT 1 |
| 66 | +12V |
| 65 | STATUS INPUT 2 |
| 64 | +12V |
| 63 | STATUS INPUT 3 |
| 62 | +12V |
| 61 | STATUS INPUT 4 |
| 60 | +12V |
| 59 | STATUS INPUT 5 |
| 58 | +12V |
| 57 | STATUS INPUT 6 |
| 56 | +12V |
| 55 | STATUS INPUT 7 |
| 54 | +12V |
| 53 | STATUS INPUT 8 |
| 52 | ANALOG GROUND |
| 51 | ANALOG INPUT 1 |
| 50 | ANALOG GROUND |
| 49 | ANALOG INPUT 2 |
| 48 | ANALOG GROUND |
| 47 | ANALOG INPUT 3 |
| 46 | ANALOG GROUND |
| 45 | ANALOG INPUT 4 |
| 44 | ANALOG GROUND |
| 43 | ANALOG INPUT 5 |
| 42 | ANALOG GROUND |
| 41 | ANALOG INPUT 6 |
| 40 | ANALOG GROUND |
| 39 | ANALOG INPUT 7 |
| 38 | ANALOG GROUND |
| 37 | ANALOG INPUT 8 |
| 36 | ANALOG GROUND |
| 35 | ANALOG GROUND |

CIRCUIT APPLICATION

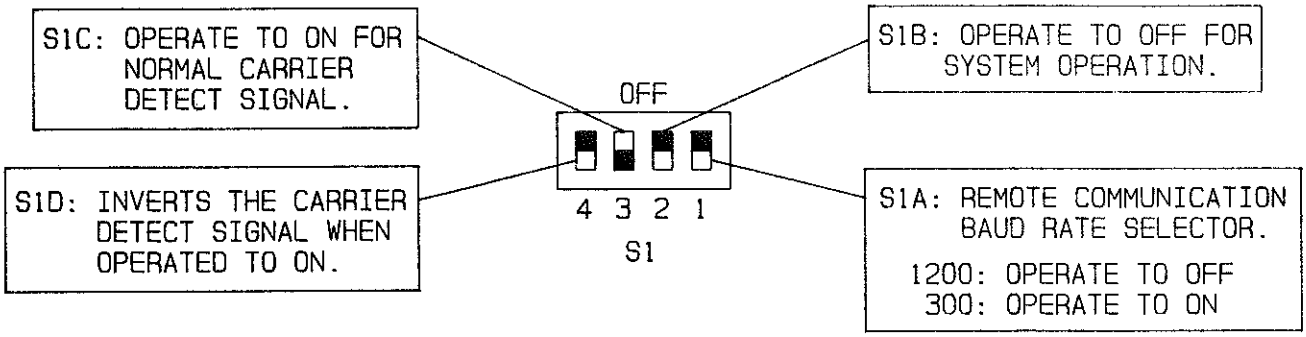



COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597-0122-27

FIGURE 2-7. TB2 ANALOG AND STATUS INPUT CONNECTIONS




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC
597-0122-28

**FIGURE 2–8. LOGIC CIRCUIT BOARD SWITCH PROGRAMMING**

## 2–38. PROGRAMMING THE DEFINITION SCREEN.

2–39. The definition screen is used when the MT–3 is interfaced with a non–MVDS transmitter. This screen allows the operator to assign titles and parameters for 8 analog input channels, 8 status input channels, and 16 output control relays.

2–40. Access to the definition screen is only required if modification of titles and/or parameters is desired. The definition screen information will be stored on disk and displayed during the interface screen as required. Refer to Figure 2–9 and Table 2–1 for a description of the definition screen.

2–41. To program the definition screen, operation of the MT–3 will be required. All standard operating procedures for the RC–1 are applicable to the MT–3. Therefore, refer to OPERATION, RC–1 SECTION III in this manual and learn the operating procedures. To access and program the definition screen, proceed as follows:

A. Contact an MVDS transmitter using the dial operation. A normal display screen will appear on the monitor.

B. Depress the I key. After a brief duration, an MT–3 screen will be displayed.

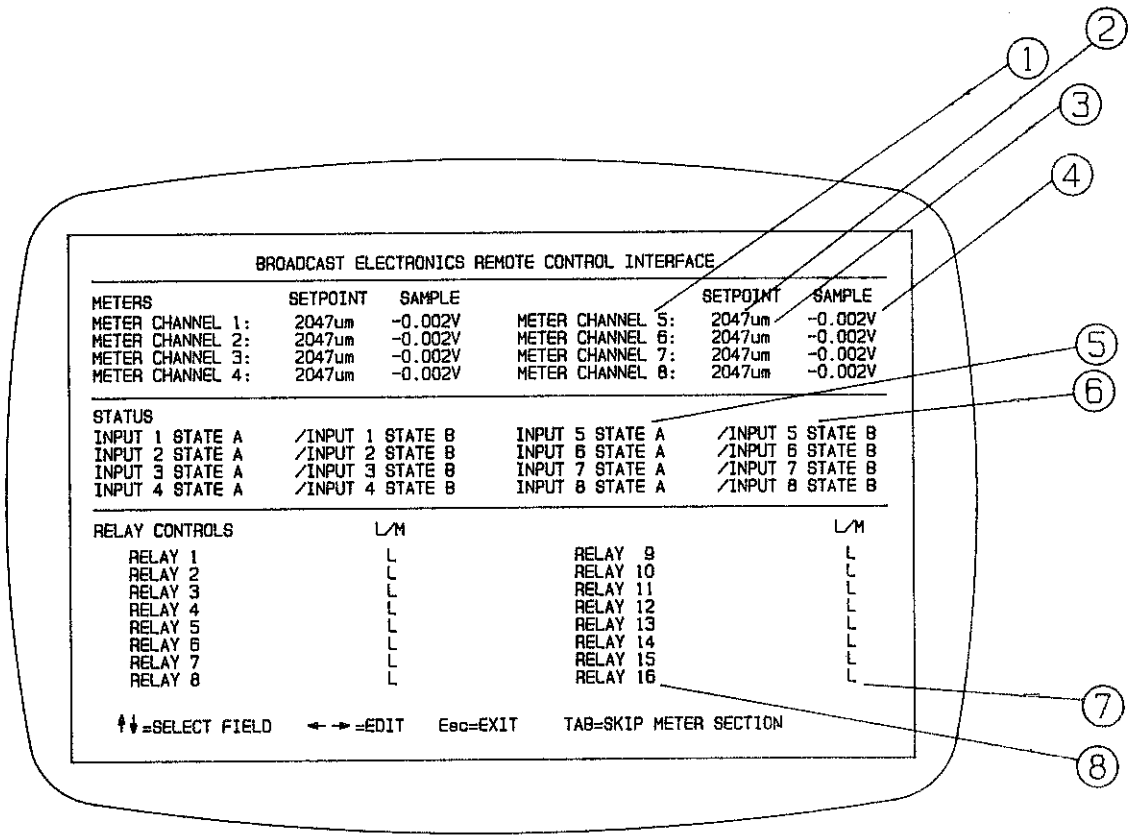
C. Depress the D key. The following message will be displayed.

ENTER PASSWORD " "

D. Enter the 8 character configuration/definition password and depress the RETURN key. (The factory default password is 12345678.) The definition screen will be displayed as shown in Figure 2–9.

E. Enter information into the meters field by performing the following procedure. If the entry of information into the meters field is not required, depress the TAB key. The cursor will advance to the status field.

1. Refer to Figure 2–9 and enter the desired title information for an analog input channel (Examples: PLATE CURRENT, PLATE VOLTAGE).
2. Depress the ⇓ key.
3. Refer to Table 2–1 and enter the setpoint information as required.
4. Depress the ⇓ key.




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

**597-0122-34**

**FIGURE 2-9. DEFINITION SCREEN**

5. Enter the appropriate unit of measure (Examples: KV, or MA).
6. Depress the ⇓ key and repeat steps 1 through 5 for each meter analog channel as required.

F. Enter information into the status field as follows:

1. Operate the ⇓ key and advance to the desired input status field. Titles may be entered for a state A condition and state B condition, or either title may be omitted for enhancement.
2. Enter a title for input condition A if required.
3. Depress the ⇓ key.
4. Enter a title for input condition B if required.
5. Depress the ⇓ key and repeat steps 1 through 4 for each status field as required.

G. Enter information into the relay controls field as follows:

1. Operate the ⇓ key and advance to the desired control relay title field.

2. Enter the desired control relay title.

3. Depress the ⇓ key.

4. Refer to Table 2–1 and enter the relay mode of operation. If momentary open operation is required for a relay which is initially latched open, the relay must first be operated to the latched closed condition. For a momentary open relay operation, proceed as follows:

   a. Depress the escape key to exit the definition screen and access the interface screen (refer to Figure 3–2 in SECTION III, OPERATION).

   b. Depress the T key to access the control mode.

   c. Depress the appropriate function key to operate the desired relay to the latched closed condition.

   d. Depress the D key to re–enter the definition screen and the TAB key to jump to the status field. Operate the ⇓ to advance to the desired relay mode field and depress the M key.

5. Depress the ⇓ and repeat steps 1 through 4 for each control relay as required.

H. Depress the escape (ESC) key.

## TABLE 2–1. DEFINITION SCREEN

| INDEX NUMBER | DESCRIPTION |
|---|---|
| 1 | Title field for an analog input channel, 15 character limit (example: PLATE VOLTAGE). |
| 2 | Setpoint field scales an analog input sample voltage to represent an actual value by positioning a decimal point, 7 digit limit including the decimal.<br><br>When entering analog setpoints, ensure the sample input potentials are at the desired levels prior to accessing the definition screen.<br><br>Example: A 5.00 volt sample which represents a plate voltage of 10 kV is connected to analog input channel 1. The setpoint may be entered as follows.<br><br>**SAMPLE VOLTAGE** — **SETPOINT** — **ACTUAL VALUE**<br>5.00 V — 010000 — 10,000V<br>OR<br>5.00 V — 00010.0 — 10.0 kV<br><br>A negative potential requires a – sign as the first entry, leading zeros must be substituted for spaces (example: 0010.00 –050.00 or 0003000). |
| 3 | Unit of measure field, 2 character limit (examples: KV, MV, A, or MA). |
| 4 | Displays an analog input sample potential which is applied to a rear–panel connection. This value is static during the definition screen display. |
| 5 | Status input condition A field, 19 character limit (example: for input 1, INCREASE XMTR POWER). If the condition on status input 1 occurs, the INCREASE XMTR POWER message will be displayed to indicate the condition. |
| 6 | Status input condition B field, 19 character limit (example: for input 1, DECREASE XMTR POWER). If the condition on status input 1 is the opposite of the previous condition, the DECREASE XMTR POWER message will be displayed to indicate the condition. |
| 7 | Relay mode of operation field, 1 character limit, L = latching, M = momentary (example: L). |
| 8 | Relay title field for an output control relay, 16 character limit (example: BACKUP XMTR H.V.). |

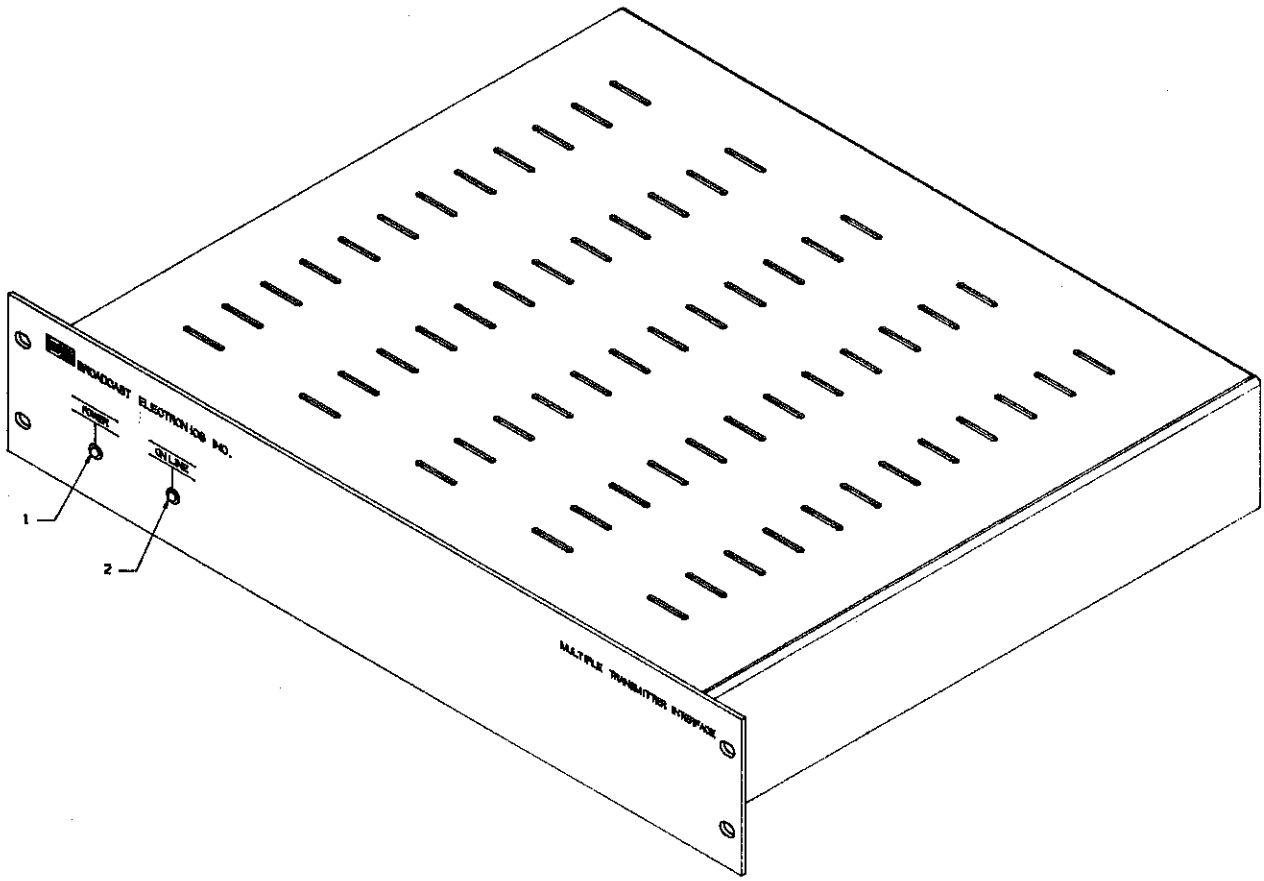
# SECTION III
# OPERATION

## 3–1. INTRODUCTION.

3–2. This section provides standard operating procedures for the MT–3 multiple transmitter interface.

## 3–3. MT–3 INDICATORS.

3–4. Refer to Figure 3–1 for the location of the indicators associated with normal operation of the MT–3 multiple transmitter interface. The function of each indicator is described in Table 3–1.




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597–0122–50

FIGURE 3–1. MT–3 INDICATORS

TABLE 3–1. MT–3 INDICATORS

| INDEX NO. | NOMENCLATURE | FUNCTION |
|---|---|---|
| 1 | POWER | Indicates the application of primary power when illuminated. |
| 2 | ON LINE | Indicates contact is established between the remote and local sites when illuminated. |

## 3–5. OPERATION.

3–6. All standard operating procedures for the RC–1 MVDS remote control system are applicable to the MT–3 multiple transmitter interface. Therefore, refer to RC–1 SECTION III, OPERATION in this manual and learn the standard operating procedures.

*NOTE* *THE FOLLOWING PROCEDURE ASSUMES THAT THE MT–3 IS COMPLETELY INSTALLED AND IS FREE OF*

*NOTE* *ANY DISCREPANCIES.*

3–7. Apply primary power to the MT–3. The front–panel POWER indicator will illuminate. Except for maintenance reasons, primary power is assumed to be constantly applied.

### 3–8. CONTACT OPERATION.

3–9. Establish contact with a transmitter using the RC–1 DIAL operation. When contact is established, the front–panel ON LINE indicator will illuminate and the following screens will be available for each transmitter.

| MVDS TRANSMITTER A | MVDS TRANSMITTER B |
|---|---|
| Normal Display Screen | Normal Display Screen |
| Customer Configuration Screen | Customer Configuration Screen |

**NON–MVDS TRANSMITTER**

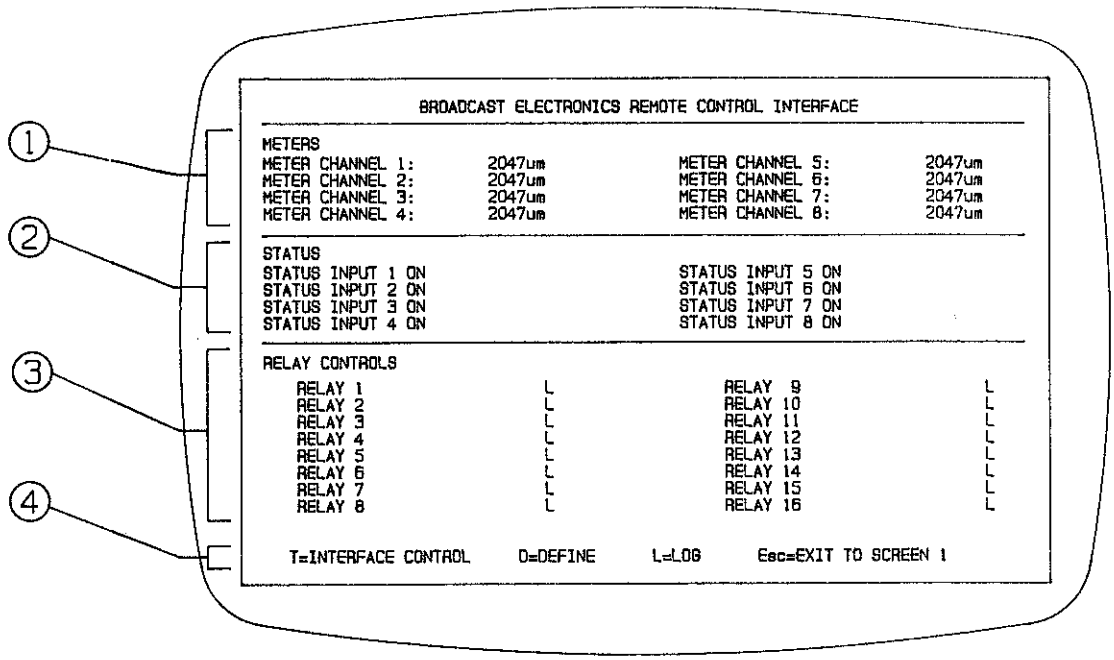
Interface Screen

Definition Screen

### 3–10. SELECTING A TRANSMITTER.

3–11. **MVDS TRANSMITTER.** To select the normal display screen for an alternate MVDS transmitter, depress the A key. The customer configuration screen and control operations for the associated transmitter are accessible from the normal display screen.

3–12. **NON–MVDS TRANSMITTER.** The interface screen for a non–MVDS transmitter can be accessed from either normal display screen. Refer to Figure 3–2 and Table 3–2 for a description of the interface screen. To access the interface screen, depress the I key.




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597-0122-29

**FIGURE 3–2. INTERFACE SCREEN**

**TABLE 3–2. INTERFACE SCREEN**

| INDEX NUMBER | DESCRIPTION |
|---|---|
| 1 | Displays current meter indications for eight meter input channels. |
| 2 | Displays current status for eight status input channels. |
| 3 | Displays sixteen output control relays and type of relay operations (L = latching, M = momentary). |
| 4 | Displays commands for the interface screen. |

## 3–13. INTERFACE SCREEN OPERATIONS.

3–14. Interface screen operations are executed from the keyboard. Refer to Table 3–3 for a description of the interface commands and special key functions.

TABLE 3-3. INTERFACE COMMANDS

| KEY | DESCRIPTION |
|---|---|
| ESC | Terminates the definition screen and returns to a normal display screen when depressed. |
| T | Accesses the interface control mode when depressed. |
| ⇑ ⇐<br>⇓ ⇒ | When the NUM LOCK LED is extinguished during the definition mode, the ⇑ and ⇓ keys select the previous and next field. The ⇐ and ⇒ keys select a character within a field.<br><br>When the ⇓ key is operated to advance through the meter field, a scaling operation is performed using the static sample potential and setpoint value. Therefore, ensure that the displayed sample potential is within acceptable limits prior to operating the ⇓ key. |
| L | Requests a log of the screen display on the studio printer when depressed. |
| D | Accesses the definition screen when depressed. |
| TAB | Executes a cursor jump from the meter channel field to the status input field when depressed. This key can be used to advance from the meter field to the status field if meter setpoints have previously been assigned. |

3–15. **INTERFACE CONTROL MODE.** The MT–3 contains sixteen output control relays which can be latched ON, latched OFF, or operated momentarily depending on previous programming. To access the interface control mode, proceed as follows:

3–16. Depress the T key. The function key symbol for each relay will be displayed in reverse video (refer to Figure 3–3).

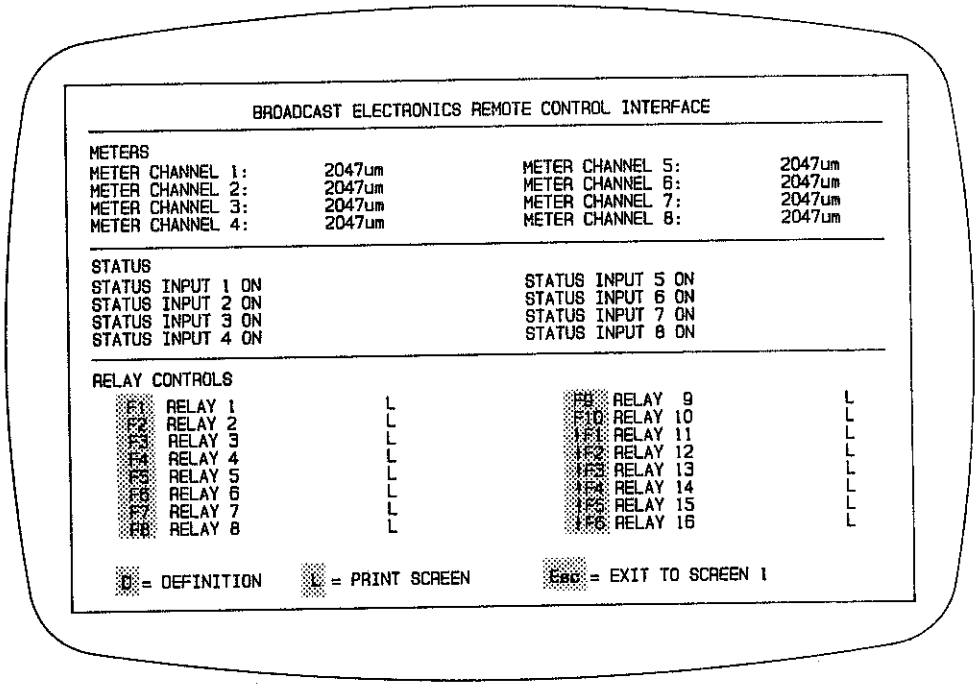
***NOTE***

***IF A FUNCTION KEY IS NOT DEPRESSED WITHIN 30 SECONDS, THE INTERFACE CONTROL MODE WILL BE AUTOMATICALLY TERMINATED.***

***NOTE***

3–17. To activate a control relay, refer to Table 3–4 and momentarily depress the appropriate function key. The function key symbol will flash and an ON message will appear to indicate the energized condition (for latching relay operation).

3–18. To deactivate a control relay, refer to Table 3–4 and momentarily depress the appropriate function key. The function key symbol will flash and the ON message will be blanked to indicate the deenergized condition (for latching relay operation).




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

**597-0122-65**

**FIGURE 3-3. INTERFACE CONTROL MODE SCREEN**

**TABLE 3-4. CONTROL MODE COMMANDS**

| KEY | DESCRIPTION |
|---|---|
| F1–F10 | Operates control relays 1 through 10 when depressed. |
| SHIFT + F1–F6 | Operates control relays 11 through 16 when the shift key is depressed with function keys F1 through F6. |

## 3–19. SYSTEM MESSAGES.

3–20. The system messages assigned to the RC–1 are also applicable to the MT–3. Therefore, refer to SYSTEM MESSAGES, SECTION III, OPERATION in PART I of this manual for a description of these messages. Refer to Table 3–5 for a description of additional messages which apply only to the MT–3.

TABLE 3–5. SYSTEM MESSAGES

| MESSAGE | DESCRIPTION |
|---|---|
| Alternate MVDS not responding, restoring original MVDS communication. | Displayed when alternate MVDS transmitter fails to acknowledge after the A key is depressed. |
| Check other MVDS transmitter, contact was requested. | Displayed when alternate MVDS transmitter requests contact. |
| Check selected MVDS transmitter, contact was requested. | Displayed when observing the interface screen and the selected MVDS transmitter requests contact. |

# SECTION IV
# THEORY OF OPERATION

## 4–1. INTRODUCTION.

4–2. This section presents the theory of operation for the Broadcast Electronics MT–3 multiple transmitter interface.

## 4–3. GENERAL DESCRIPTION.

4–4. The MT–3 consists of the following: 1) a logic circuit board, 2) input/output circuit board, 3) relay circuit board, and 4) a power supply.

### 4–5. LOGIC CIRCUIT BOARD.

4–6. The logic circuit board processes: 1) transmitter status and logging information to the studio site, and 2) transmitter control information from the studio site. Directed by instructions from a system operating program in memory, a central processing unit (CPU) controls three receiver/transmitter integrated circuits to provide remote communication and control for two MVDS equipped transmitters. In addition, the logic circuit board contains circuitry for controlling a non–MVDS transmitter.

### 4–7. INPUT/OUTPUT CIRCUIT BOARD.

4–8. The input/output (I/O) circuit board provides RFI filtering for eight transmitter status input circuits and EMI filtering for eight analog input circuits. This circuit board is provided for a non–MVDS transmitter.

### 4–9. RELAY CIRCUIT BOARD.

4–10. The relay circuit board provides control for a non–MVDS transmitter. This circuit board contains 16 relays (K1 through K16) for transmitter control functions. In addition, a fail–safe circuit is provided by relay K17.

### 4–11. POWER SUPPLY.

4–12. The power supply provides five regulated operating voltages. The +15V, –15V, +5V, and –5V regulators are located on the logic circuit board. The voltage regulator for the +12V supply is mounted on the chassis. All rectifier and filter components are located on a separate circuit board.

## 4–13. DETAILED DESCRIPTION.

### 4–14. LOGIC CIRCUIT BOARD.

4–15. The logic circuit board contains the transmitter control and communication processing circuitry. Refer to Figure 4–1 as required for discussion of the following circuits:

A. Central Processing Unit (CPU) Circuit

B. Clock Frequency Generator Circuit

C. Device Select Decoder Circuit

D. CPU Memory Circuit

E. Status Input and Control Circuit

F. Analog Input Circuit

G. Transmitter A and Transmitter B Communication Circuits

H. Remote Communication Circuit

I. Power–Up Preset Circuit

J. Address Monitor Circuit

4–16. **CPU CIRCUIT.** The CPU circuit contains a Z84C00 microprocessor which operates as the primary control device for the logic circuit board. The remaining circuitry on the logic circuit board assist in transferring information to and from memory or peripherals, and communicating to external devices.

4–17. The Z84C00 (Z80 CMOS version) is equipped with three output signals to indicate the current operational status. These signals synchronize various logic circuits to direct data as required by the microprocessor. Output signals memory request ($\overline{MREQ}$), read ($\overline{RD}$), and write ($\overline{WR}$) indicate the following functions:

A. The $\overline{MREQ}$ signal indicates an address is present on the address bus when logic LOW. The $\overline{MREQ}$ signal is routed to device select decoder circuit U12/U13 to enable the circuit.

B. The $\overline{RD}$ ($\overline{READ}$) signal indicates the microprocessor will transfer data from memory or peripherals when logic LOW. The $\overline{READ}$ signal is routed to CPU memory circuit U2 and U3, status input and control circuit U4, and analog input circuit U5.

C. The $\overline{WR}$ ($\overline{WRITE}$) signal indicates the microprocessor will transfer data to memory or peripherals when logic LOW. The $\overline{WRITE}$ signal is routed to CPU memory circuit U3, status input and control circuit U4, analog input circuit U5, transmitter A and transmitter B communication circuits U6 and U7, and remote communication circuit U8.

4–18. The microprocessor is equipped with sixteen active HIGH output address signals (A0 through A15). These signals connect the CPU with various logic circuits and operate as an address bus.

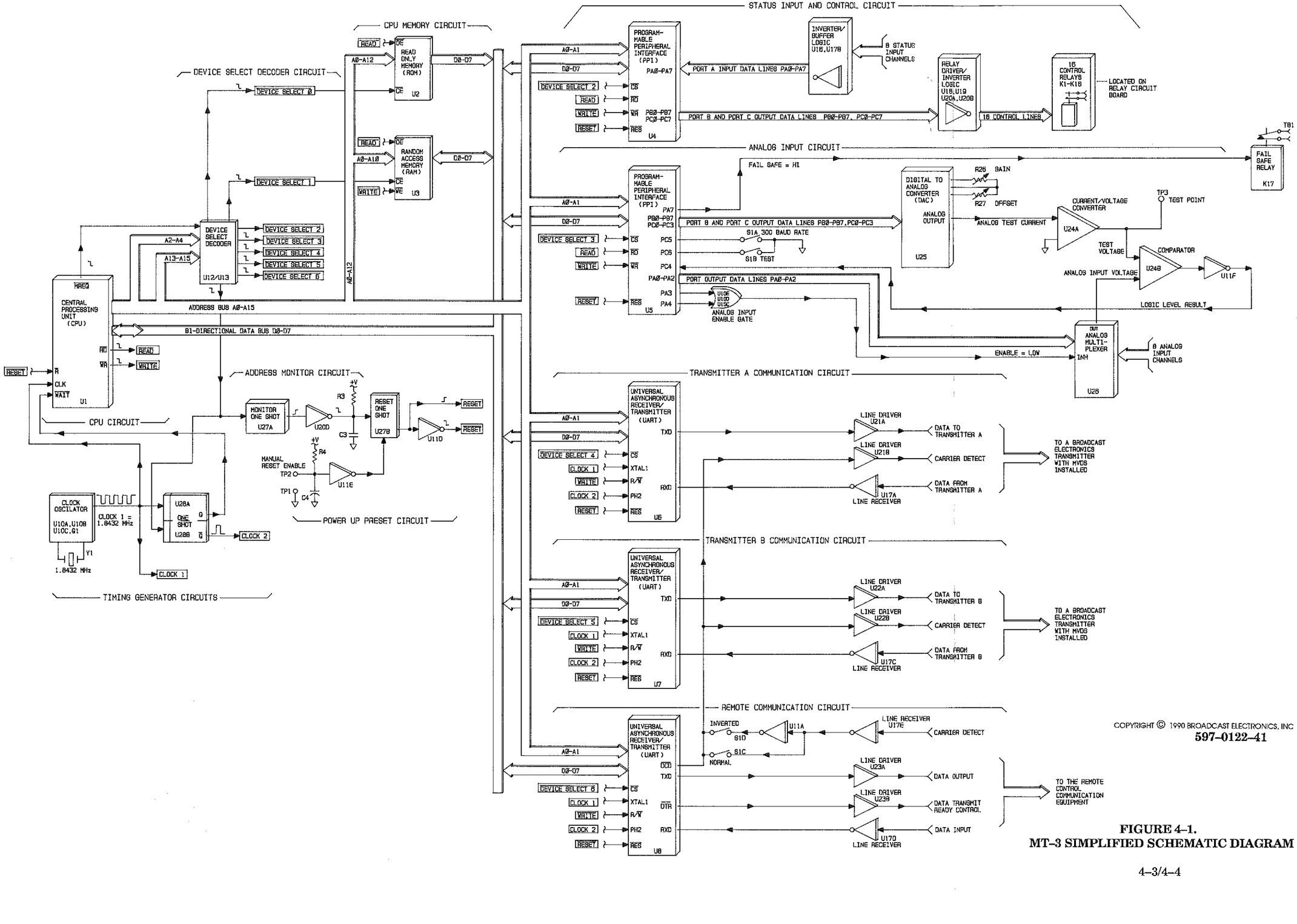
4–19. The microprocessor is also equipped with eight bidirectional signals (D0 through D7). These signals connect the CPU with various logic circuits and operate as a data bus. The data bus allows the CPU to route information to and from memory or peripherals.

4–20. **Read Operation.** During a read operation, the microprocessor will select a memory location or peripheral by presenting the appropriate address location on the address bus. The $\overline{READ}$ signal will go LOW to enable the selected device. The device will respond by presenting the required information on the data bus to be accessed by the CPU.

4–21. **Write Operation.** During a write operation, the microprocessor will select a memory location or peripheral by presenting the appropriate address location on the address bus, and the information on the data bus. The $\overline{WRITE}$ signal will go LOW to enable the selected device. The device will respond by accessing the required information from the data bus.

4–22. **TIMING GENERATOR CIRCUITS.** The timing generator circuits provide the operating signals for the CPU and universal asynchronous receiver/transmitter (UART) logic circuits. This circuitry consists of a clock oscillator and a dual one shot.

4–23. **Operation.** Components U10A, U10B, U10C, Q1, and Y1 operate as a crystal controlled oscillator with an output frequency (CLOCK 1) of 1.8432 MHz. CLOCK 1 is routed to CPU U1, UARTs U6, U7, U8, and the input of one shots U28A and U28B.




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

**597-0122-41**

**FIGURE 4-1.**
**MT-3 SIMPLIFIED SCHEMATIC DIAGRAM**

4–24. With clock 1 and a signal from device select decoder U12/U13, one shot U28B will generate a single pulse (clock 2) to the UARTs when a UART is addressed. This pulse is used by the UARTs to transfer data to or from the data bus.

4–25. With clock 1 and a signal from device select decoder U12/U13, one shot U28A will generate a wait signal to the CPU when a UART is addressed. The CPU will terminate processing until the UART data transfer operation is completed.

4–26. **DEVICE SELECT DECODER CIRCUIT.** Device select decoder circuit U12/U13 selects and enables a device for the microprocessor. Prior to a read/write operation, the CPU will present the address of the required device on the address bus, and the $\overline{\text{MREQ}}$ signal will go LOW.

4–27. **Operation.** When input signal $\overline{\text{MREQ}}$ is logic LOW, U12/U13 will decode the information on address input lines A2 through A4 and A13 through A15. If the address is valid, an output line will go LOW to select one of seven devices. The following list describes the output lines and valid addresses for each device.

| OUTPUT LINE | ADDRESS | DEVICE |
|---|---|---|
| DEVICE SELECT 0 | 0000–1FFF | ROM Memory U2 |
| DEVICE SELECT 1 | 2000–27FF | RAM Memory U3 |
| DEVICE SELECT 2 | 8000–8003 | Status Input and Transmitter Control Circuit U4 |
| DEVICE SELECT 3 | 8004–8007 | Analog Input Circuit U5 |
| DEVICE SELECT 4 | 8014–8017 | UART U6 |
| DEVICE SELECT 5 | 8018–801B | UART U7 |
| DEVICE SELECT 6 | 801C–801F | UART U8 |

4–28. The device select decoder circuit also provides an output line to address monitor circuit U27A. This line is pulsed LOW when logic circuits U4 through U8 are selected by the microprocessor.

4–29. **CPU MEMORY CIRCUIT.** The memory circuit provides both read only memory (ROM) and random access memory (RAM) for the CPU. ROM memory U2 contains the system operating program that can only be read by the microprocessor. However, RAM memory U3 can be read from or written to by the microprocessor.

4–30. **RAM Write Operation.** During a write operation, input lines $\overline{\text{WRITE}}$ and $\overline{\text{DEVICE SELECT 1}}$ will go LOW. U3 internally decodes the memory location on address lines A0 through A10. If the address is valid, U3 will access the information from the data bus.

4–31. **RAM Read Operation.** During a read operation, input lines $\overline{\text{READ}}$ and $\overline{\text{DEVICE SELECT 1}}$ will go LOW. U3 internally decodes the memory location on address lines A0 through A10. If the address is valid, U3 will present the information on the data bus to be accessed by the CPU.

4–32. **ROM Operation.** During a read operation, input lines $\overline{\text{READ}}$ and $\overline{\text{DEVICE SELECT 0}}$ will go LOW. U2 internally decodes the memory location on address lines A0 through A12. If the address is valid, U2 will present the information on the data bus to be accessed by the CPU.

4–33. **STATUS INPUT AND CONTROL CIRCUIT.** This circuit provides status input and control channels for a non–MVDS transmitter. The circuit consists of a programmable peripheral interface (PPI), inverter/buffer logic, relay driver/inverter logic, and 16 control relays.

4–34. PPI U4 is an input/output device with 24 I/O lines which are directed by the system operating program to function as input and/or output circuits. The 24 lines are divided into 3 ports and programmed as follows:

| PORT/DESIGNATION | | NUMBER OF LINES | DIRECTION |
|---|---|---|---|
| A | PA0–PA7 | 8 | Input |
| B | PB0–PB7 | 8 | Output |
| C | PC0–PC7 | 8 | Output |

4–35. **Status Input Operation.** Data lines PA0–PA7 route 8 transmitter status channels to the input of U4 through inverter/buffer logic U16 and U17B. During a read operation, input lines $\overline{\text{READ}}$ and $\overline{\text{DEVICE SELECT 3}}$, will go LOW. If the address is valid, U4 will respond by presenting port A status information on the data bus to be accessed and processed by the CPU.

4–36. **Relay Output Operation.** Output data lines PB0–PB7 and PC0–PC7 connect PPI U4 to 16 control relays through relay driver/inverter logic U18, U19, U20A, and U20B. When a relay is required to be energized, the CPU will present the appropriate information on the data bus. U4 input lines $\overline{\text{WRITE}}$ and $\overline{\text{DEVICE SELECT 3}}$ will go LOW. If the address is valid, U4 will access the information from the data bus.

4–37. U4 decodes the information and outputs a HIGH to port B or port C. This HIGH is inverted by relay driver/inverter logic U18, U19, U20A, or U20B to energize the appropriate relay (K1 through K16).

4–38. **ANALOG INPUT CIRCUIT.** This circuit provides analog input channels for a transmitter not equipped with an MVDS system. The circuit consists of a programmable peripheral interface (PPI), digital to analog converter (DAC) and associated circuitry, analog input multiplexer and associated circuitry, and a fail–safe circuit.

4–39. PPI U5 is an input/output device with 24 I/O lines which are directed by the system operating program to function as input and/or output circuits. The 24 lines are divided into 3 ports and programmed as follows:

| PORT/DESIGNATION | | NUMBER OF LINES | DIRECTION |
|---|---|---|---|
| A | PA0–PA4 | 5 | Output |
| A | PA5–PA6 | 2 | Not Used |
| A | PA7 | 1 | Output |
| B | PB0–PB7 | 8 | Output |
| C | PC0–PC3 | 4 | Output |
| C | PC4 | 1 | Input |
| C | PC5–PC6 | 2 | Input |
| C | PC7 | 1 | Not Used |

4–40. **Fail–Safe Operation.** Normally, the fail–safe relay is operated in the energized condition. If a fail–safe condition exists, the CPU will instruct PPI U5 to output a HIGH on line PA7 which deenergizes fail–safe relay K17.

4–41. **Switch Read Operation.** Switch S1 is a 4 pole dip switch on the logic circuit board. On power–up or a manual reset operation, the CPU will read PPI U5 input lines PC5 and PC6 which are connected to S1A and S1B respectively.

4–42. If S1A is closed (LOW), the CPU is instructed to operate the remote communication circuit at 300 baud rate. If S1B is closed (LOW), the CPU is instructed to execute a DAC gain and offset circuit calibration program.

4–43. **Analog Input Operation.** Output data lines PA0–PA2 connect PPI U5 to 8 analog input channels through analog multiplexer U26. Also, output lines PA3 and PA4 connect U5 to analog input enable gate U10E, U10D, and U15C. When an analog channel selection is required, the CPU will instruct U5 to access the appropriate information from the data bus.

4–44. U5 will decode the information and output an address on data lines PA0–PA2 to U26. U5 also outputs a LOW on PA3 or PA4 to the analog input enable gate which outputs a LOW to enable U26. If the address is valid, U26 will select and connect the appropriate analog channel to the input of comparator U24B.

4–45. **DAC Operation.** The digital to analog circuit consists of DAC U25, gain control R26, offset control R27, current/voltage converter U24A, comparator U24B, and inverter U11F. Output data lines PB0–PB7 and PC0–PC3 connect PPI U5 to DAC U25.

4–46. Prior to a DAC operation, the CPU will execute an analog input operation. U5 is then instructed to route 12 bits of test information to U25 through data lines PB0–PB7 and PC0–PC3. U25 decodes the information and outputs an analog test current to the input of U24A.

4–47. U24A will convert the test current to a test voltage which is applied to comparator U24B and test point TP3. U24B compares the test voltage with the analog input voltage and applies a logic level to inverter U11F.

4–48. U11F inverts the output of comparator U24B and applies a resultant logic level to U5 input line PC4. The CPU will request a read operation of input line PC4 and process the data to determine if the test sample voltage or the analog input voltage is greater. The CPU will repeat DAC operations until the digital equivalent value of the analog input voltage is established.

4–49. When the digital value is established, the CPU will store the test information in RAM memory. When required, the CPU will retrieve the information from RAM for transmission to the remote terminal.

4–50. **Gain and Offset Operation.** Gain control R26 and offset control R27 provide precise calibration of DAC U25 and current/voltage converter U24A. TP3 provides a monitoring test point during calibration.

4–51. **TRANSMITTER A AND TRANSMITTER B COMMUNICATION CIRCUITS.** Transmitter A communication circuit and transmitter B communication circuit provide control for two MVDS equipped transmitters. These circuits are identical in operation. Therefore, only transmitter A circuit will be discussed.

4–52. Transmitter A communication circuit consists of UART U6, line drivers U21A and U21B, and line receiver U17A. The UART transmit baud rate is derived from input signal CLOCK 1. The data transfer rate between the UART and CPU is derived from input signal CLOCK 2.

4–53. **Data Transmit Operation.** When a data transfer to transmitter A MVDS is required, the CPU will present the appropriate information on the data bus. U6 input lines $\overline{\text{WRITE}}$ and $\overline{\text{DEVICE SELECT 4}}$ will go LOW. If the address is valid, U6 will access the information from the data bus.

4–54. U6 output line TXD will serially transfer the information to line driver U21A. U21A converts this information from TTL signal level to RS–232 signal level to be received by transmitter A MVDS.

4–55. **Data Receive Operation.** Prior to a data receive operation, the CPU will execute a data transmit operation to request information from the transmitter A MVDS. The appropriate information from the MVDS is input to U17A in an RS–232 format.

4–56. U17A inverts and converts the data from an RS–232 signal level to a TTL signal level which is applied to U6 input line RXD. In response to the CPU request, U6 will present the information on the data bus. The CPU will access and store the information in RAM memory.

4–57. **Line Driver U21B Operation.** U21B transmits the carrier detect signal from the modem to the transmitter MVDS. The position of switches S1C and S1D determine the polarity of the carrier detect logic at the input of U21B.

4–58. **REMOTE COMMUNICATION CIRCUIT.** UART U8, line drivers U23A and U23B, and line receiver U17D operate as a communication circuit to provide data transfers between the MT–3 and remote control communication equipment.

4–59. The remote control communication circuit and transmitter A communication circuit are identical in operation with the exception of U8 input line $\overline{\text{DCD}}$ and output line $\overline{\text{DTR}}$. Therefore, only these lines will be explained.

4–60. **$\overline{\text{DCD}}$ Input Line Operation.** The $\overline{\text{DCD}}$ (data carrier detect) input line indicates the status of the remote control communication device. This signal is derived from the carrier detect signal through line driver U17E, inverter U11A, and switch S1. The purpose of S1 is to invert this signal if required.

4–61. The CPU will periodically execute a read operation of U8 to determine the status of the $\overline{\text{DCD}}$ line. If the $\overline{\text{DCD}}$ line is LOW, the CPU will acknowledge and establish contact with the remote control communication device.

4–62. **$\overline{\text{DTR}}$ Output Line Operation.** The $\overline{\text{DTR}}$ (data terminal ready) output line establishes contact with the remote control communication device. To contact the device, the CPU will write a LOW to U8 output line $\overline{\text{DTR}}$. This LOW is applied to the device through line driver U23B.

4–63. **POWER–UP PRESET CIRCUIT.** Inverters U11D, U11E and associated circuitry, and reset one–shot U27B operate as a preset power circuit. For a short duration when power is applied to the MT–3, capacitor C4 is discharged which applies a LOW to U11E input. U11E inverts the LOW to HIGH which is applied to U27B.

4–64. U27B will output a HIGH (RESET) to PPI U4 and U5. The RESET signal is also applied to U11D which inverts the signal and applies a LOW ($\overline{\text{RESET}}$) to UARTs U6, U7, and U8. TP1 and TP2 are provided for manual reset operation when required.

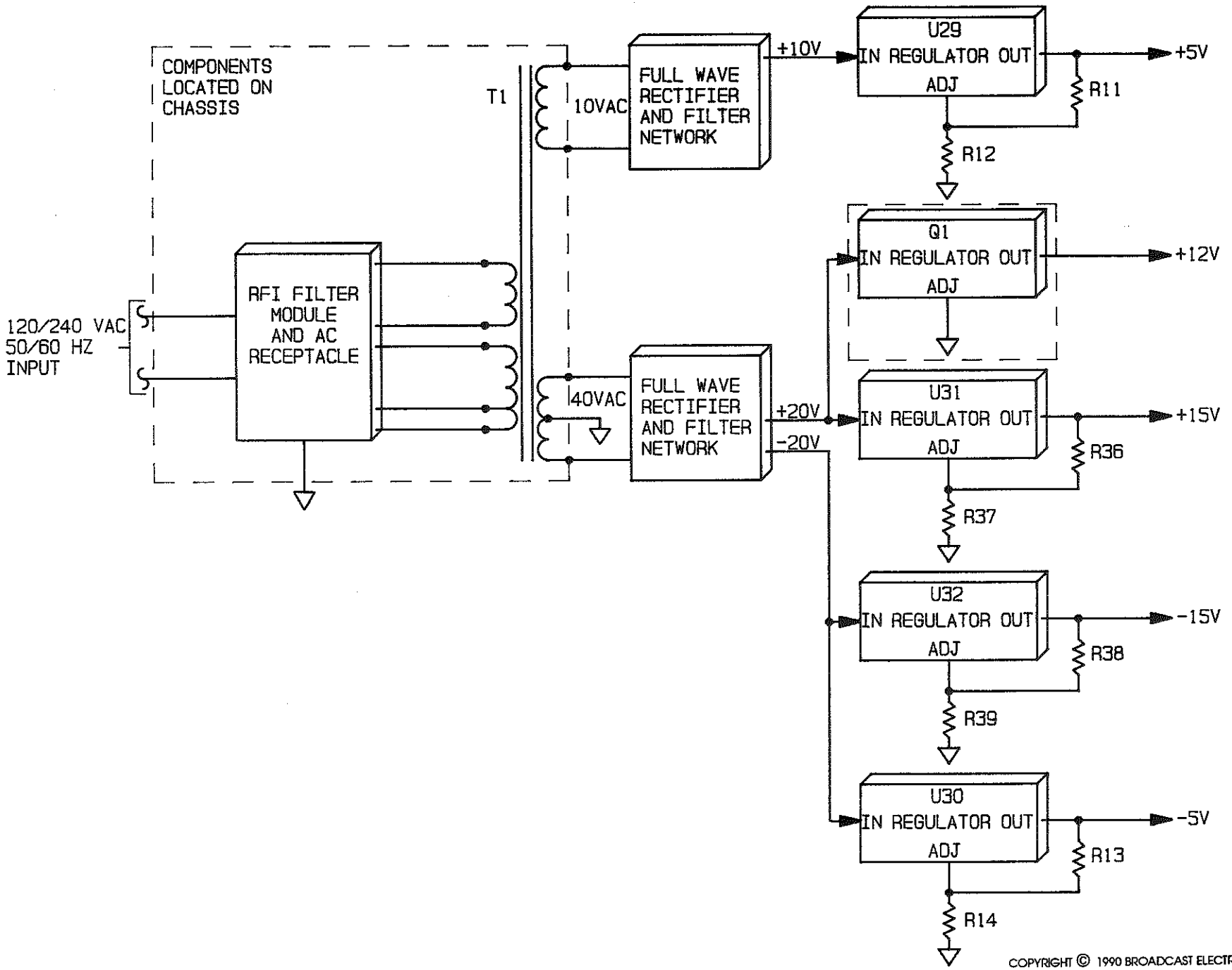
4–65. **ADDRESS MONITOR CIRCUIT.** Monitor one–shot U27A, inverter U20D, resistor R3, and capacitor C3 operate as a missing pulse detector circuit. During normal operation, a periodic pulse is input to U27A from device select decoder U12/U13. U27A will output a HIGH to inverter U20D which applies a LOW to U27B and C3.

4–66. As long as these periodic pulses are present, C3 is prevented from charging and triggering reset one–shot U27B. In the event these pulses are missing for a duration which exceeds a time constant established by C3 and R3, C3 will charge and activate U27B to generate a reset pulse.

4–67. **POWER SUPPLY.**

4–68. Figure 4–2 presents a simplified schematic of the MT–3 power supply circuitry. Refer to Figure 4–2 as required for the following discussion.

4–69. Primary power is applied to the MT–3 through an RFI filter network and ac receptacle module. Power from the receptacle is routed to the primary of power transformer T1 to provide 10 volt and 40 volt ac potentials at the secondaries.




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597-0122-42

**FIGURE 4–2. POWER SUPPLY SIMPLIFIED SCHEMATIC**

4–70. **+5 VOLT SUPPLY.** The 10 volt ac potential is routed to a full–wave rectifier and filter network and applied to voltage regulator U29. Resistors R11 and R12 adjust U29 to provide a regulated +5 volt dc potential to the logic circuit board.

4–71. **+12 VOLT SUPPLY.** The 40 volt ac potential is routed to a full–wave rectifier and filter network to provide +20 volt and –20 volt dc potentials at the output. The +20 volt dc is applied to voltage regulator Q1 to provide +12 volt dc potential to the logic circuit board, relay circuit board, and input/output circuit board.

4–72. **+15 VOLT SUPPLY.** +20 volt dc is also applied to the input of voltage regulator U31. Resistors R36 and R37 adjust U31 to provide a regulated +15 volt dc potential to the logic circuit board.

4–73. **–15 VOLT SUPPLY.** The –20 volt dc is applied to the input of voltage regulator U32. Resistors R38 and R39 adjust U32 to provide a regulated –15 volt dc potential to the logic circuit board.

4–74. **–5 VOLT SUPPLY.** –20 volt dc is also applied to the input of voltage regulator U30. Resistors R13 and R14 adjust U30 to provide a regulated –5 volt dc potential to the logic circuit board.

# SECTION V
# MAINTENANCE

## 5–1. INTRODUCTION.

5–2. This section provides general maintenance and troubleshooting information, electrical adjustment procedures, and component replacement procedures for the Broadcast Electronics MT–3 multiple transmitter interface.

### 5–3. SAFETY CONSIDERATIONS.

5–4. Low voltages are used throughout the MT–3 logic circuit board. Several power supply components on the chassis contain primary ac line voltage. Therefore, do not perform any maintenance or troubleshooting procedures on the power supply circuitry with power applied. Maintenance with power energized is always considered hazardous and caution should be observed. Good judgment, care, and common sense must be practiced to prevent accidents. The procedures contained in this section should be performed only by experienced and trained personnel.

## 5–5. FIRST LEVEL MAINTENANCE.

5–6. First level maintenance consists of precautionary procedures applied to the equipment to prevent future failures. The procedures are performed on a regular basis and the results recorded in a performance log.

*WARNING* *DISCONNECT THE PRIMARY POWER TO THE MT–3 BEFORE ATTEMPTING ANY EQUIPMENT*
*WARNING* *MAINTENANCE.*

### 5–7. GENERAL.

5–8. Periodically remove abrasions from the MT–3 chassis with a cloth moistened with a mild household cleaner. Remove dust from the chassis exterior with a brush and vacuum cleaner as required.

### 5–9. ELECTRICAL.

5–10. All circuit boards should be periodically cleaned of accumulated dust using a soft brush and vacuum cleaner. Check the logic circuit board for improperly seated semiconductors and components damaged by overheating.

## 5–11. SECOND LEVEL MAINTENANCE.

5–12. The second level maintenance consists of procedures required to restore an MT–3 to operation after a fault has occurred. The procedures are divided into troubleshooting, electrical adjustments, and electrical component replacement procedures.

5–13. The MT–3 maintenance philosophy consists of isolating the problem to a specific assembly with subsequent troubleshooting to isolate defective components.

### 5–14. ELECTRICAL ADJUSTMENTS.

5–15. **REQUIRED EQUIPMENT.** The following tools and equipment are required for electrical adjustment procedures.

A. Insulated adjustment tool (P/N 407–0083).

B. Precision digital voltmeter, HP3486A or equivalent.

5–16. **A/D CONVERTER OFFSET AND GAIN ADJUSTMENTS (R26 AND R27).** Potentiometers R26 and R27 on the logic circuit board adjust the A/D converter gain and offset voltage. Potentiometers R26 and R27 are adjusted as follows.

5–17. **Procedure.** To adjust R26 and R27, proceed as follows:

*WARNING* ***DISCONNECT THE PRIMARY POWER TO THE MT–3 BEFORE PROCEEDING.***

*WARNING*

A. Disconnect the MT–3 primary power.

B. Remove the MT–3 bottom–panel. Refer to Figure 5–1 and operate TEST switch S1B on the logic circuit board to the ON position.

C. Refer to Figure 5–1 and connect a precision digital voltmeter between TP3 and analog ground.

D. Apply primary power to the MT–3.

E. Refer to Figure 5–1 and adjust offset control R27 until the voltmeter indicates –5.000V ±0.000V.

F. Operate TEST switch S1B on the logic circuit board to the OFF position.

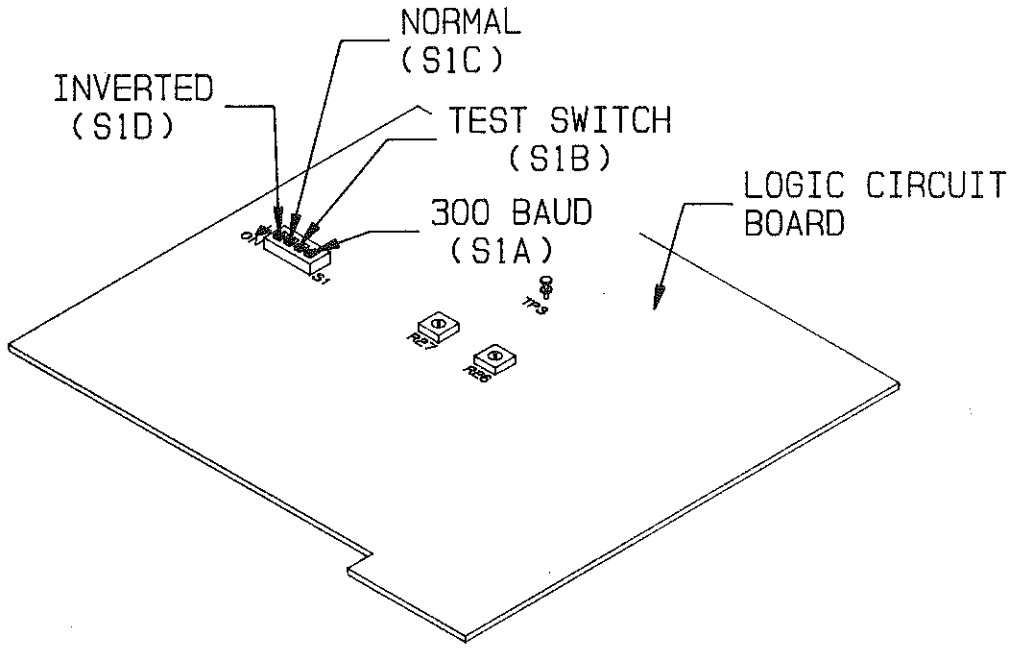
G. Refer to Figure 5–1 and adjust gain control R26 until the voltmeter indicates +5.000V ±0.000V.

*WARNING* ***DISCONNECT THE PRIMARY POWER TO THE MT–3 BEFORE PROCEEDING.***

*WARNING*

H. Disconnect MT–3 primary power to terminate the test program.

I. Remove all test equipment, ensure TEST switch S1B is in the OFF position, and replace the bottom–panel.




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597–0122–30

**FIGURE 5–1. CONTROLS AND TEST POINTS**

5–18. **FUSE LINK REPLACEMENT.** The relay output circuits are protected with replaceable fuse links on the relay circuit board. A fuse link is replaced as follows.

5–19. **Procedure.** To replace a fuse link, proceed as follows:

***WARNING*** ***DISCONNECT THE PRIMARY POWER TO THE MT–3 AND ANY HIGH VOLTAGE TERMINATIONS TO THE MT–3 REAR–PANEL BEFORE PROCEEDING.***

***WARNING***

A. Disconnect the MT–3 primary power.

B. Remove the top–panel and the relay circuit board guard.

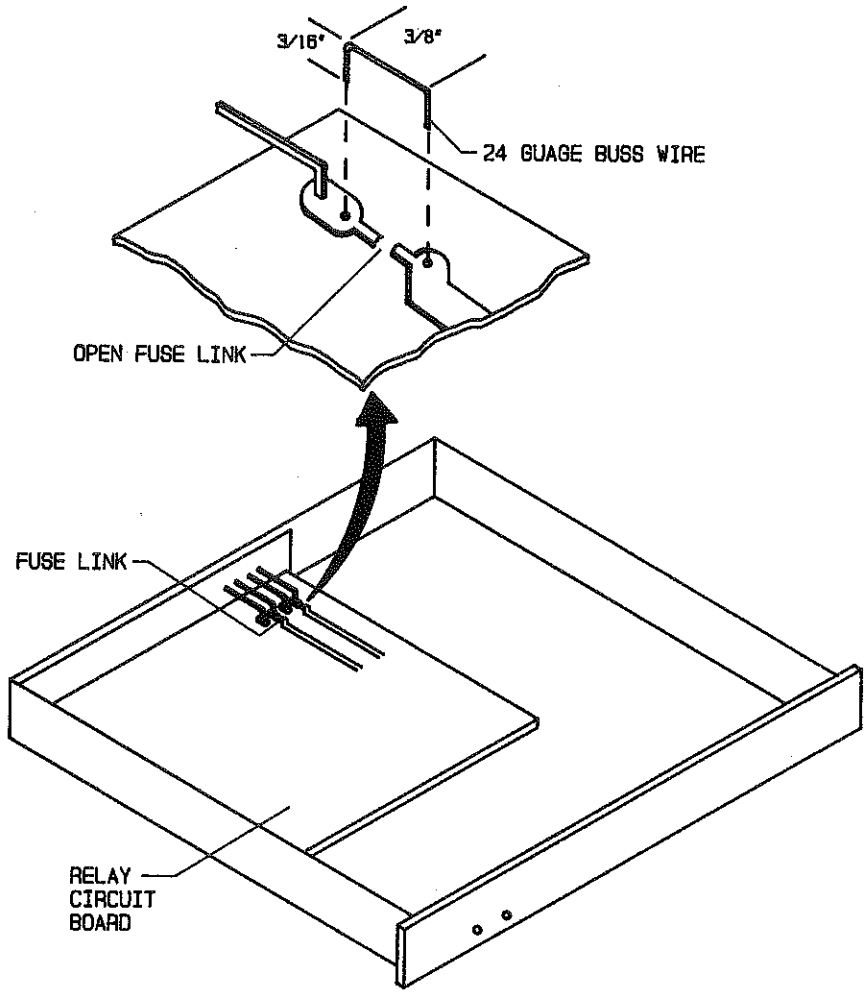
C. Refer to Figure 5–2 and fabricate a jumper using 24 gauge buss wire as shown.

D. Refer to Figure 5–2 and insert the jumper across the open fuse link. Apply solder to the component side of the circuit board.

E. Replace the relay circuit board guard and top–panel.

5–20. **TROUBLESHOOTING.**

5–21. The troubleshooting philosophy for the multiple transmitter interface consists of isolating a problem to a specific circuit. The problem may be further isolated by referencing the following information and Table 5–1 which presents the MT–3 troubleshooting information.




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC
597-0122-51

**FIGURE 5–2. MT–3 FUSE LINE LOCATION**

***WARNING*** ***DISCONNECT THE PRIMARY POWER SOURCE FROM THE MT–3 BEFORE REMOVING OR REPLACING ANY***
***WARNING*** ***COMPONENTS.***

***CAUTION*** ***INADVERTENT CONTACT BETWEEN ADJACENT COM–***
***CAUTION*** ***PONENTS OR CIRCUIT BOARDS WITH TEST EQUIP–MENT MAY CAUSE SERIOUS DAMAGE TO THE MULTIPLE TRANSMITTER INTERFACE.***

5–22. After the problem is isolated and power is totally deenergized, refer to the schematic diagrams and the theory of operation to assist in problem resolution. The defective component may be repaired locally or the entire device may be returned to Broadcast Electronics Inc. for repair or replacement.

TABLE 5–1. MT–3 TROUBLESHOOTING

| SYMPTOM | DEFECT/REMEDY |
|---|---|
| NO OPERATION | 1 Check the ac line fuse on the rear–panel.<br>2. Check +15V, –15V, +5V, and –5V operating voltages.<br>3. Check central processing unit U1. |
| NO 1.8432 MHz SIGNAL | 1. Check clock oscillator circuit U10A, U10B, U10C, transistor Q1, and crystal Y1. |
| NO MANUAL RESET OPERATION | 1. Check inverter U11E and capacitor C4. |
| NO POWER–UP RESET OPERATION | 1. Check reset circuit U27B, inverter U11D, and capacitor C3. |
| NO CONTROL RELAY OPERATION | 1. Check driver/inverter logic U18, U19, U20A, and U20B. |
| NO STATUS INPUT AND RELAY OPERATION | 1. Check programmable peripheral interface circuit U4. |
| NO FAIL–SAFE RELAY OPERATION | 1. Check fail–safe relay K17. |
| NO ANALOG CHANNEL INPUT OPERATION | 1. Check analog multiplexer U26.<br>2. Check analog input enable gate U10E, U10D, and U15C. |
| NO D/A OPERATION | 1. Check digital/analog converter U25, current/voltage converter U24A, comparator U24B, and inverter U11E. |
| NO ANALOG CHANNEL INPUT AND D/A OPERATION | 1. Check programmable peripheral interface circuit U5. |
| NO TRANSMITTER A CONTROL OPERATION | 1. Check UART U6, line drivers U21A, U21B, and line receiver U17A. |
| NO REMOTE COMMUNICATION OPERATION | 1. Check UART U8, line drivers U23A, U23B, line receivers U17E, and U17D. |

*WARNING* *DISCONNECT THE PRIMARY POWER BEFORE RE-MOVING OR REPLACING CIRCUIT BOARDS OR COMPONENTS.*

*WARNING*

*CAUTION* *WHEN REPLACING A COMPONENT MOUNTED ON A HEAT-SINK, ENSURE A THIN FILM OF A ZINC-BASED HEAT-SINK COMPOUND IS USED TO ASSURE ADE-QUATE HEAT DISSIPATION.*

*CAUTION*

5-23. **COMPONENT REPLACEMENT.**

5-24. On all circuit boards, the adhesion between the copper trace and the circuit board fails at almost the same temperature as solder melts. A circuit board trace can be destroyed by excessive heat or lateral movement during soldering. Use of a small soldering iron with steady pressure is required for circuit board repairs.

5-25. To remove a soldered component from a circuit board, cut the leads from the body of the defective component while the device is still soldered to the board. Grip a component lead with needle-nose pliers. Touch the soldering iron to the lead at the solder connection on the circuit side of the board. When the solder begins to melt, push the lead through the back side of the board and cut off the clinched end of the lead. Each lead may now be heated independently and pulled out of each hole. The holes may be cleared by careful re-heating with a low wattage iron and removing solder with a soldering vacuum tool.

5-26. Install the new component and apply solder from the circuit side of the board. If no damage has been incurred to the plated-through holes, soldering of the component side of the board will not be required.

*WARNING* *MOST SOLVENTS WHICH REMOVE ROSIN FLUX ARE VOLATILE AND TOXIC BY NATURE AND SHOULD BE USED ONLY IN SMALL AMOUNTS IN A WELL VENTI-LATED AREA AWAY FROM FLAME, CIGARETTES, AND HOT SOLDERING IRONS.*

*WARNING*

*WARNING* *OBSERVE THE MANUFACTURES CAUTIONARY INSTRUCTIONS.*

*WARNING*

5-27. After soldering, remove residual flux with a suitable solvent. Rubbing alcohol is highly diluted and is not effective.

5-28. The board should be checked to ensure the flux has been completely removed. Rosin flux is not normally corrosive; however, in time the flux will absorb enough moisture to become conductive and create problems.

5-29. **INTEGRATED CIRCUITS.** Special care should be exercised with integrated circuits. Each intergrated circuit must be installed by matching the integrated circuit notch with the notch on the socket. Do not attempt to remove an integrated circuit from a socket with your fingers. Use an integrated circuit puller to pry the component from the socket.

# SECTION VI
# PARTS LIST

## 6–1. INTRODUCTION.

6–2. This section provides descriptions and part numbers of electrical components, assemblies, and selected mechanical parts required for maintenance of the MT–3 multiple transmitter interface. Each table entry in this section is indexed by reference designators appearing on the applicable schematic diagram.

**TABLE 6–1. REPLACEABLE PARTS LIST INDEX**


| TABLE | DESCRIPTION | PART NO. | PAGE |
|---|---|---|---|
| 6–2 | MT–3 MULTIPLE TRANSMITTER INTERFACE | 909–0127–004 | 6–2 |
| 6–3 | LOGIC CIRCUIT BOARD ASSEMBLY | 919–0300 | 6–2 |
| 6–4 | STATUS/ANALOG I/O CIRCUIT BOARD ASSEMBLY | 919–0301 | 6–4 |
| 6–5 | RELAY I/O CIRCUIT BOARD ASSEMBLY | 919–0302 | 6–5 |
| 6–6 | CABLE ASSEMBLY | 949–0153 | 6–5 |
| 6–7 | POWER SUPPLY CIRCUIT BOARD ASSEMBLY | 910–0105 | 6–5 |
| 6–8 | ACCESSORY KIT | 979–0127 | 6–6 |
| 6–9 | CABLE ASSEMBLY MVDS TO MT–3 | 949–0204 | 6–6 |

## TABLE 6–2. MT–3 MULTIPLE TRANSMITTER INTERFACE – 909–0127–004

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| C1,C2 | Capacitor, Electrolytic, 10 uF, 50V | 023–1076 | 2 |
| DS1 | Indicator, LED, Green, 521–9175, 3V @ 40 mA Maximum | 323–9224 | 1 |
| DS2 | Indicator, LED, Yellow, 521–9176, 3V @ 30 mA Maximum | 323–9225 | 1 |
| J11 | Connector Housing, 6–Pin | 418–0006 | 1 |
| P2 | Connector Housing, 6–Pin | 418–0670 | 1 |
| Q1 | Integrated Circuit, LM340K–12, Three–Terminal Positive Fixed Voltage Regulator, +12V, TO–3 Case | 227–7812–A | 1 |
| T1 | Transformer, Power<br>Dual Primary: 110V/220V ±10%, 50/60 Hz, Single–Phase<br>Dual Secondary: ±18V dc @ 250 mA<br>+8V dc @ 1A | 370–0027 | 1 |
| —— | Fused Power Connector/Voltage Selector/EMI Filter, 120/240V | 360–6504 | 1 |
| —— | Fuse, AGC, 1A, 250V, Slow–Blow for use on 117 VAC 50/60 Hz | 334–0100 | 2 |
| —— | Fuse AGC, 1/2A. 250V, Slow–Blow for use on 220 VAC 50/60 Hz | 334–0550 | 2 |
| —— | Fuse Clip | 415–1001 | 2 |
| —— | Insulator, Mica, Transistor Mounting, TO–3 Case | 418–0010 | 1 |
| —— | Socket, Transistor, TO–3 Case | 417–0298 | 1 |
| —— | Pins, Connector | 417–0036 | 6 |
| —— | Socket, Connector | 417–0053 | 6 |
| —— | Multiple Transmitter Controller Cable Assembly | 949–0153 | 1 |
| —— | Power Supply Circuit Board Assembly | 910–0105 | 1 |
| —— | Relay I/O Circuit Board Assembly | 919–0302 | 1 |
| —— | Logic Circuit Board Assembly | 919–0300 | 1 |
| —— | Status I/O Circuit Board Assembly | 919–0301 | 1 |
| —— | MT–3 Accessory Kit | 979–0127 | 1 |

## TABLE 6–3. LOGIC CIRCUIT BOARD ASSEMBLY – 919–0300
(Sheet 1 of 3)

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| C1 | Capacitor, Mica, 33 pF ±5%, 500V | 042–3312 | 1 |
| C2 | Capacitor, Mica, 100 pF, 500V | 040–1022 | 1 |
| C3 | Capacitor, Electrolytic, 1 uF, 50V | 024–1064 | 1 |
| C4 | Capacitor, Electrolytic, 100 uF, 35V | 023–1084 | 1 |
| C5 THRU C12 | Capacitor, Electrolytic, 10 uF, 35V | 023–1076 | 8 |
| C13 | Capacitor, Electrolytic, 1 uF, 50V | 024–1064 | 1 |
| C14 THRU C17 | Capacitor, Electrolytic, 10 uF, 35V | 023–1076 | 4 |
| C18 THRU C25 | Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V | 003–1054 | 8 |
| C26 THRU C33 | Capacitor, Electrolytic, 10 uF, 35V | 023–1075 | 8 |
| C34,C35 | Capacitor, Mylar Film, 0.1 uF, 100V | 030–1053 | 2 |
| C36,C37 | Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V | 003–1054 | 2 |
| C39 | Capacitor, Mica, 33 pF ±5%, 500V | 042–3312 | 1 |
| C40 THRU C66 | Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V | 003–1054 | 27 |
| C67,C68,C69 | Capacitor, Mica, 100 pF, 500V | 040–1022 | 3 |
| C70 THRU C74 | Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V | 003–1054 | 5 |
| D1 | Diode, 1N4148, Silicon, 75V @ 0.3 Amperes | 203–4148 | 1 |
| D2 | Diode, 1N4005, Silicon, 600V @ 1 Ampere | 203–4005 | 1 |

## TABLE 6–3. LOGIC CIRCUIT BOARD ASSEMBLY – 919–0300
(Sheet 2 of 3)

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| D3,D4 | Diode, 1N4148, Silicon, 75V @ 0.3 Amperes | 203–4148 | 2 |
| D5 THRU D9 | Diode, 1N4005, Silicon, 600V @ 1 Ampere | 203–4005 | 5 |
| D10 THRU D13 | Diode, 1N4148, Silicon, 75V @ 0.3 Amperes | 203–4148 | 4 |
| D14 | Diode, 1N4005, Silicon, 600V @ 1 Ampere | 203–4005 | 1 |
| D15 | Diode, 1N4737, Zener, 7.5V ±10%, 1W | 200–4737 | 1 |
| D16 | Diode, 1N4148, Silicon, 75V @ 0.3 Amperes | 203–4148 | 1 |
| J4,J5 | Connector Header, 26–Pin | 417–0182 | 2 |
| J7 | Receptacle, Male, 8–Pin In–Line, Right Angle | 417–0080–001 | 1 |
| J8,J9,J10 | Connector Header, 10–Pin Dual In–Line | 417–0179 | 3 |
| Q1 | Transistor, 2N3906, PNP, Silicon, TO–92 Case | 210–3906 | 1 |
| R1 | Resistor, 2.2 Meg Ohm ±5%, 1/4W | 100–2273 | 1 |
| R2 | Resistor, 10 k Ohm ±5%, 1/4W | 100–1053 | 1 |
| R3 | Resistor, 1 Meg Ohm ±5%, 1/4W | 100–1073 | 1 |
| R4 THRU R9 | Resistor, 10 k Ohm ±5%, 1/4W | 100–1053 | 6 |
| R10 | Resistor, 100 k Ohm ±5%, 1/4W | 100–1063 | 1 |
| R11 | Resistor, 124 Ohm ±1%, 1/4W | 103–1241 | 1 |
| R12 | Resistor, 392 Ohm ±1%, 1/4W | 103–3923 | 1 |
| R13 | Resistor, 124 Ohm ±1%, 1/4W | 103–1241 | 1 |
| R14 | Resistor, 392 Ohm ±1%, 1/4W | 103–3923 | 1 |
| R15 THRU R22 | Resistor, 3.3 k Ohm ±5%, 1/4W | 100–3343 | 8 |
| R23 | Resistor, 100 k Ohm ±5%, 1/4W | 100–1063 | 1 |
| R24 | Resistor, 100 Ohm ±5%, 1/4W | 100–1033 | 1 |
| R25 | Resistor, 2.4 k Ohm ±5%, 1/4W | 100–2443 | 1 |
| R26,R27 | Potentiometer, 100 Ohm ±10%, 1/2W | 177–1034 | 2 |
| R28 | Resistor, 100 Ohm ±5%, 1/4W | 100–1033 | 1 |
| R29 | Resistor, 2.2 Meg Ohm ±5%, 1/4W | 100–2273 | 1 |
| R30 | Resistor, 100 Ohm ±5%, 1/4W | 100–1033 | 1 |
| R31 | Resistor, 100 k Ohm ±5%, 1/4W | 100–1063 | 1 |
| R32 THRU R35 | Resistor, 10 k Ohm ±5%, 1/4W | 100–1053 | 4 |
| R36 | Resistor, 124 Ohm ±1%, 1/4W | 103–1241 | 1 |
| R37 | Resistor, 1.37 k Ohm ±1%, 1/4W | 100–1341 | 1 |
| R38 | Resistor, 124 Ohm ±1%, 1/4W | 103–1241 | 1 |
| R39 | Resistor, 1.37 k Ohm ±1%, 1/4W | 100–1341 | 1 |
| R40 | Resistor, 10 k Ohm ±5%, 1/4W | 100–1053 | 1 |
| R41,R42 | Resistor, 220 Ohm ±5%, 1/4W | 100–2233 | 2 |
| R43 | Resistor, 1 Meg Ohm ±5%, 1/4W | 100–1073 | 1 |
| RN3,RN4 | Resistor Network, 9–10 k Ohm ±2%, 1/4W Resistor, Single In–Line 10–Pin Package | 226–1050 | 2 |
| S1 | Switch, SPST, 4–Position, 8–Pin DIP Dual In–Line | 340–0002 | 1 |
| TP1,TP2,TP3 | Terminal, Turret, Double Shoulder | 413–1597 | 3 |
| U1 | Integrated Circuit, Z84C00, CMOS Processor, 40–Pin DIP | 220–8400 | 1 |
| U2 | Integrated Circuit, EPROM, 8K X 8 RAM, 12.5V PGM, 200 nS, 28–Pin DIP | 220–2764 | 1 |
| U3 | Integrated Circuit, X2816AD Non–Volital 2K X 8 RAM, ,CMOS, 24–Pin DIP | 220–2816 | 1 |
| U4,U5 | Integrated Circuit, 82C55A, CMOS Programmable Peripheral Interface, 24 Parallel I/O, 40–Pin DIP | 220–8255 | 2 |

## TABLE 6–3. LOGIC CIRCUIT BOARD ASSEMBLY – 919–0300
(Sheet 3 of 3)

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| U6,U7,U8 | Integrated Circuit, 65C51, CMOS Asynchronous Communications Interface Adapter, 8–Bit Processor, 28–Pin DIP | 220–6551 | 3 |
| U9 | Integrated Circuit, 74HC245, 8–Bit, Bi–Directional Bus Driver, 3–State High Speed CMOS, 20–Pin DIP | 220–4245 | 1 |
| U10 | Integrated Circuit, CD4069CN, Hex Inverter, CMOS, 14–Pin DIP | 228–4069 | 1 |
| U11 | Integrated Circuit, MC14584, Hex Schmitt Trigger, CMOS, 14–Pin DIP | 228–4584 | 1 |
| U12,U13 | Integrated Circuit, 74HC42, 1–10 Decoder, High Speed CMOS, 16–Pin DIP | 220–7442 | 2 |
| U14 | Integrated Circuit, 74HC245, 8–Bit, Bi–Directional Bus Driver, 3–State High Speed CMOS, 20–Pin DIP | 220–4245 | 1 |
| U15 | Integrated Circuit, MC14023B, CMOS, Triple 3–Input NAND Gate | 228–4023 | 1 |
| U16,U17 | Integrated Circuit, ULN2001, Darlington Seven Transistor Arrays, NPN, 16–Pin DIP | 220–2001 | 2 |
| U18,U19,U20 | Integrated Circuit, ULN2003, 7 Section NPN Darlington Driver, CMOS, 16–Pin DIP | 229–2003 | 3 |
| U21,U22,U23 | Integrated Circuit, RC4558DN, Dual Operational Amplifier, 8–Pin DIP | 221–4558 | 3 |
| U24 | Integrated Circuit, RC4559NB, Operational Amplifier, 8–Pin DIP | 221–4559 | 1 |
| U25 | Integrated Circuit, AD565AJ, 12–Bit Digital/Analog Converter, 24–Pin DIP | 220–0565 | 1 |
| U26 | Integrated Circuit, MC14051BCP, 8–Bit Analog Multiplexer, CMOS, 16–Pin DIP | 220–4051 | 1 |
| U27,U28 | Integrated Circuit, MC14013BCP, Dual D–Type Flip–Flop, CMOS, 14–Pin DIP | 228–4013 | 2 |
| U29 | Integrated Circuit, LM317K, Three–Terminal Adjustable Positive Voltage Regulator, 1.2 to 37V, 1.5 Ampere Maximum, TO–3 Case | 227–0318 | 1 |
| U30 | Integrated Circuit, LM337T, Adjustable Negative Voltage Regulator, 1.2V to 37V, 1.5 Ampere, TO–220 Case | 227–0337 | 1 |
| U31 | Integrated Circuit, LM317T, Adjustable Positive Voltage Regulator, 1.2V to 37V, 1.5 Ampere, TO220 Case | 227–0317 | 1 |
| U32 | Integrated Circuit, LM337T, Adjustable Negative Voltage Regulator, 1.2V to 37V, 1.5 Ampere, TO–220 Case | 227–0337 | 1 |
| Y1 | Crystal, 1.8432 MHz, 13 pF Load Capacitance, 500 Ohms, A/T Cut, HC33/U Case | 390–0021 | 1 |
| —— | Socket, 8–Pin DIP | 417–0804 | 4 |
| —— | Socket, 14–Pin DIP | 417–1404 | 5 |
| —— | Socket, 16–Pin DIP | 417–1604 | 8 |
| —— | Socket, 20–Pin DIP | 417–2004 | 2 |
| —— | Socket, 24–Pin DIP | 417–2404 | 2 |
| —— | Socket, 28–Pin DIP | 417–2804 | 4 |
| —— | Socket, 40–Pin DIP | 417–4005 | 3 |
| —— | Blank Logic Circuit Board | 519–0300 | 1 |

## TABLE 6–4. STATUS/ANALOG I/O CIRCUIT BOARD ASSEMBLY – 919–0301
(Sheet 1 of 2)

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| C1 THRU C17 | Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V | 003–1054 | 17 |
| J5 | Connector Header, 26–Pin | 417–0182 | 1 |
| L1 THRU L9 | RF Choke, 4.7 uH ±10%, 430 mA, DC Resistance: 0.55 Ohms, 0.43 Amperes Maximum, Resonant at 115 MHz | 360–0022 | 9 |

## TABLE 6–4. STATUS/ANALOG I/O CIRCUIT BOARD ASSEMBLY – 919–0301
(Sheet 2 of 2)

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| RN1 | Resistor Network, 9 resistors, 1.0 k Ohm ±2%, 0.3W, 10–Pin Single In–Line Package | 226–0393 | 1 |
| RN2 | Resistor Network, 8–10 k Ohm ±1%, 1/4W, 16–Pin DIP | 226–1055 | 1 |
| TB2 | 34–Pin Terminal Block | 412–0046 | 1 |
| —— | Blank Status/Analog I/O Circuit Board | 519–0301 | 1 |

## TABLE 6–5. RELAY I/O CIRCUIT BOARD ASSEMBLY – 919–0302

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| J4 | Connector Header, 26–Pin | 417–0182 | 1 |
| K1 THRU K17 | Relay, Circuit Board Mount<br>Coil: 12V dc<br>Contacts: SPDT, 3A @ 28V dc and 3A @ 120V ac | 270–0059 | 17 |
| TB1 | 34–Pin Terminal Block | 412–0046 | 1 |
| —— | Blank Relay I/O Circuit Board | 519–0302 | 1 |

## TABLE 6–6. CABLE ASSEMBLY – 949–0153

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| J1,J2,J3 | Connector, Male, 9–Pin | 417–0181 | 3 |
| P1 | Connector Housing, 12–Pin | 418–1271 | 1 |
| P3 | Connector Plug, 9–Pin | 417–0059 | 1 |
| P4,P4,P5,P5 | Plug, Ribbon Cable, 26–Pin Dual In–Line | 418–2600 | 4 |
| P7 | Plug, Housing, 8–Pin | 417–0046 | 1 |
| P8,P9,P10 | Connector, 10–Pin | 417–0180 | 3 |
| P11 | Connector Housing, 6–Pin | 418–0670 | 1 |
| —— | Pins, Connector | 417–0036 | 6 |
| —— | Pins, Connector | 417–0053 | 19 |
| —— | Pins, Crimp Type | 417–8766 | 8 |

## TABLE 6–7. POWER SUPPLY CIRCUIT BOARD ASSEMBLY – 910–0105

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| C1 THRU C4 | Capacitor, Electrolytic, 4700 uF, 50V | 014–4793 | 4 |
| D1 THRU D4 | Diode, MR502, Silicon, 200V @ 3 Amperes | 202–0502 | 4 |
| D5 THRU D8 | Diode, MR751, Silicon, 100V @ 6 Amperes | 202–0751 | 4 |
| D9,D10,D11 | Diode, 1N4005, Silicon, 600V @ 1 Ampere | 203–4005 | 3 |
| D12,D13 | Diode, MR751, Silicon, 100V @ 6 Amperes | 202–0751 | 2 |
| D14 | Diode, 1N4005, Silicon, 600V @ 1 Ampere | 203–4005 | 1 |
| J1 | Receptacle, 12–Pin | 417–1276 | 1 |
| J2 | Receptacle, 6–Pin | 417–0677 | 1 |
| J3 | Connector, 9–Pin | 418–0900 | 1 |
| —— | Blank Power Supply Circuit Board | 510–0105 | 1 |

## TABLE 6–8. ACCESSORY KIT – 979–0127

| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| J2 | Receptacle, 9–Pin | 418–2432 | 1 |
| —— | AC Line Cord, N.E.M.A. 3–Wire North American Plug | 682–0001 | 1 |
| —— | Plug, 25–Pin | 417–2517 | 1 |
| —— | Adapter, 25–Pin Female/9–Pin Male | 804–0063 | 1 |
| —— | IBM AT to Modem Cable Assembly | 804–0062 | 1 |
| —— | Cable Assembly, MVDS to MT–3 | 949–0204 | 1 |

## TABLE 6–9. CABLE ASSEMBY MVDS TO MT–3 – 949–0204

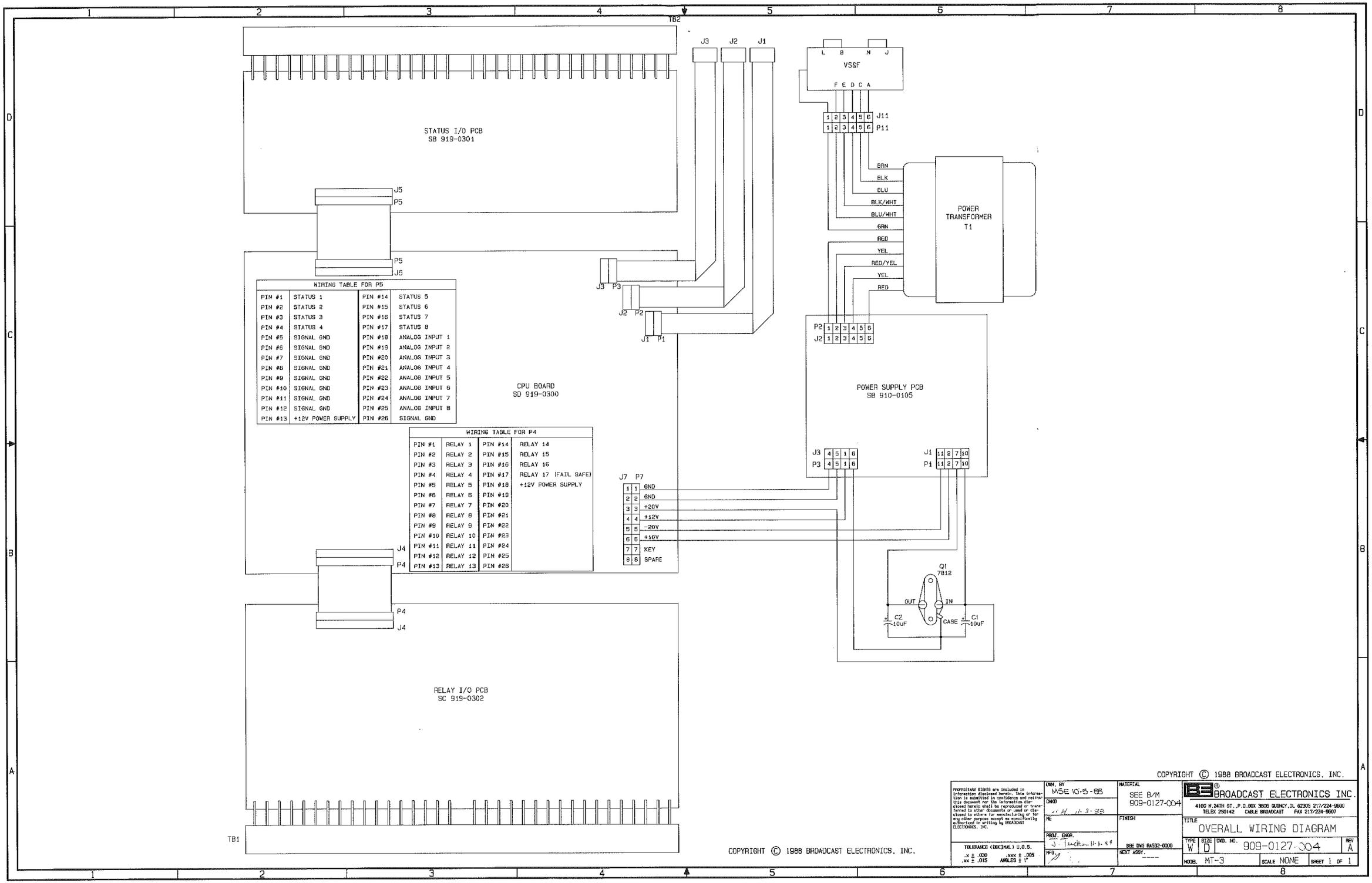
| REF. DES. | DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| —— | Pins, Socket | 417–0143 | 4 |
| —— | Connector, Plug, 25–Pin | 417–0251 | 1 |
| —— | Receptacle, 9–Pin | 417–0901 | 1 |
| —— | Pins, Connector | 417–0142 | 4 |

# SECTION VII
# DRAWINGS

## 7–1. INTRODUCTION.

7–2. This section provides assembly diagrams, schematic diagrams, and cable diagrams as listed below for the Broadcast Electronics MT–3 multiple transmitter interface.

| FIGURE | TITLE | NUMBER |
|---|---|---|
| 7–1 | MT–3 OVERALL WIRING DIAGRAM | WD909–0127–004 |
| 7–2 | MT–3 ASSEMBLY DIAGRAM | AD909–0127–004 |
| 7–3 | CPU CIRCUIT BOARD SCHEMATIC | SD919–0300 |
| 7–4 | CPU CIRCUIT BOARD ASSEMBLY | AC919–0300 |
| 7–5 | STATUS I/O CIRCUIT BOARD SCHEMATIC | SC919–0301 |
| 7–6 | STATUS I/O CIRCUIT BOARD ASSEMBLY | 597–0122–43 |
| 7–7 | RELAY I/O CIRCUIT BOARD SCHEMATIC | SC919–0302 |
| 7–8 | RELAY I/O CIRCUIT BOARD ASSEMBLY | 597–0122–44 |
| 7–9 | POWER SUPPLY CIRCUIT BOARD SCHEMATIC | SB910–0105 |
| 7–10 | POWER SUPPLY CIRCUIT BOARD ASSEMBLY | 597–0122–45 |
| 7–11 | MT–3 INTERFACE CABLE DIAGRAMS | 597–0122–31 |




WIRING TABLE FOR P5

| | | | |
|---|---|---|---|
| PIN #1 | STATUS 1 | PIN #14 | STATUS 5 |
| PIN #2 | STATUS 2 | PIN #15 | STATUS 6 |
| PIN #3 | STATUS 3 | PIN #16 | STATUS 7 |
| PIN #4 | STATUS 4 | PIN #17 | STATUS 8 |
| PIN #5 | SIGNAL GND | PIN #18 | ANALOG INPUT 1 |
| PIN #6 | SIGNAL GND | PIN #19 | ANALOG INPUT 2 |
| PIN #7 | SIGNAL GND | PIN #20 | ANALOG INPUT 3 |
| PIN #8 | SIGNAL GND | PIN #21 | ANALOG INPUT 4 |
| PIN #9 | SIGNAL GND | PIN #22 | ANALOG INPUT 5 |
| PIN #10 | SIGNAL GND | PIN #23 | ANALOG INPUT 6 |
| PIN #11 | SIGNAL GND | PIN #24 | ANALOG INPUT 7 |
| PIN #12 | SIGNAL GND | PIN #25 | ANALOG INPUT 8 |
| PIN #13 | +12V POWER SUPPLY | PIN #26 | SIGNAL GND |

WIRING TABLE FOR P4

| | | | |
|---|---|---|---|
| PIN #1 | RELAY 1 | PIN #14 | RELAY 14 |
| PIN #2 | RELAY 2 | PIN #15 | RELAY 15 |
| PIN #3 | RELAY 3 | PIN #16 | RELAY 16 |
| PIN #4 | RELAY 4 | PIN #17 | RELAY 17 (FAIL SAFE) |
| PIN #5 | RELAY 5 | PIN #18 | +12V POWER SUPPLY |
| PIN #6 | RELAY 6 | PIN #19 | |
| PIN #7 | RELAY 7 | PIN #20 | |
| PIN #8 | RELAY 8 | PIN #21 | |
| PIN #9 | RELAY 9 | PIN #22 | |
| PIN #10 | RELAY 10 | PIN #23 | |
| PIN #11 | RELAY 11 | PIN #24 | |
| PIN #12 | RELAY 12 | PIN #25 | |
| PIN #13 | RELAY 13 | PIN #26 | |

COPYRIGHT © 1988 BROADCAST ELECTRONICS, INC.

COPYRIGHT © 1988 BROADCAST ELECTRONICS, INC.

PROPRIETARY RIGHTS are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY: MSE 10-5-88
CHKD: [illegible] 11-3-88
ME:
PROJ. ENGR.: J. [illegible] 11-1-89
MFG.:

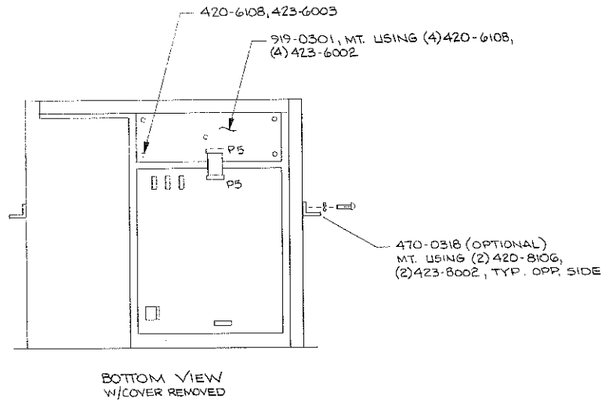
MATERIAL: SEE B/M 909-0127-004
FINISH: SEE DWG RA592-0000
NEXT ASSY.: ----

BROADCAST ELECTRONICS INC.
4100 N.24TH ST., P.O.BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST FAX 217/224-9607

TITLE: OVERALL WIRING DIAGRAM

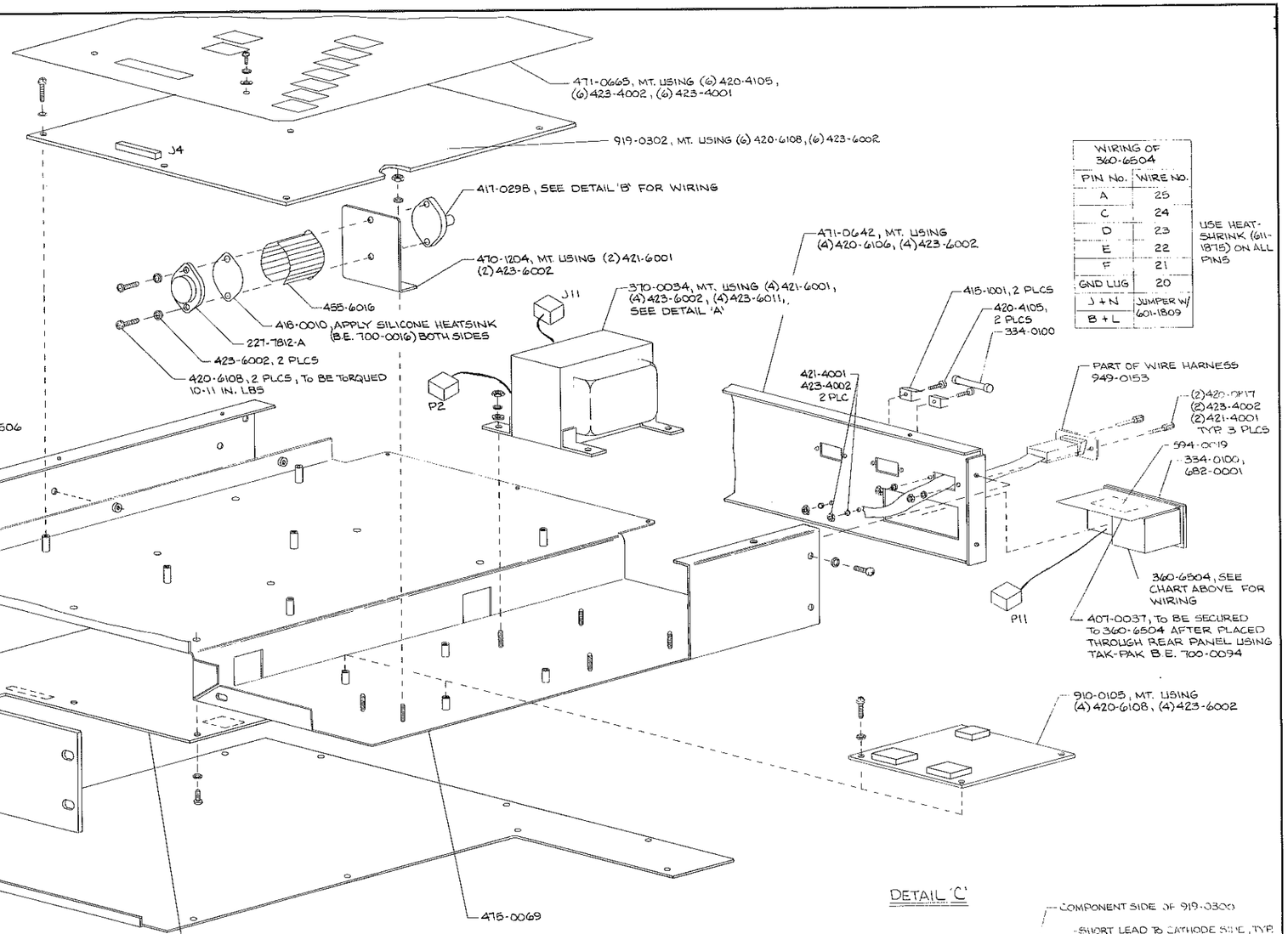
TYPE: W | SIZE: D | DWG. NO. 909-0127-004 | REV: A

MODEL: MT-3 | SCALE: NONE | SHEET 1 OF 1




BOTTOM VIEW
W/COVER REMOVED

COPYRIGHT © 1988 BROADCAST ELECTRONICS, INC.

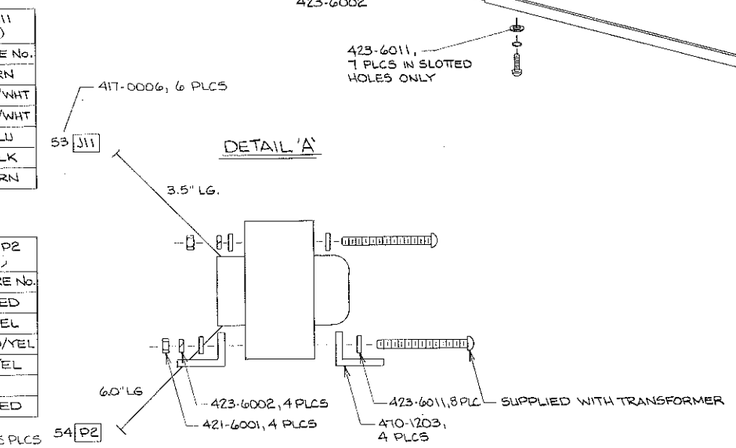


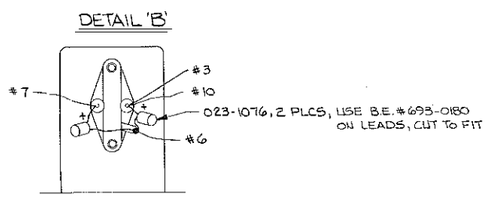

| WIRING OF 360-6504 | |
|---|---|
| PIN No. | WIRE No. |
| A | 25 |
| C | 24 |
| D | 23 |
| E | 22 |
| F | 21 |
| GND LUG | 20 |
| J + N | JUMPER W/ 601-1809 |
| B + L | |

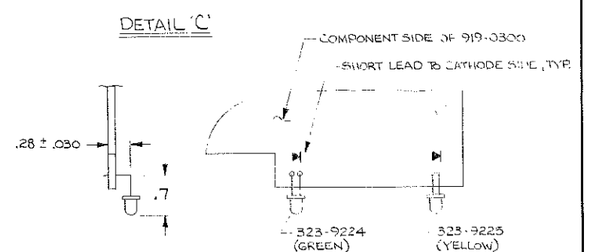
USE HEAT-SHRINK (611-1875) ON ALL PINS

| WIRING OF J11 (418-0006) | |
|---|---|
| PIN No. | WIRE No. |
| 1 | GRN |
| 2 | BLU/WHT |
| 3 | BLK/WHT |
| 4 | BLU |
| 5 | BLK |
| 6 | BRN |

| WIRING OF P2 (419-0670) | |
|---|---|
| PIN No. | WIRE No. |
| 1 | RED |
| 2 | YEL |
| 3 | RED/YEL |
| 4 | YEL |
| 5 | |
| 6 | RED |




COPYRIGHT © 1988 BROADCAST ELECTRONICS, INC.

PROPRIETARY RIGHTS are included in information disclosed hereto. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
xx ± .015 ANGLES ± 1°

DWN. BY MSE 10-5-88
CHKD MH 11-1-88
ME
PROJ. ENGR. J Tucker 11-1-87
MFG.
NEXT ASSY.

MATERIAL SEE B/M 909-0127-004
FINISH
SEE DWG. RA592-0900

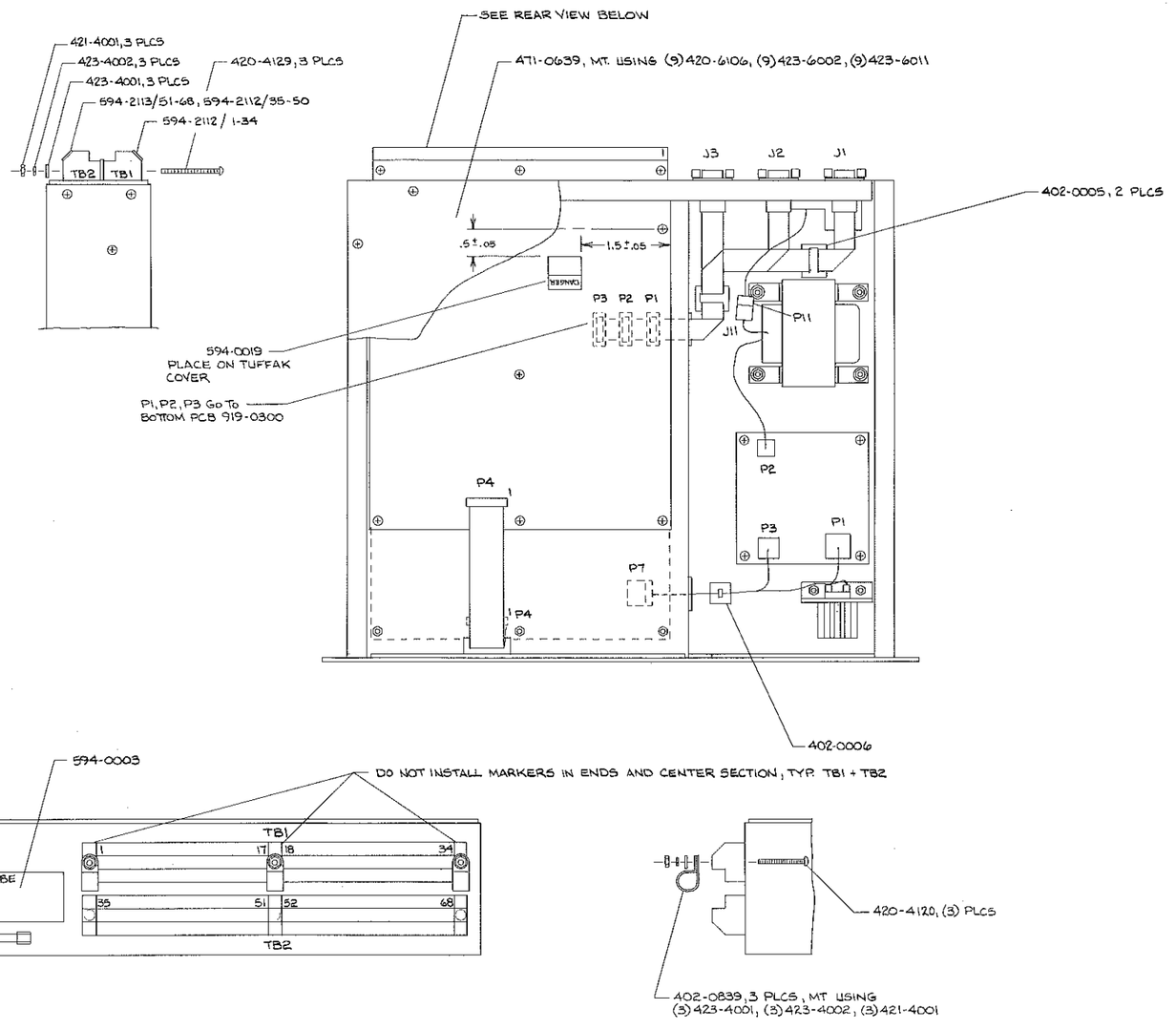
BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O. BOX 3606, QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE ASSY MULTIPLE TRANSMITTER INTERFACE

TYPE A | SIZE D | DWG. NO. 909-0127-004 | REV A

MODEL MVDS EXTE CNTL | SCALE 1/2 | SHEET 1 OF 2

COPYRIGHT © 1988 BROADCAST ELECTRONICS, INC.




REAR VIEW

COPYRIGHT © 1988 BROADCAST ELECTRONICS, INC.

PROPRIETARY RIGHTS are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY MSE 10-5-88
CHKD MH 11-1-88
ENG
PROJ. ENGR. 11-1-88
MFG.

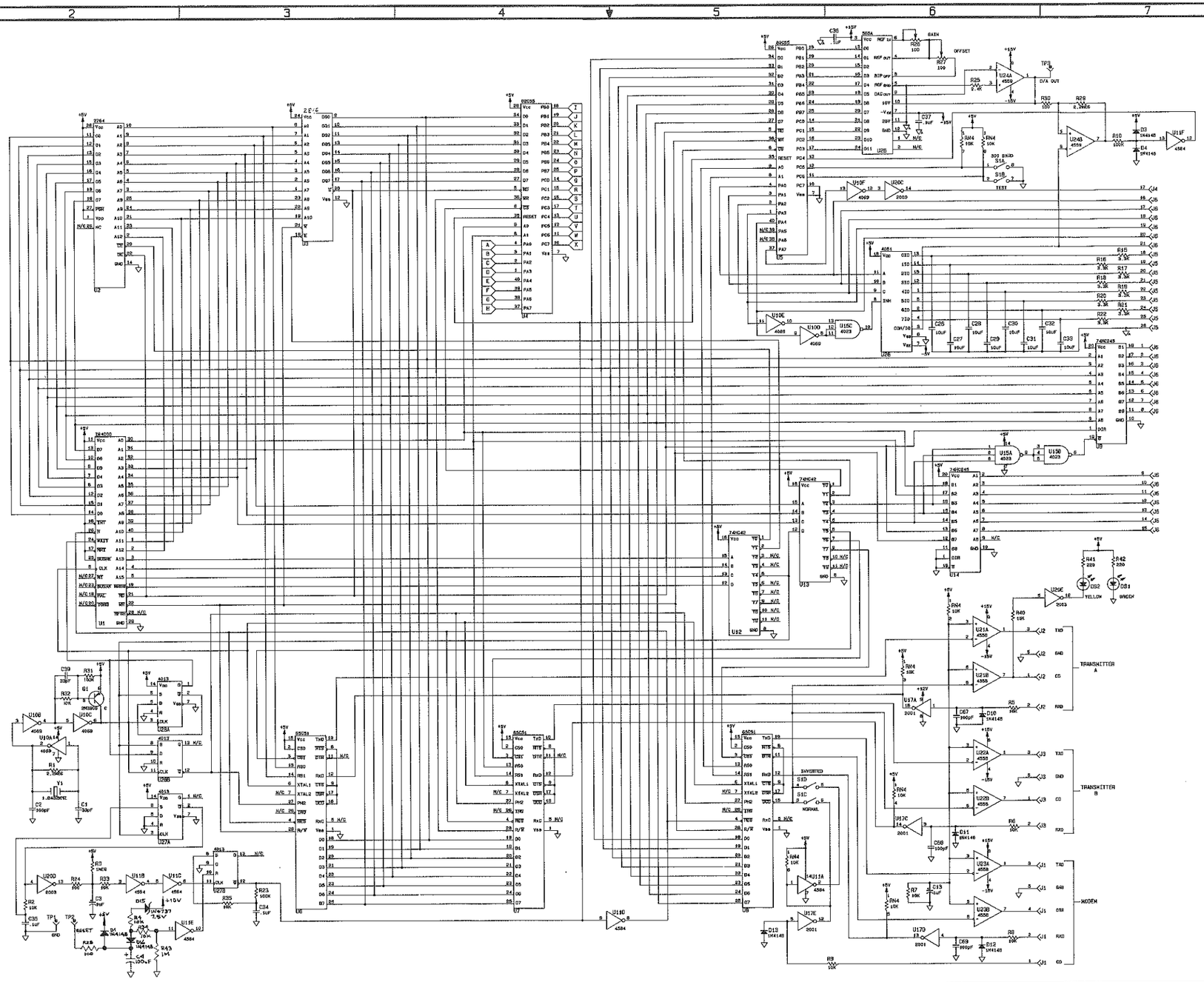
MATERIAL SEE B/M 909-0127-004
FINISH
SEE DWG RA592-0000
NEXT ASSY.

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O. BOX 3506 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE ASSY MULTIPLE TRANSMITTER INTERFACE

| TYPE | SIZE | DWG. NO. | REV |
|---|---|---|---|
| A | D | 909-0127-004 | A |

MODEL MVDS RMTE CNTL SCALE 1/2 SHEET 2 OF 2



COPYRIGHT © 1988 BROADCAST ELECTRONICS, INC.

COPYRIGHT © 1988 BROADCAST ELECTRONICS, INC.

PROPRIETARY RIGHTS are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

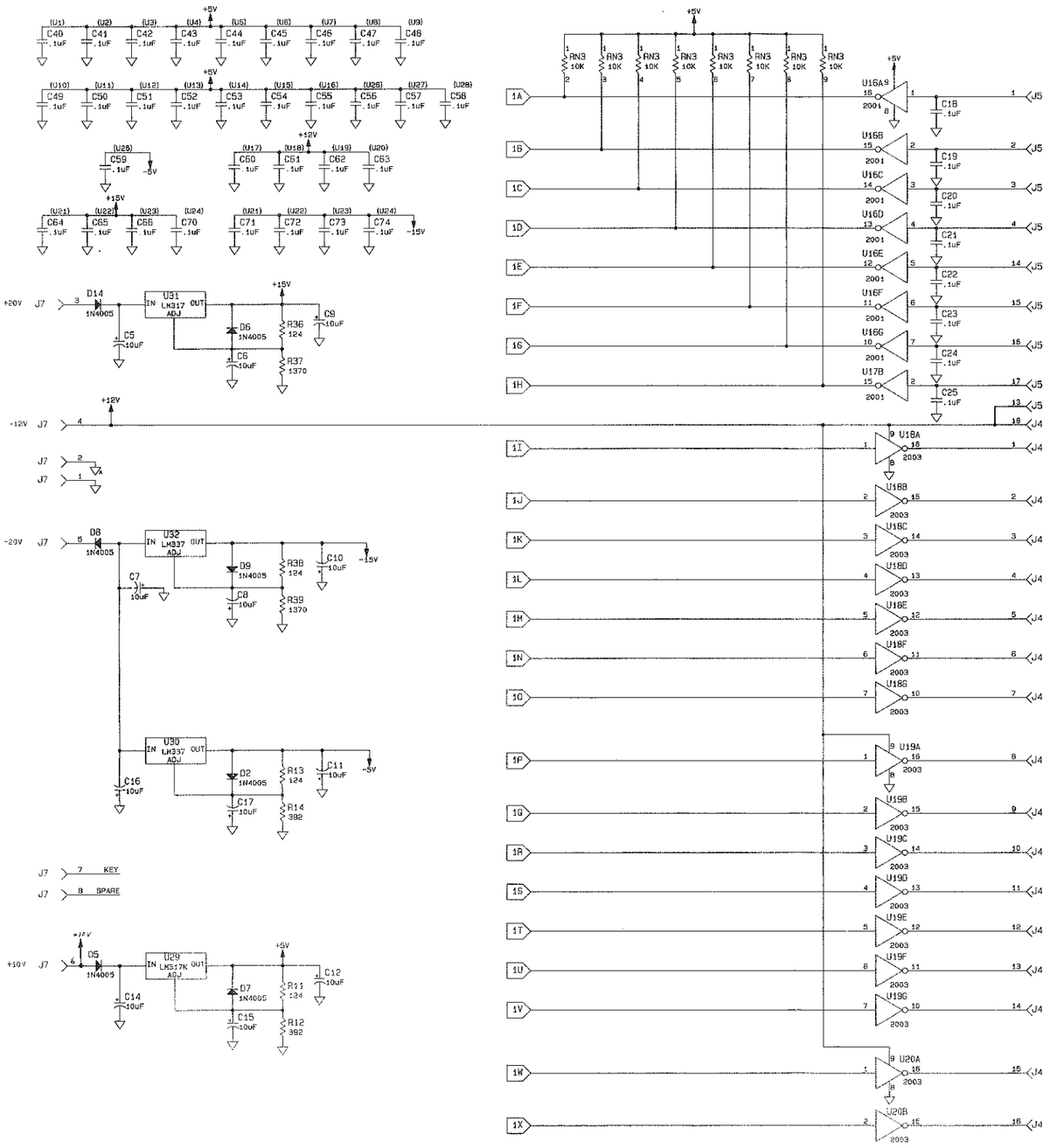
| | |
|---|---|
| DWN. BY | JAH 8-14-87 |
| CHKD | |
| ME | |
| PROJ. ENGR. | |
| MFR. | |
| TOLERANCE (DECIMAL) U.O.G. | .x ± .030 .xxx ± .005 .xx ± .015 ANGLES ± 1° |
| MATERIAL | SEE B/M 919-0300 |
| FINISH | --- |
| | SEE DWG RA592-0000 |
| NEXT ASSY. | 909-0127 |

BROADCAST ELECTRONICS INC.
4100 N.24TH ST., P.O.BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST FAX 217/224-9607

TITLE: CPU BOARD

| TYPE | SIZE | DWG. NO. | REV |
|---|---|---|---|
| S | D | 919-0300 | D |

MODEL MT-3 | SCALE NONE | SHEET 1 OF 2




NOTES:

1. ALL RESISTORS IN OHMS, 1/4W, 5% UNLESS OTHERWISE SPECIFIED.
2. LAST COMPONENTS USED: R43, C74, D16, U32, J7, G1, S1, Y1, DS2, & TP3
3. COMPONENTS NOT USED: C38
4. SEE PCB ASSEMBLY: AD 919-0300

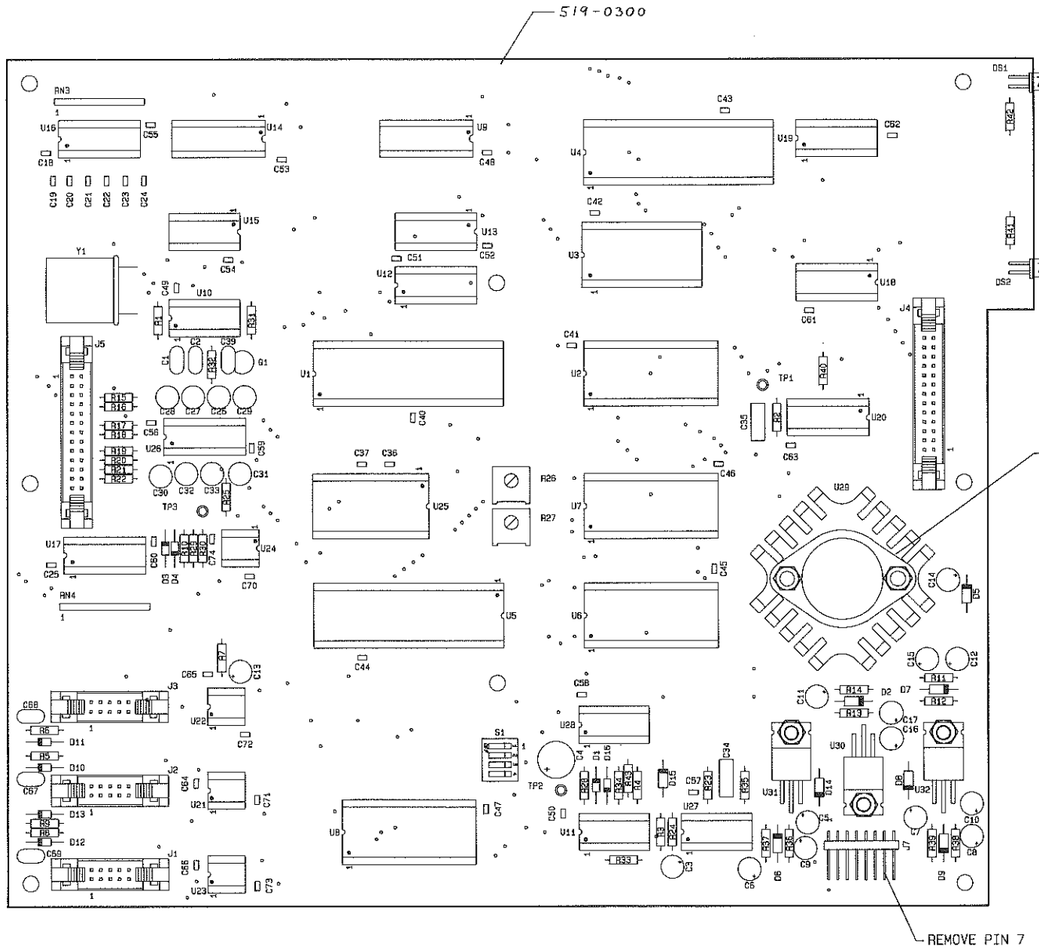
COPYRIGHT © 1988 BROADCAST ELECTRONICS, INC.

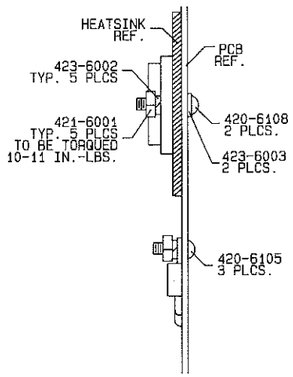
PROPRIETARY RIGHTS are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

| | | | |
|---|---|---|---|
| DWN. BY JAH 8-17-87 | MATERIAL SEE B/M 919-0300 | BROADCAST ELECTRONICS INC. | |
| CHKD | | 4100 N.24TH ST.,P.O.BOX 3606 QUINCY,IL 62305 217/224-9600 TELEX 250142 CABLE BROADCAST FAX 217/224-9607 | |
| ME | FINISH ---- | TITLE CPU BOARD | |
| PROJ. ENGR. | SEE DWG #A552-0000 | TYPE S SIZE D DWG. NO. 919-0300 | REV D |
| MFG. | NEXT ASSY. 909-0127 | MODEL MT-3 SCALE NONE | SHEET 2 OF 2 |

TOLERANCE (DECIMAL) U.O.S. .X ± .030 .XXX ± .005 .XX ± .015 ANGLES ± 1°

COPYRIGHT © 1988 BROADCAST ELECTRONICS, INC.




NOTES:

1. LAST COMPONENT USED: C74, D16, DS2, J7, Q1, R43, S1, TP3, U32, & Y1.
2. SEE SCHEMATIC: SD919-0300

COPYRIGHT © 1991 BROADCAST ELECTRONICS, INC.

PROPRIETARY RIGHTS are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

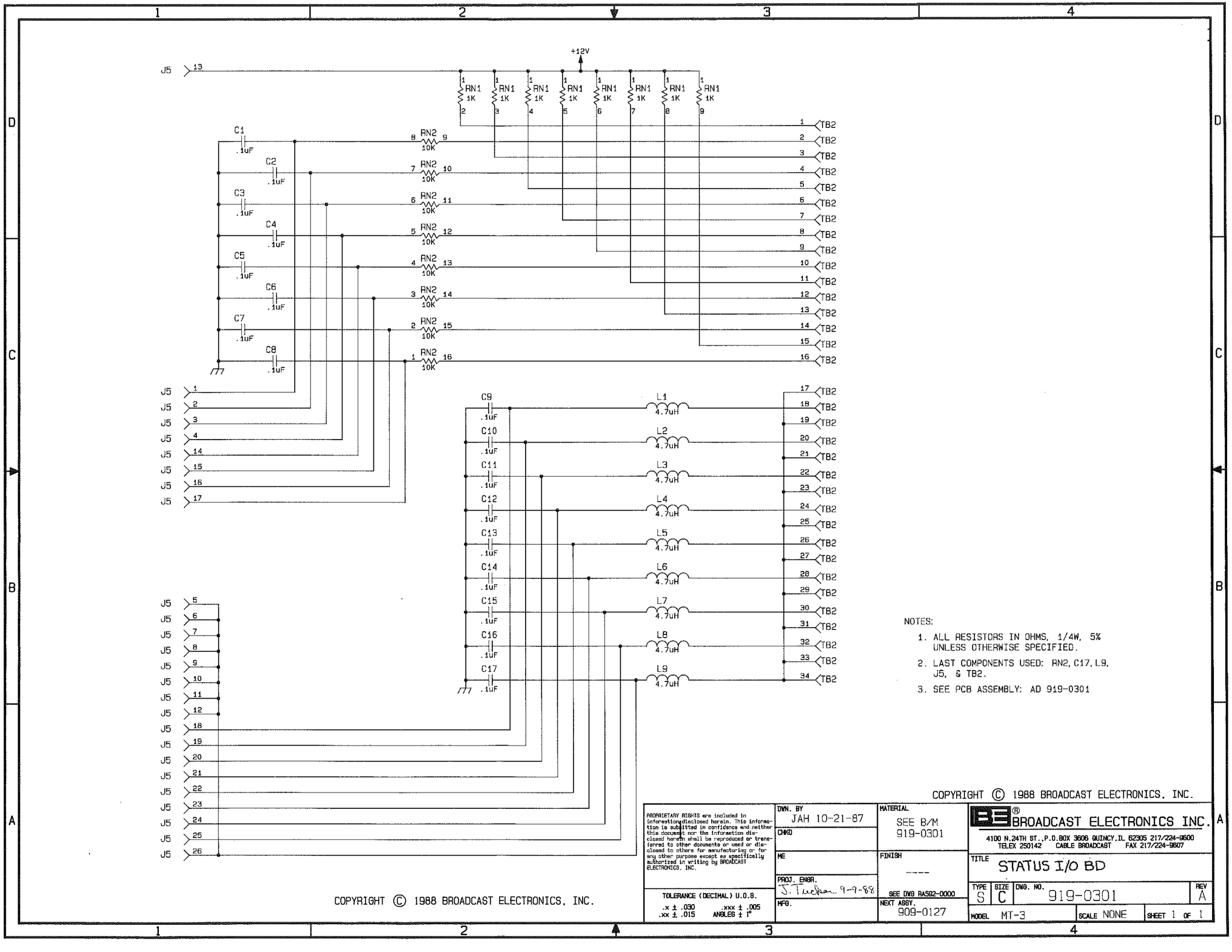
TOLERANCE (DECIMAL) U.O.S.
.X ± .030 .XXX ± .005
.XX ± .015 ANGLES + 1°

| | |
|---|---|
| DWN. BY | KLS 12-17-87 |
| CHKD | |
| ME | JHS 9-9-88 |
| PROJ. ENGR. | JLT 9-9-88 |
| MFG. | DBN 9-9-88 |
| MATERIAL | SEE BOM 919-0300 |
| FINISH | SEE DWG RA592-0000 |
| NEXT ASSY. | |

BROADCAST ELECTRONICS INC.
4100 N.24TH ST. P.O.BOX 3606 QUINCY, IL. 62305 PH. 217/224-9600
TELEX 250142 CABLE BROADCAST FAX 217/224-9607

| | | | |
|---|---|---|---|
| TITLE | PCB ASSEMBLY CPU | | |
| TYPE A | SIZE C | DWG No. 919-0300 | REV G |
| MODEL MT-3 | SCALE 1:1 | SHEET 1 OF 1 | |

COPYRIGHT © 1991 BROADCAST ELECTRONICS, INC.




NOTES:

1. ALL RESISTORS IN OHMS, 1/4W, 5% UNLESS OTHERWISE SPECIFIED.
2. LAST COMPONENTS USED: RN2, C17, L9, J5, & TB2.
3. SEE PCB ASSEMBLY: AD 919-0301

COPYRIGHT © 1988 BROADCAST ELECTRONICS, INC.

COPYRIGHT © 1988 BROADCAST ELECTRONICS, INC.

PROPRIETARY RIGHTS are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

DWN. BY JAH 10-21-87
CHKD
ME
PROJ. ENGR. J. Tuckson 9-9-88
MFG.

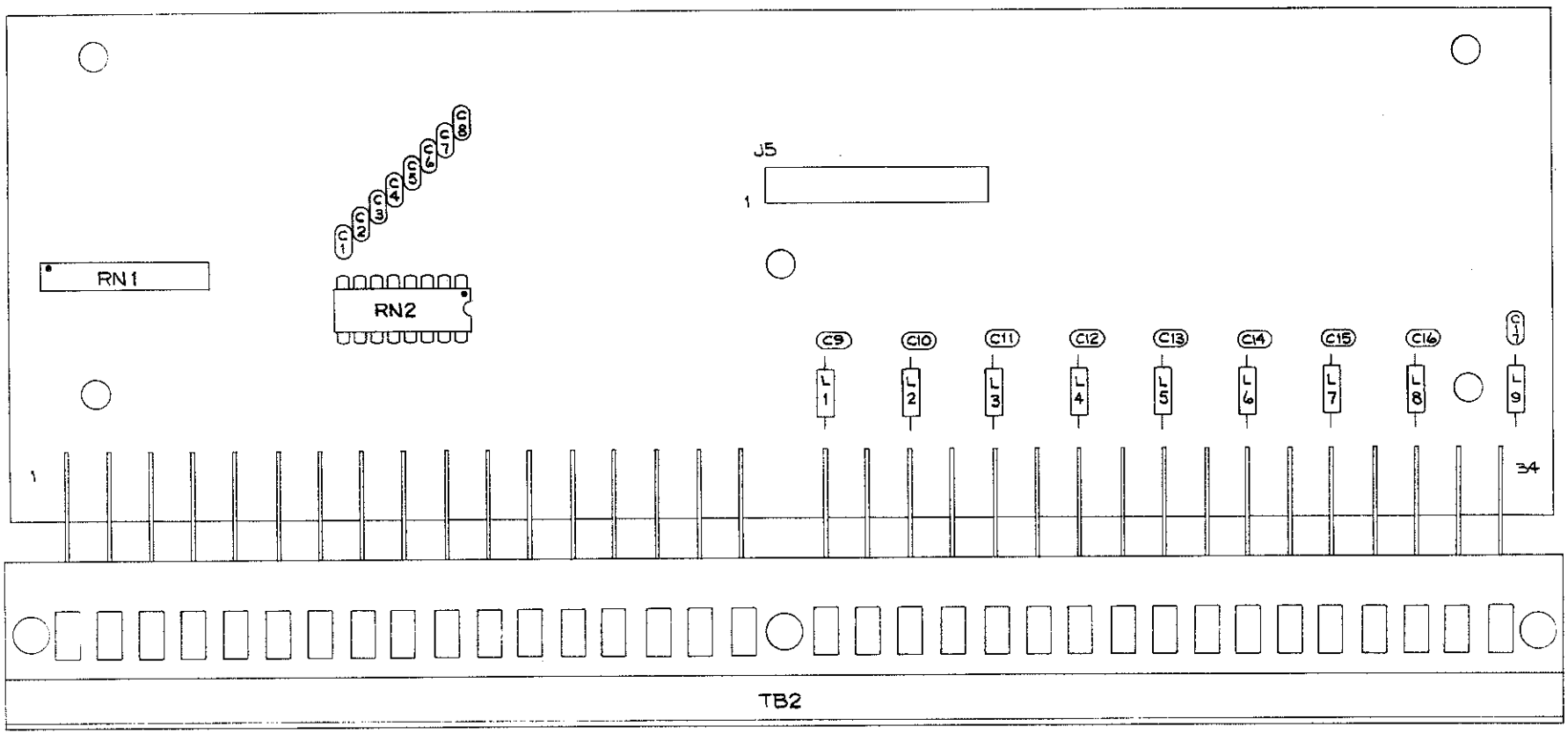
MATERIAL SEE B/M 919-0301
FINISH ----
SEE DWG RA592-0000
NEXT ASSY. 909-0127

BROADCAST ELECTRONICS INC.
4100 N.24TH ST.,P.O.BOX 3606 QUINCY,IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST FAX 217/224-9607

TITLE STATUS I/O BD

TYPE S | SIZE C | DWG. NO. 919-0301 | REV A

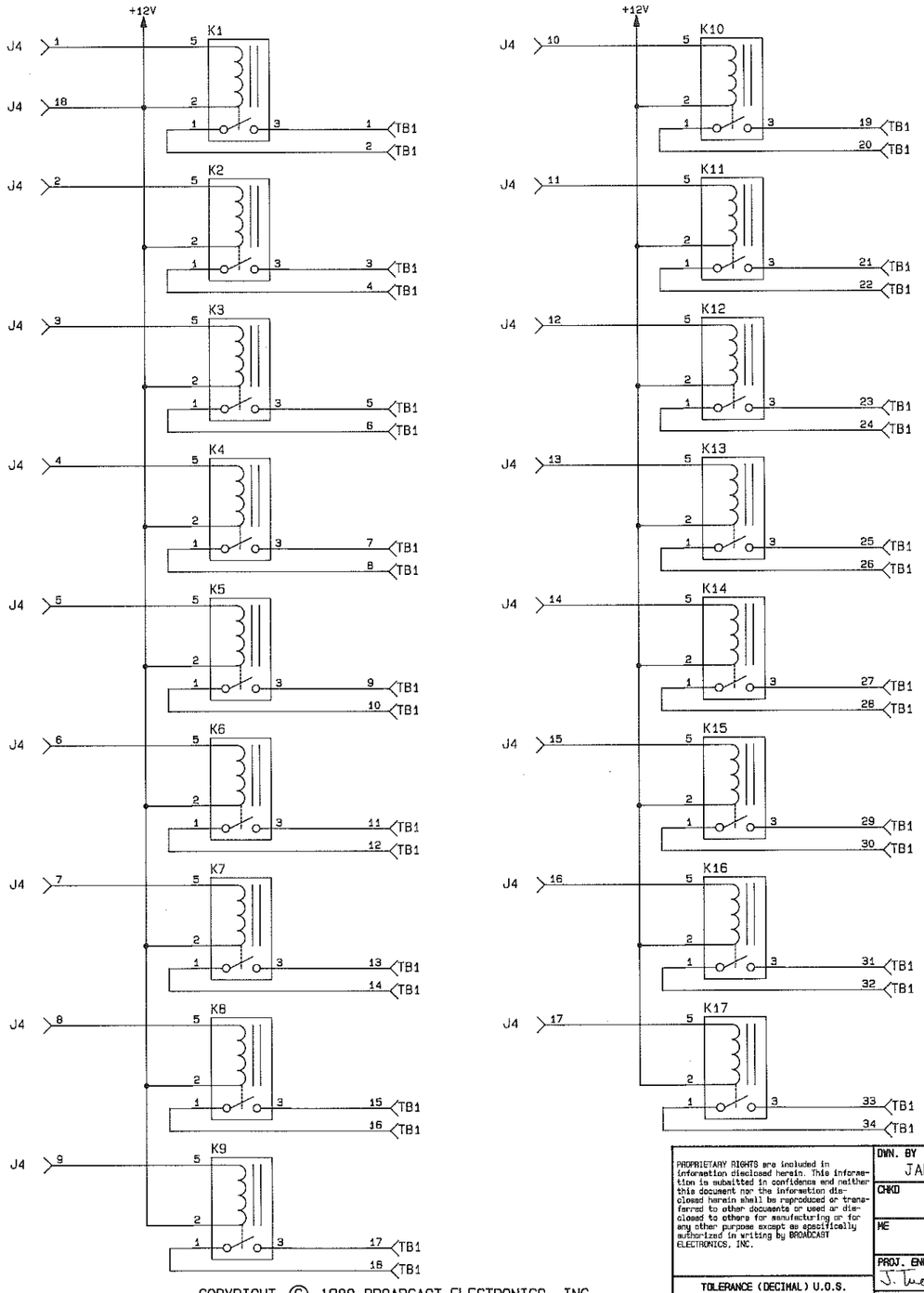
MODEL MT-3 | SCALE NONE | SHEET 1 OF 1




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

**597–0122–43**

**FIGURE 7–6. STATUS I/O CIRCUIT BOARD ASSEMBLY (AD919–0301)**




NOTES:

1. LAST COMPONENTS USED: K17, J4, & TB1.
2. SEE PCB ASSEMBLY: AD 919-0302

COPYRIGHT © 1988 BROADCAST ELECTRONICS, INC.

COPYRIGHT © 1988 BROADCAST ELECTRONICS, INC.

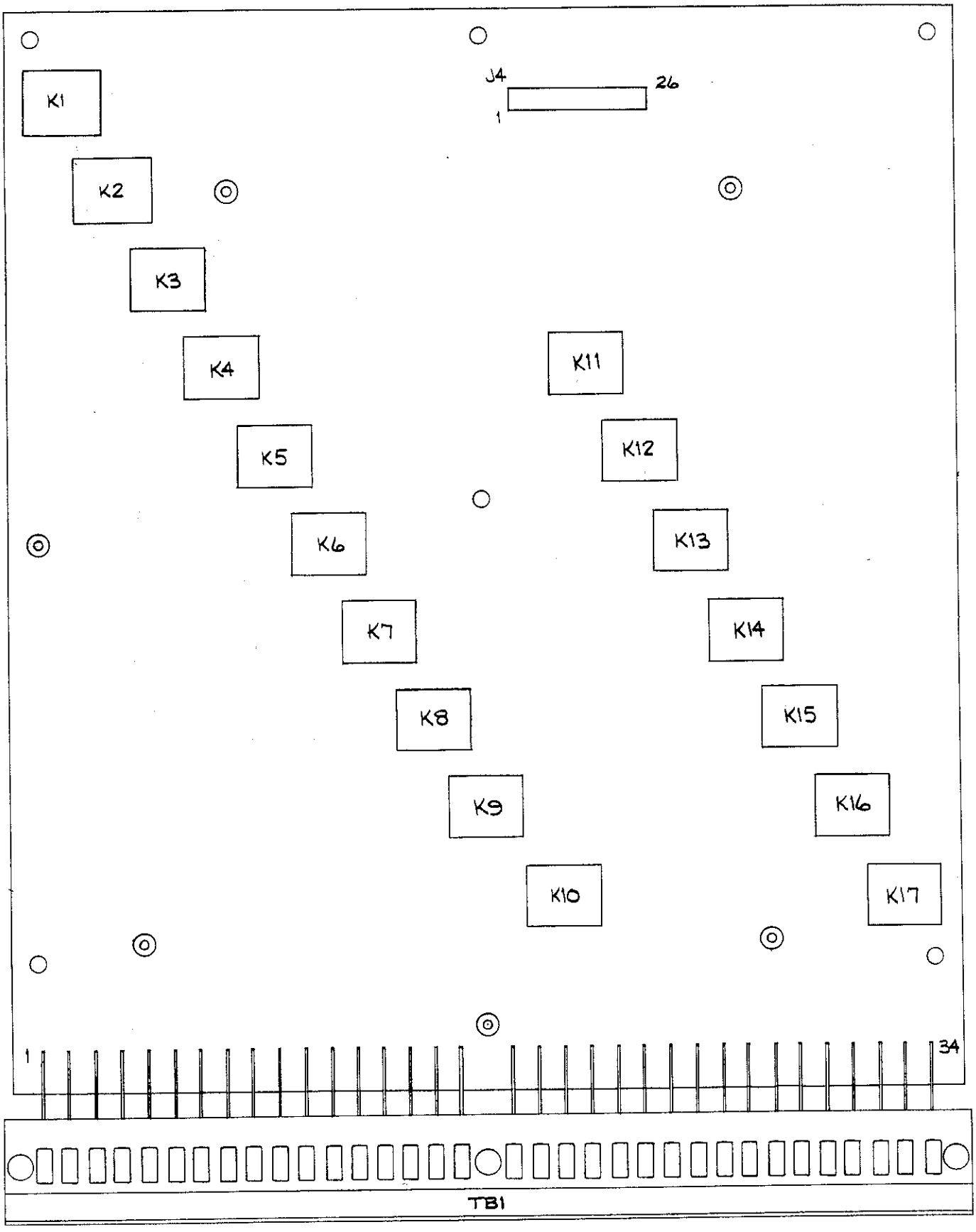
PROPRIETARY RIGHTS are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1°

| | |
|---|---|
| DWN. BY | JAH 10-23-87 |
| CHKD | |
| ME | |
| PROJ. ENGR. | J. Tucker 9-9-88 |
| MFG. | [illegible] 9-9-88 |
| MATERIAL | SEE B/M 919-0302 |
| FINISH | ---- |
| | SEE DWG RA592-0000 |
| NEXT ASSY. | 909-0127 |

BROADCAST ELECTRONICS INC.
4100 N.24TH ST.,P.O.BOX 3606 QUINCY,IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST FAX 217/224-9607

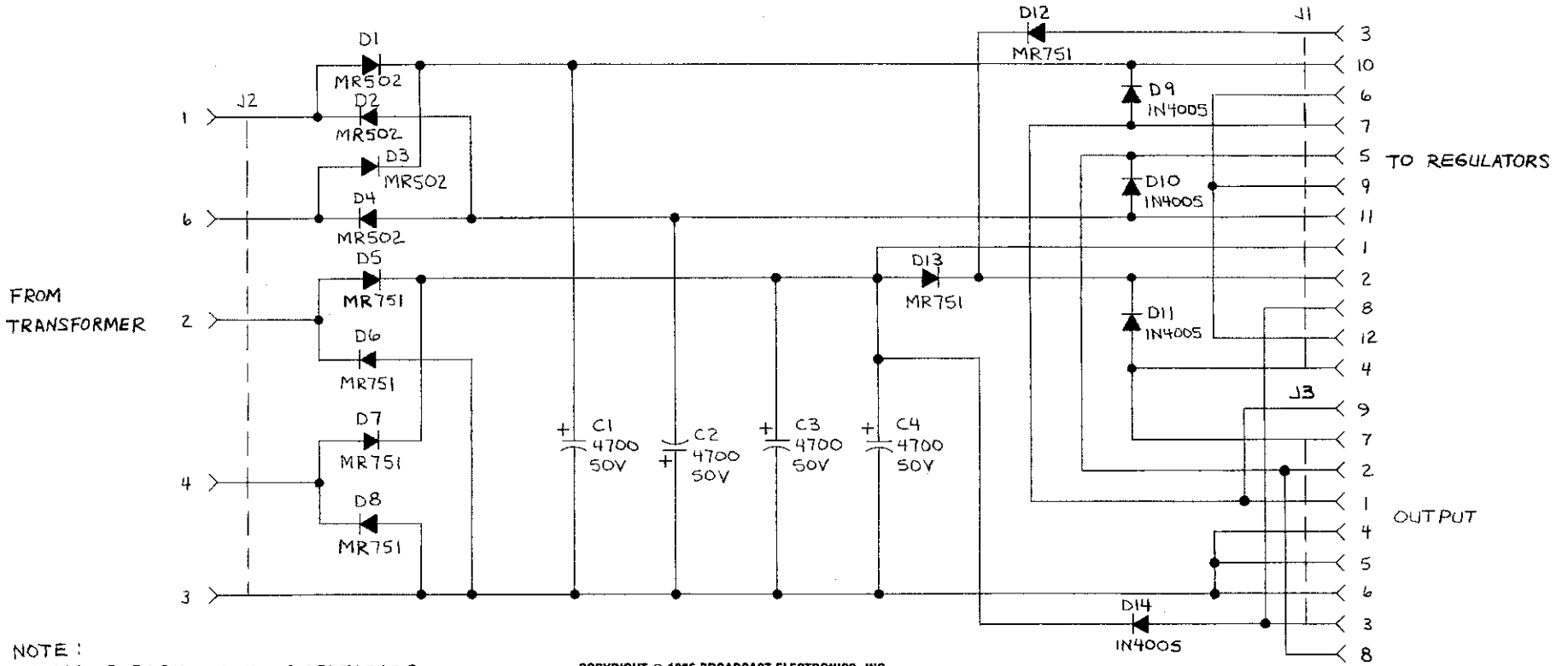
| | | | | |
|---|---|---|---|---|
| TITLE | RELAY I/O BD | | | |
| TYPE S | SIZE C | DWG. NO. 919-0302 | | REV A |
| MODEL MT-3 | | SCALE NONE | SHEET 1 OF 1 | |




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597-0122-44

**FIGURE 7-8. RELAY I/O CIRCUIT BOARD ASSEMBLY (AD919-0302)**




NOTE:
1. ALL CAPACITORS IN MICROFARADS.
2. COMPONENTS LAST USED:
   C4, D14, J3
3. SEE ASSY. # AC910-0105
   SEE B/M # 910-0105

COPYRIGHT © 1986 BROADCAST ELECTRONICS, INC.

PROPRIETARY RIGHTS are included in information disclosed herein. This information is submitted in confidence and neither this document nor the information disclosed herein shall be reproduced or transferred to other documents or used or disclosed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.

TOLERANCE (DECIMAL) U.O.S.
.x ± .030 .xxx ± .005
.xx ± .015 ANGLES ± 1

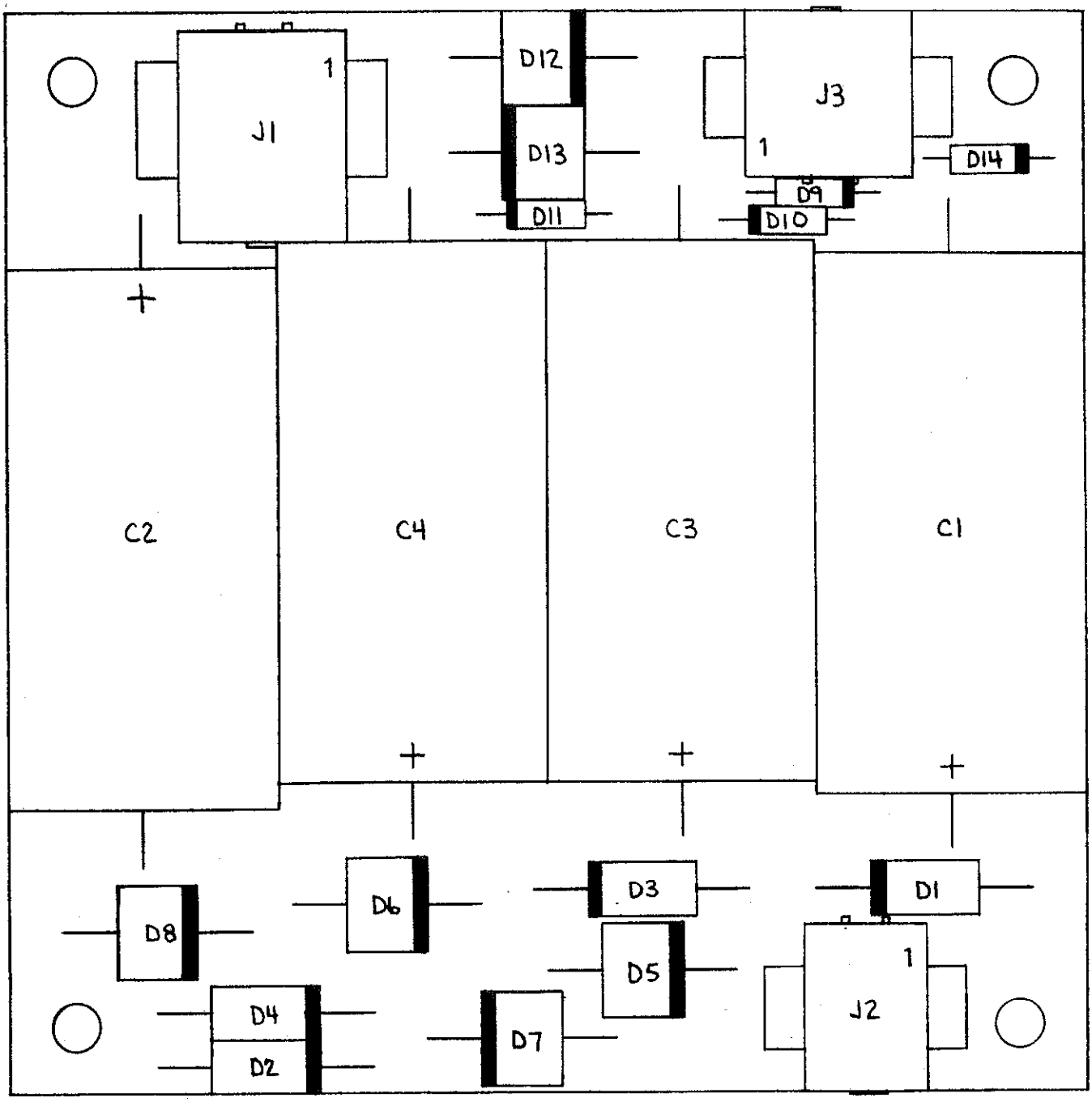
| | | |
|---|---|---|
| DWN. BY SLEE 7-14-86 | | MATERIAL |
| CHKD MH 7-21-86 | | |
| ME | | FINISH |
| PROJ. ENGR. J. Tucker 2-3-87 | | |
| MFG. | | NEXT ASSY. |

BROADCAST ELECTRONICS INC.
4100 N. 24TH ST., P.O.BOX 3606 QUINCY, IL 62305 217/224-9600
TELEX 250142 CABLE BROADCAST

TITLE SCHEMATIC, POWER SUPPLY BOARD

| TYPE | SIZE | DWG. NO. | REV |
|---|---|---|---|
| S | B | 910-0105 | B |

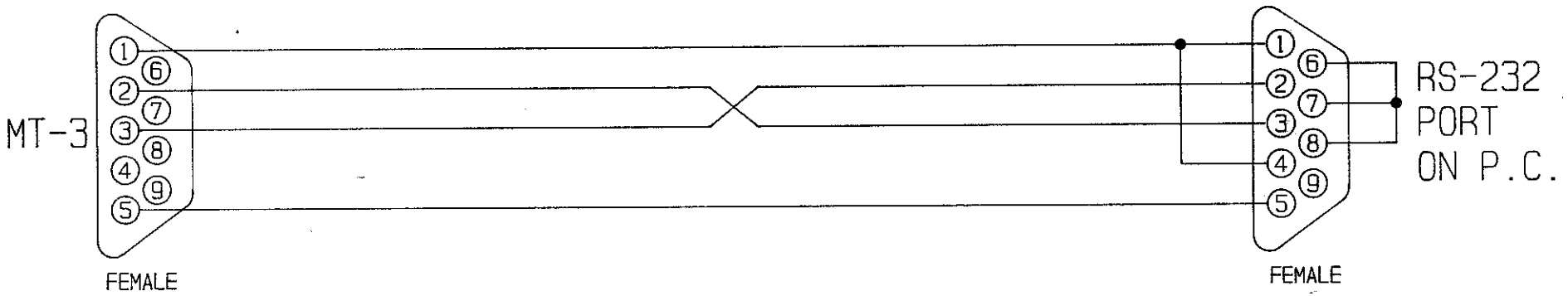
MODEL DV2 & MT-3 SCALE NTS SHEET 1 OF 1

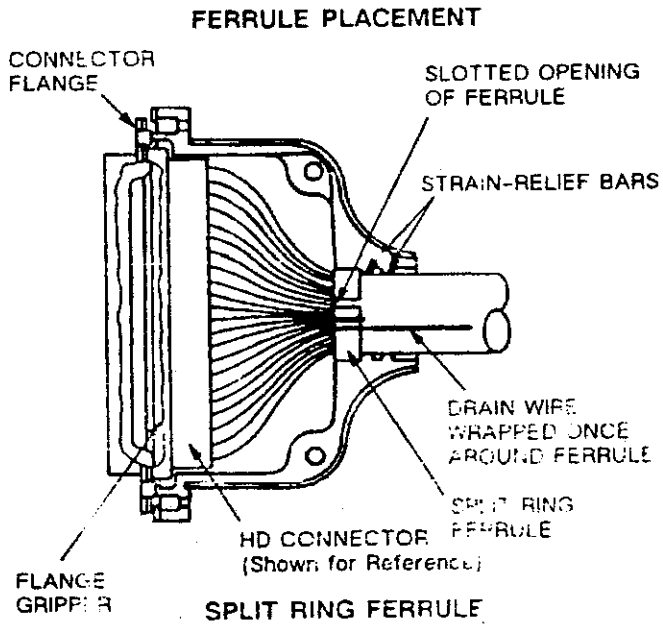



COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597–0122–45

**FIGURE 7–10. POWER SUPPLY CIRCUIT BOARD ASSEMBLY (AC910–0105)**




COPYRIGHT © 1990 BROADCAST ELECTRONICS, INC

597-0122-31

NOTE: IF THE PERSONAL COMPUTER IS EQUIPPED WITH A 25-PIN RS-232 PORT, USE THE 25-PIN TO 9-PIN ADAPTOR LOCATED IN THE MT-3 ACCESSORY KIT P/N 979-0127.

**FIGURE 7-11. MT-3 INTERFACE CABLE DIAGRAM**

MT-3 TO P.C. CABLE ASSEMBLY DIAGRAM

# PRODUCT WARRANTY

LIMITED TWO YEAR

While this warranty gives Purchaser specific legal rights, which terminate two (2) years (one year on cartridge and blower motors) from the date of shipment, Purchaser may also have other rights which vary state to state.

Broadcast Electronics, Inc. ("Seller") hereby warrants cartridge machines, consoles, and other new Equipment manufactured by Seller against any defects in material or workmanship at the time of delivery thereof, that develop under normal use within a period of two (2) years (one year for cartridge and blower motors) from the date of shipment, as such term is defined herein. Other manufacturer's and suppliers' Equipment and services, if any, including electronic tubes, solid state devices, transmission line, antennas, towers, related equipment and installation and erection services, shall carry only such manufacturer's or suppliers' standard warranty. This warranty extends to the original user and any subsequent purchaser during the warranty period. Seller's sole responsibility with respect to any equipment or parts not conforming to this warranty is to replace such equipment or parts upon the return thereof F.O.B. Seller's factory or authorized repair depot within the period aforesaid.

In the event of replacement pursuant to the foregoing warranty, only the unexpired portion of the warranty from the time of the original purchase will remain in effect for any such replacement. However, the warranty period will be extended for the length of time that Purchaser is without the services of the Equipment due to its being serviced pursuant to this warranty. The terms of the foregoing warranty shall be null and void if the Equipment has been altered or repaired without specific written authorization of Seller, or if Equipment is operated under environmental conditions or circumstances other than those specifically described in Seller's product literature or instruction manual which accompany the Equipment. Seller shall not be liable for any expense of any nature whatsoever incurred by the original user without prior written consent of Seller.

Seller shall not be liable to Purchaser for any and all incidental or consequential damages for breach of either expressed or implied warranties. However, some states do not allow the exclusion or limitation of incidental or consequential damages, so the above limitation or exclusion may not apply to Purchaser. All express and implied warranties shall terminate at the conclusion of the period set forth herein. Any card which is enclosed with the equipment will be used by Seller for survey purposes only.

If the Equipment is described as used, it is sold as is and where is. If the contract covers equipment not owned by Seller at this date, it is sold subject to Seller's acquisition of possession and title.

**EXCEPT AS SET FORTH HEREIN, AND EXCEPT AS TO TITLE, THERE ARE NO WARRANTIES, OR ANY AFFIRMATIONS OF FACT OR PROMISES BY SELLER, WITH REFERENCE TO THE EQUIPMENT, OR TO MERCHANTABILITY, FITNESS FOR A PARTICULAR APPLICATION, SIGNAL COVERAGE, INFRINGEMENT, OR OTHERWISE, WHICH EXTEND BEYOND THE DESCRIPTION OF THE EQUIPMENT ON THE FACE HEREOF.**

BROADCAST ELECTRONICS, INC.
4100 North 24th Street, P.O. Box 3606, Quincy, Illinois 62305