INSTRUCTION MANUAL

DV-2A DIGITAL AUDIO RECORDER

March, 1990

IM No. 597-0110

BROADCAST ELECTRONICS, INC.



IMPORTANT INFORMATION

EQUIPMENT LOST OR DAMAGED IN TRANSIT

When delivering the equipment to you, the truck driver or carrier's agent will present a receipt for your signature. Do not sign it until you have (a) inspected the containers for visible signs of damage and (b) counted the containers and compared with the amount shown on the shipping papers. If a shortage or evidence of damage is noted, insist that notation to that effect be made on the shipping papers before you sign them.

Further, after receiving the equipment, unpack it and inspect thoroughly for concealed damage. If concealed damage is discovered, immediately notify the carrier, confirming the notification in writing, and secure an inspection report. This item should be unpacked and inspected for damage WITHIN 15 DAYS after receipt. Claims for loss or damage will not be honored without proper notification of inspection by the carrier.

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Phone (217) 224-9600 Customer Service

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Do not return any merchandise without our written approval and Return Authorization. We will provide special shipping instructions and a code number that will assure proper handling and prompt issuance of credit. Please furnish complete details as to circumstances and reasons when requesting return of merchandise. All returned merchandise must be sent freight prepaid and properly insured by the customer.

REPLACEMENT PARTS

Replacement and Warranty Parts may be ordered from the address below. Be sure to include equipment model and serial number and part description and part number.

Broadcast Electronics, Inc. 4100 N. 24th St., P.O. Box 3606 Quincy, Illinois 62305 Tel: (217) 224-9600 Telex: 25-0142

Cable: BROADCAST Fax: (217) 224-9607

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MODIFICATIONS

Broadcast Electronics, Inc. reserves the right to modify the design and specifications of the equipment in this manual without notice. Any modifications shall not adversely affect performance of the equipment so modified.

TABLE OF CONTENTS

PARAGRAPH		PAGE NO
SECTION I 1-1 1-3 1-5 1-7 1-9 1-11 1-12 1-13 1-15	GENERAL INFORMATION Introduction Equipment Description Electrical Description Audio Circuitry Memory Circuitry Control Circuitry Remote Control Physical Description Equipment Description	1-1 1-1 1-2 1-2 1-2 1-2 1-2 1-2 1-3
SECTION II 2-1 2-3 2-6 2-8 2-10 2-12 2-13 2-16 2-18 2-19 2-20 2-25 2-26 2-30 2-31	INSTALLATION Introduction Unpacking Installation Requirements Installation Preliminary Installation DV-2A Circuit Board Programming Input Voltage Check Placement Wiring Audio Input/Output Connections Remote Connections Automatic Sequencing Emergency Power Systems Installation Adjustments Output Level Adjustment	2-1 2-1 2-1 2-1 2-1 2-2 2-2 2-3 2-3 2-3 2-3 2-5 2-6 2-6
SECTION III 3-1 3-3 3-5 3-6 3-8 3-9 3-10 3-11 3-12 3-13 3-14 3-20 3-26 3-27 3-30 3-31 3-36 3-41 3-43	OPERATION Introduction Controls and Indicators Operation Preliminary Operation Record/Playback Functions Reset Pause Remaining Time Record Operation Program Material Preliminary Record Operation Recording Program Material Special Record Functions Playback Operation Special Playback Functions Repeat Operation Continuous Playback Operation Memory Clear Audio Monitoring	3-1 3-3 3-3 3-3 3-5 3-5 3-5 3-5 3-6 3-6 3-6 3-7 3-7

PARAGRAI	<u>PH</u>	PAGE NO.
SECTION	IV THEORY OF OPERATION	
4-1	Introduction	4-1
4-3	Functional Description	4-1
4-4	Record Circuit	4-1
4-10	Audio Input Indicator Circuit	4-2
4-12	Audio Sampling Circuit	4-2
4-16	Microprocessor and Interface Circuitry	4-9
4-17	General	4-9
4-18	Read-Only-Memory (ROM)	4-9
4-19	Microprocessor	4-9
4-20 4-21	Microprocessor Interface Circuit	4-9
4-21	Microprocessor Clock Circuit	4-10
4-29	Timing Circuit	4-10
4-34	Address Circuitry Data Sampling and Momeny White Openation	4-11
4-37	Data Sampling and Memory Write Operation Memory Read and Data Output Operation	4-12 4-12
4-41	Time/Selection Display Write Operation	4-12
4-42	Front-Panel/Remote Indicator Write	4-13 4-13
, , ,	Operation	4-13
4-43	End-Of-Message Circuitry	4-13
4-44	Refresh Circuit	4-13
4-47	Interrupt Logic	4-14
4-48	Reset Logic	4-14
4-49	Mode Control Circuit	4-14
4-53	Memory Circuit	4-15
4-59	Playback Audio Circuit	4-15
4-62	Output Driver Circuit	4-16
4-63	Headphone Circuit	4-16
4-65 4-69	Power Supply Circuit	4-16
4-09	Emergency Power Systems	4-16
SECTION	· · · · · · · · · · · · · · · · · · ·	
5-1	Introduction	5-1
5-3	Safety Considerations	5-1
5 - 5	First Level Maintenance	5-1
5-7	General	5-1
5 - 9	Internal Battery Back-Up System	5-1
5-11 5-13	Secondary Battery Back-Up System	5-2
5-16	Second Level Maintenance Electrical Adjustments	5-2 5-2
5 - 18	Audio Circuit Board Adjustments	5-2 5-2
5-19	Record Circuit Audio Filter Alignment	5-2
5-20	Playback Circuit Audio Filter Alignment	5-2
5-21	Output Level Adjustment	5-2
5-22	Sample and Hold Circuit Input Level	5-3
	Calibration	- •
5-35	Audio Input Indicator Calibration	5-5
5-46	Troubleshooting	5-6

<u>PARAGRAPH</u>		PAGE NO.
5-50 5-51 5-52 5-58	Memory Circuit Board Troubleshooting CPU Circuit Board Troubleshooting Component Replacement Integrated Circuits	5-6 5-11 5-11 5-12
SECTION VI 6-1	PARTS LISTS Introduction	6-1
SECTION VII 7-1	DRAWINGS Introduction	7-1
APPENDIX A A-1	MANUFACTURERS DATA Introduction	A-1
	LIST OF ILLUSTRATIONS	
FIGURE 1-1 2-1 2-2 2-3 3-1 4-1 5-1 5-2 5-3	DESCRIPTION DV-2A Digital Audio Recorder DV-2A Circuit Board Jumper Programming Remote Control Emergency Power System, Battery Installation DV-2A Controls and Indicators DV-2A Simplified Schematic Audio Circuit Board Adjustment Controls Troubleshooting Tree, No Record Audio Troubleshooting Tree, No Playback Audio	PAGE NO. 1-1 2-2 2-4 2-6 3-4 4-3 5-4 5-9 5-8
	LIST OF TABLES	
TABLE NO. 1-1 3-1 5-1 5-2 6-1	DESCRIPTION DV-2A Electrical, Physical, and Environmental Specifications Controls and Indicators DV-2A Troubleshooting Memory Circuit Board Troubleshooting Replaceable Parts Lists	PAGE NO. 1-3 3-1 5-6 5-11 6-1

SECTION I GENERAL INFORMATION

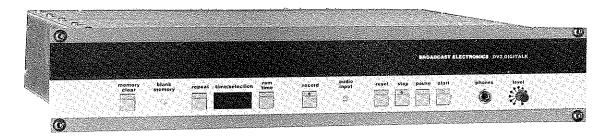
1-1. INTRODUCTION.

1-2. Information presented by this section provides a general description of the Broadcast Electronics DV-2A digital audio recorder and lists equipment specifications.

1-3. EQUIPMENT DESCRIPTION.

1-4. The Broadcast Electronics DV-2A is a totally solid-state digital audio record/playback device designed for continuous playback applications (refer to Figure 1-1). The unit features a six minute and twenty-nine second memory capacity. A random access design allows the recording of up to 79 individual audio messages. A comprehensive remote control system provides the interfacing required for manual or automated external control. The following text presents ordering information and recommended spare parts kits.

MODEL	PART NO.	DESCRIPTION
DV-2A	900-1000-001	DV-2A Digital Audio Recorder, 19 inch (48.21 cm) rack mount, 117V ac 60 Hz operation.
DV-2A	900-1000-301	DV-2A Digital Audio Recorder, 19 inch (48.21 cm) rack mount, 220V ac 50 Hz operation.
	970-0096	Recommended Spare Parts Kit for the DV-2A digital audio recorder. Includes selected semi-conductors, potentiometers, crystals, indicators, and switches etc.



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FIGURE 1-1. DV-2A DIGITAL AUDIO RECORDER

1-5. ELECTRICAL DESCRIPTION.

- 1-6. The DV-2A is a completely solid-state digital audio recorder designed for continuous playback operations. Several advanced circuit applications are employed to provide flexible and reliable playback/record service.
- 1-7. AUDIO CIRCUITRY. The DV-2A audio input circuitry is designed with a programmable instrumentation amplifier to allow the recording of microphone or line level inputs. The input circuitry also features an automatic-gain-control (AGC) circuit which acts to maintain a precision input record level.
- 1-8. The audio output circuit features a DYNAFEX $^{\circledR}$ noise reduction system to enhance the quality of the reproduced signal. The audio output receptacle is transformer balanced and equipped with an XLR connector for convenience. Monitoring of the record or playback audio is provided by a built-in headphone system.
- 1-9. MEMORY CIRCUITRY. Over three megabytes of dynamic RAM is employed to provide a six minute and twenty-nine second memory capacity. All memory control operations are directed by a Z-80 microprocessor. Random access design of the memory control circuit allows the recording and reproduction of up to 79 individual audio messages.
- 1-10. The memory circuit is protected from momentary power failures by an internal battery back-up system. A connection for a secondary external battery back-up system which protects the DV-2A from extended power failures is provided on the rear-panel.
- 1-11. CONTROL CIRCUITRY. All record and playback operating parameters are controlled by front-panel microswitches. Selected microswitches contain indicators to provide easy recognition of operational parameters. A time/selection display provides an indication of remaining memory time or the number of the current audio selection. A bi-color front-panel indicator displays the condition of the audio input level.
- 1-12. REMOTE CONTROL. The DV-2A is designed for complete remote control operation. The remote control circuitry contains optical couplers to provide a high degree of isolation. An end-of-message (EOM) output and the remote control system format provide the interfacing required for external control of the unit by manual or automated equipment.

1-13. PHYSICAL DESCRIPTION.

- 1-14. The DV-2A is designed for placement in a 19 inch (48.3 cm) rack. The circuitry is arranged in modular assemblies to provide ease of maintenance. All circuit board interconnections are constructed with receptacle/connector devices for service convenience.
- DYNAFEX® is a registered trademark of Circuit Research Laboratories

This equipment is a Class A (or Class B) digital apparatus which complies with the Radio Interference Regulation, CRC c.1374.

1-15. <u>EQUIPMENT SPECIFICATIONS</u>.

1-16. Refer to Table 1-1 for the electrical, physical, and environmental specifications of the DV-2A digital audio recorder.

TABLE 1-1. DV-2A ELECTRICAL, PHYSICAL, AND ENVIRONMENTAL SPECIFICATIONS (Sheet 1 of 2)

PARAMETER	SPECIFICATIONS	
ELECTRICAL		
RECORD TIME	Six minutes and twenty-nine seconds.	
FREQUENCY RESPONSE	+1 dB to -4 dB, 20 Hz to 6500 Hz. Measured with pink noise audio.	
DISTORTION	1.5% or less at a Ø dBv to +18 dBv out- put level into 600 Ohms. 400 Hz ref- erence at an input level from -10 dBv to +10 dBv.	
SIGNAL-TO-NOISE RATIO	56 dB or greater below a +8 dBm output level.	
AUDIO INPUT LEVEL		
Microphone, AGC Enabled	-55 dBv to -25 dBv.	
Line, AGC Enabled	-15 dBv to +20 dBv.	
Line, AGC Disabled	Ø dBv before limiting. +8 dBv ±2 dBv before overload indication. +20 dBv maximum.	
AUDIO INPUT IMPEDANCE	20 k Ohms, balanced, bridged. Other input impedance terminations available by resistor installation.	
AUDIO OUTPUT LEVEL	+8 dBm nominal into 600 Ohms. +18 dBm maximum.	
AUDIO OUTPUT IMPEDANCE	600 Ohms, transformer balanced.	
AUDIO SELECTION CAPACITY	79 individual selections.	
INTERNAL BATTERY BACK-UP	Six D-size alkaline cells. Maintains memory circuit operation for approximately 10 minutes.	

TABLE 1-1. DV-2A ELECTRICAL, PHYSICAL, AND ENVIRONMENTAL SPECIFICATIONS (Sheet 2 of 2)

(Silect 2 of 2)			
PARAMETER	SPECIFICATIONS		
SECONDARY BATTERY BACK-UP	+12V dc @ 3 Amperes continuous operation.		
AC POWER REQUIREMENTS	97V to 133V ac, 60 Hz. or 194V to 266V ac, 50 Hz.		
PHYSICAL			
DIMENSIONS Width	19 inches (48.3 cm).		
Height	3.5 inches (8.9 cm).		
Depth	18.75 inches (47.6 cm).		
WEIGHT	16.3 pounds (7.4 kg).		
<u>ENVIRONMENTAL</u>			
AMBIENT TEMPERATURE RANGE	+32°F to +132°F (ذC to +55°C).		
MAXIMUM HUMIDITY	95%, Non-condensing.		
COOLING	Natural convection and conduction.		
·			
	,		

SECTION II INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains the information required for the installation and preliminary checkout of the Broadcast Electronics DV-2A digital audio recorder.

2-3. UNPACKING.

- 2-4. The equipment becomes the property of the customer when the equipment is delivered to the carrier. Carefully unpack the DV-2A digital audio recorder. Perform a visual inspection to determine that no apparent damage has been incurred during shipment. All shipping materials should be retained until it is determined that the unit has not been damaged. Claims for damaged equipment must be promptly filed with the carrier or the carrier may not accept the claim.
- 2-5. The contents of the shipment should be as indicated on the packing list. If the contents are incomplete, or if the unit is damaged electrically or mechanically, notify both the carrier and Broadcast Electronics, Inc.

2-6. INSTALLATION REQUIREMENTS.

2-7. Refer to the environmental specifications in Table 1-1 and ensure a proper operational environment exists prior to DV-2A installation.

2-8. INSTALLATION.

- 2-9. Each DV-2A digital recorder is assembled, operated, tested, and inspected at the factory prior to shipment and is ready for installation when received. Prior to installation, this publication should be studied to obtain a thorough understanding of the operation, circuitry, nomenclature, and installation requirements. Installation is accomplished as follows: 1) Preliminary Installation, 2) Placement, 3) Wiring, and 4) Installation Adjustments.
- 2-10. PRELIMINARY INSTALLATION.

WARNING

ENSURE NO PRIMARY OR EMERGENCY SYSTEM POWER IS CONNECTED TO THE DV-2A BEFORE PROCEEDING.

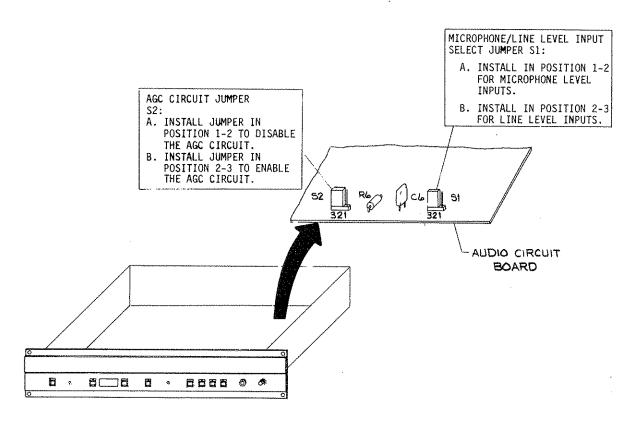
2-11. Refer to the following information and perform the preliminary installation procedures. The procedures will require the unit be placed on a work surface with the top-panel removed. After completion of the procedures, replace the unit top-panel.

2-12. DV-2A CIRCUIT BOARD PROGRAMMING. The DV-2A is equipped with programmable audio preamplifier and automatic-gain-control (AGC) circuitry for microphone or line level input applications (refer to Figure 2-1). It is recommended the AGC circuit be enabled for microphone level input applications only. Refer to Figure 2-1 and program the audio circuitry as required.

WARNING

ENSURE NO PRIMARY OR EMERGENCY SYSTEM POWER IS CONNECTED TO THE DV-2A BEFORE PROCEEDING.

- 2-13. INPUT VOLTAGE CHECK. The DV-2A is programmed for the proper power supply voltage when shipped from the factory. Ensure the power supply voltage programming is correct as follows.
- 2-14. Ensure the power supply voltage to be used (100V, 115V/120V, 220V, or 230/240V) is visible from the ac line voltage selector device on the DV-2A rear-panel. If the ac line voltage must be changed, proceed as follows:
 - A. Remove the ac voltage selector circuit board with a small pair of needle-nose pliers. Re-insert the circuit board so that the correct ac line voltage is visible from the ac voltage selector device window.



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FIGURE 2-1. DV-2A CIRCUIT BOARD JUMPER PROGRAMMING

2-15. Remove the fuse from the ac voltage selector device. Ensure the fuse and the spare fuse are slow-blow types rated at 1.5A for 100V to 120V operation or 0.75A for 220V to 240V operation.

2-16. PLACEMENT.

2-17. The DV-2A digital audio recorder requires 3.5 inches (8.9 cm) of a 19 inch (48.3 cm) cabinet and may be mounted in any convenient location within reach of signal and power cables. An additional 1.75 inches (4.4 cm) of cabinet space above and below the unit is required to provide adequate cooling. The unit should not be mounted directly above or below heat-generating equipment, otherwise no special requirements need be observed.

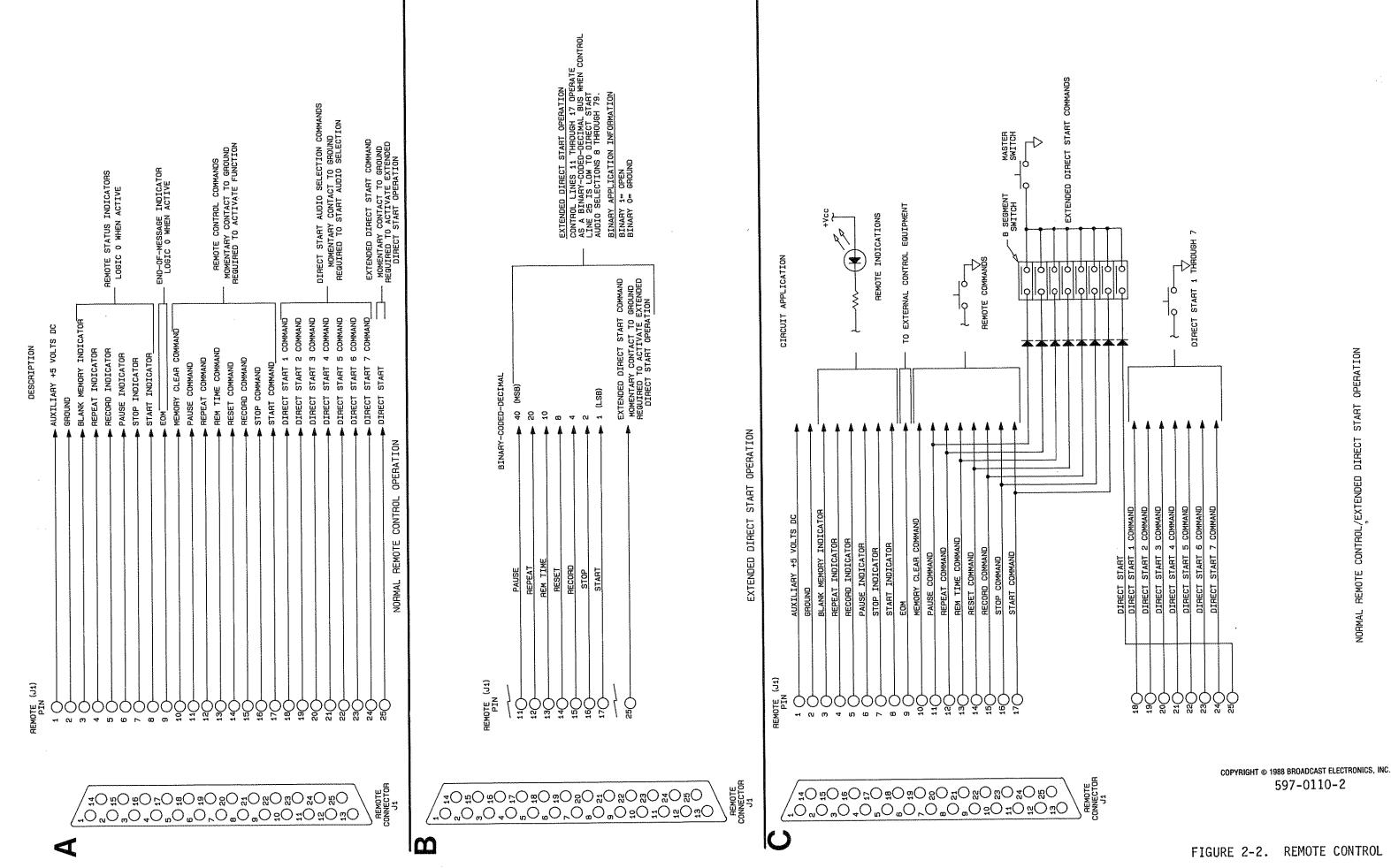
2-18. WIRING.

2-19. AUDIO INPUT/OUTPUT CONNECTIONS. Balanced input and output audio connections are provided by the IN (J2) and OUT (J3) receptacles on the DV-2A rear-panel. Construct audio input and output interface cables using 2-conductor shielded audio cable such as Belden 8451 and the audio IN and OUT mating connectors (located in the DV-2A accessory kit). The mating connector terminal descriptions are as follows:

XLR CONNECTOR TERMINAL	DESCRIPTION
1	Ground
2	+
3	***

- 2-20. REMOTE CONNECTIONS. All DV-2A operating parameters may be remotely controlled. Remote control interfacing is provided by the 25-Pin REMOTE CONTROL (J1) receptacle on the DV-2A rear-panel. Due to the design of the remote control system, the system will perform two types of remote control operations: 1) Standard remote control operation and 2) Extended direct start operation.
- 2-21. Standard Remote Control Operation. Standard remote control connections are illustrated in Figure 2-2A. Control of operating functions such as memory clear, pause, repeat, remaining time, reset, record, stop, start, and direct starting of audio selections 1 through 7 is accomplished using momentary contact-to-ground logic. The direct starting of an audio selection allows the operator to start a particular audio selection with a single switch. Remote status indications such as blank memory, repeat, record, pause, stop, and start are: 1) designed with open-collector drivers, 2) employ negative logic when active, and 3) do not contain current limiting resistors. Refer to Figure 2-2A and construct a remote interface cable as required using the REMOTE mating connector (located in the DV-2A accessory kit).

- 2-22. Extended Direct Start Operation. Direct starting of audio selections 8 though 79 is accomplished by a second remote control operation. REMOTE connector control lines 11 through 17 direct start audio selections 8 through 79 by operating as a binary-coded-decimal (BCD) data bus whenever the direct start control line (pin 25) is LOW (refer to Figure 2-2B). Simultaneous encoding of the BCD audio selection number and direct start control line is required to initiate extended direct start operation. The design allows the individual starting of any audio selection by manual or microprocessor controlled equipment. Refer to Figure 2-2B and construct a remote interface cable and control network for extended direct start operation as required. A REMOTE mating connector is provided in the DV-2A accessory kit.
- 2-23. Standard Remote Control/Extended Direct Start Operation. The remote control system may be operated to allow both standard remote control and extended direct start operation (refer to Figure 2-2C). If standard remote control and extended direction start operation is required, refer to Figure 2-2C and construct a remote interface cable and control circuit using the REMOTE mating connector (located in the DV-2A accessory kit).
- 2-24. <u>EOM Output</u>. The remote system also provides an end-of-message (EOM) output (pin 9). The EOM output employs negative logic to indicate the end of an audio selection and activate external automation or microprocessor control systems. Refer to Figure 2-2 and connect the EOM output to external control equipment as required.
- 2-25. AUTOMATIC SEQUENCING. The DV-2A digital audio recorder may be configured for automatic sequencing operations to continuously reproduce recorded program material. If automatic sequencing operations are desired, refer to Figure 2-2 and connect the EOM output (pin 9) to the remote start input (pin 17).
- 2-26. EMERGENCY POWER SYSTEMS. The DV-2A is designed with two types of emergency power systems: 1) an internal battery back-up system and 2) connections for an external emergency power supply system. The following text provides application and installation information for each system.
- 2-27. <u>Internal Battery Back-Up.</u> The internal battery back-up system maintains the DV-2A memory in the event of a momentary power failure. The system will maintain the memory for approximately 10 minutes.
- 2-28. The internal battery back-up system requires six D-size batteries. Refer to Figure 2-3 and install the batteries as shown.
- 2-29. External Emergency Power Supply Connections. Connections are provided on terminal strip TB1 for an external emergency power supply system which maintains DV-2A memory operation in the event of an extended power failure. The emergency power supply may be any +12V dc source rated at 3 amperes continuous operation (i.e. automotive battery). If desired, connect the emergency power supply system to TB1. The TB1 terminal descriptions are as follows:



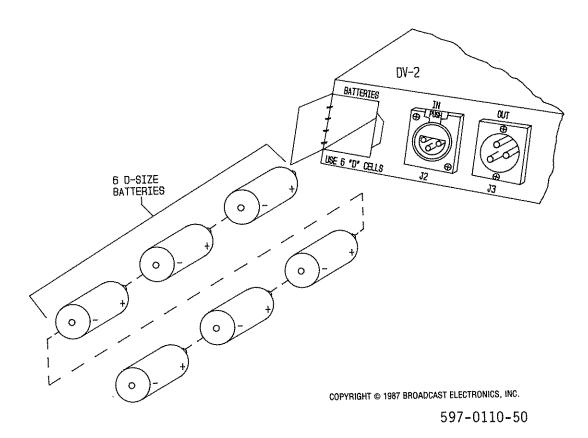


FIGURE 2-3. EMERGENCY POWER SYSTEM, BATTERY INSTALLATION

TERMINAL STRIP TB1	DESCRIPTION
1	+
2	Ground

2-30. INSTALLATION ADJUSTMENTS.

- 2-31. OUTPUT LEVEL ADJUSTMENT. The DV-2A is equipped with a continuously variable output level (+18 dBm maximum). The unit is shipped from the factory with a +8 dBm output level. To adjust the output level as required by the equipment application, proceed as follows:
 - A. Connect a VU meter to the DV-2A audio OUT (J3) receptacle.
 - B. Refer to SECTION III, OPERATION and operate the DV-2A to record a sample of program material.
 - C. Refer to SECTION III, OPERATION and operate the DV-2A to reproduce the test audio.
 - D. Refer to Figure 3-1 and adjust the OUTPUT VOLUME control for the desired level as indicated on the VU meter.
 - E. Remove the external VU meter.

SECTION III OPERATION

3-1. <u>INTRODUCTION</u>.

3-2. This section identifies all controls and indicators associated with the DV-2A digital audio recorder and provides standard operating procedures.

3-3. CONTROLS AND INDICATORS.

3-4. Refer to Figure 3-1 for the location of all controls and indicators associated with the DV-2A digital audio recorder. The function of each control or indicator is described by Table 3-1.

TABLE 3-1. CONTROLS AND INDICATORS (Sheet 1 of 3)

(6.1.66 1 6.1 6.7				
INDEX NO.	NOMENCLATURE	FUNCTION		
1	RECORD Switch/ Indicator	SWITCH: Operates the DV-2A into the record mode.		
		INDICATOR: Illuminates to indicate the DV-2A is operating in the record mode.		
2	AUDIO INPUT Indicator (Red/Green Illumination)	RED Illuminates red to INDICATION: indicate an excessive audio input condition.		
	T T Tulli Tita C Toll)	GREEN Illuminates green to INDICATION: indicate a normal audio input condition.		
3	AGC Circuit	Position 1-2: Disables the AGC circuit.		
	Jumper	Position 2-3: Enables the AGC circuit.		
4	Microphone/Line Level Input Select Jumper	Position 1-2: Programs the audio amplifier circuit for microphone level input audio.		
		Position 2-3: Programs the audio amplifier circuit for line level input audio.		

TABLE 3-1. CONTROLS AND INDICATORS (Sheet 2 of 3)

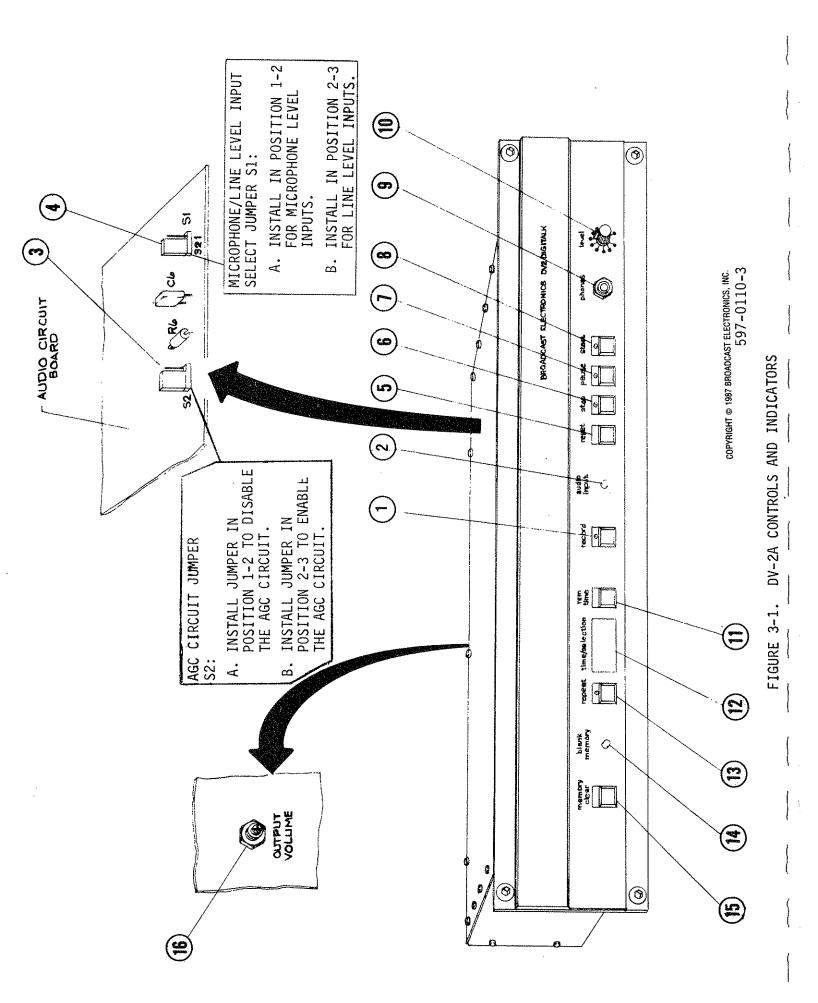
INDEX NO.	NOMENCLATURE	FUNCTION		
5	RESET Switch	Terminates playback operation and instructs the DV-2A microprocessor to access the begin-ning of the current audio selection.		
6	STOP Switch/ Indicator	SWITCH: A. Terminates playback or record operation. Instructs the DV-2A microprocessor to access the end of the current audio selection and display the next sequential audio selection number.		
		B. Allows the operator to sequentially access the end of each audio selection.		
		INDICATOR: Illuminates to indicate playback or record termination.		
7	PAUSE Switch/ Indicator	SWITCH: Suspends playback or record opera- tion.		
		INDICATOR: Illuminates to indicate the sus- pension of playback or record operation.		
8	START Switch/ Indicator	SWITCH: A. Initiates record or playback opera- tion.		
		B. Allows the operator to sequentially access the beginning of each audio selection.		
		INDICATOR: Illuminates to indicate playback or record operation.		
9	PHONES Receptacle	Headphone receptacle.		
10	LEVEL Control	Adjusts the headphone volume.		
11	REM TIME Switch	Indicates the remaining time available for recording as indicated on the TIME/SELECTION display. Operational only when the unit is in the stop mode.		

TABLE 3-1. CONTROLS AND INDICATORS (Sheet 3 of 3)

INDEX NO.	NOMENCLATURE	FUNCTION	
12	TIME/SELECTION Display	Indicates the remaining time available for recording or the current audio selection number.	
13	REPEAT Switch/ Indicator	SWITCH: A. Initiates an operation which pro- grams the circuitry to repeat the current audio selection.	
		B. Configures the unit for continuous playback operation.	
		INDICATOR: Illuminates to indicate the unit is configured for repeat or con- tinuous playback operation.	
14	BLANK MEMORY Indicator	Illuminates to indicate blank memory is available for recording.	
15	MEMORY CLEAR Switch	Erases ALL DV-2A memory when simultaneously operated with the RECORD switch/indicator.	
16	OUTPUT VOLUME Control	Adjusts the DV-2A output volume.	

NOTE	THE FOLLOWING	PROCEDURE ASSUN	MES THAT THE
alabera dia manana	DV-2A DIGITAL	AUDIO RECORDER	IS COMPLETELY
NOTE	INSTALLED AND	IS FREE OF ANY	DISCREPANCIES.

- 3-5. OPERATION.
- 3-6. PRELIMINARY OPERATION.
- 3-7. Ensure the emergency power supply systems are operational and apply power to the DV-2A by connecting the ac power cord to the appropriate power source. Initialize the DV-2A memory by simultaneously depressing the MEMORY CLEAR and RECORD switch/indicators.
- 3-8. RECORD/PLAYBACK FUNCTIONS.
- 3-9. RESET. The reset function allows the operator to conveniently terminate playback operation and access the beginning of the current audio selection. To initiate a reset command, depress the REPEAT switch during playback operation.



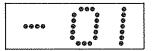
3-4

- 3-10. PAUSE. The pause function temporarily suspends playback or record operation. To initiate a pause operation, depress the PAUSE switch/indicator to illuminate the switch/indicator during playback or record operation.
- 3-11. REMAINING TIME. The remaining time function allows the operator to access the remaining memory time available for recording. To access the remaining memory time, depress the REM TIME switch when the unit is in the stop mode.
- 3-12. RECORD OPERATION.
- 3-13. PROGRAM MATERIAL. The DV-2A will record and reproduce any type of program material including single-tone audio. Due to the nature of the DV-2A data compression system, the PAUSE function is not compatible with single-tone audio reproduction. Do not operate the unit in the PAUSE mode when reproducing single-tone audio.
- 3-14. PRELIMINARY RECORD OPERATION. Select the program material to be recorded. Ensure the audio input level is within the DV-2A specifications (refer to the DV-2A Specifications in SECTION I, GENERAL INFORMATION).
- 3-15. Remove the DV-2A top-panel.
- 3-16. Refer to Figure 3-1 and install microphone/line level select jumper S1 and AGC circuit jumper S2 in the appropriate positions.
- 3-17. Replace the DV-2A top-panel.
- 3-18. Operate the STOP switch/indicator to illuminate the switch/indicator.
- 3-19. Calibrate the audio input level as follows:
 - A. Start the playback system to apply program audio to the DV-2A.
 - B. Adjust the playback system output level until the AUDIO INPUT indicator illuminates green.
- 3-20. RECORDING PROGRAM MATERIAL. Ensure the preceding preliminary procedures are correctly performed and begin recording program material as follows.
- 3-21. Depress the STOP switch/indicator until the BLANK MEMORY indicator illuminates.
- 3-22. Operate the DV-2A to the record mode by performing one of the following operations:
 - A. Depress and hold the RECORD switch/indicator, then depress the START switch/indicator to illuminate the switch/indicator.

- B. Operate the RECORD switch/indicator to illuminate the switch/indicator. Operate the START switch/indicator to illuminate the switch/indicator.
- 3-23. Start the playback system and begin recording program material.
- 3-24. At the end of the program material, depress the STOP switch/indicator to illuminate the switch/indicator. The DV-2A will terminate the record operation and output an End-of-Message (EOM) signal (momentary contact closure to ground).
- 3-25. Repeat the procedure as required for the desired program format.
- 3-26. SPECIAL RECORD FUNCTIONS. The following special function may be initiated as required.
 - A. REM TIME (Operational only when the unit is in the stop mode.)
 - B. PAUSE
- 3-27. PLAYBACK OPERATION.
- 3-28. Access the desired selection by depressing the STOP switch/indicator until the selection number is indicated on the TIME/SELECTION display.
- 3-29. After the selection is located, depress the START switch/indicator to illuminate the switch/indicator. The DV-2A will respond by initiating playback operation.
- 3-30. SPECIAL PLAYBACK FUNCTIONS. The following special functions may be initiated during playback operation if desired.
 - A. PAUSE
 - B. RESET
- 3-31. REPEAT OPERATION.
- 3-32. The repeat function allows the operator to conveniently repeat the current audio selection. A repeat function is initiated as follows.
- 3-33. Access the desired selection for repeat operation by depressing the STOP switch/indicator until the selection number is indicated on the TIME/SELECTION display.
- 3-34. After the selection is located, depress the REPEAT switch/indicator to illuminate the switch/indicator.

- 3-35. Depress the START switch/indicator. The DV-2A will respond by reproducing the audio selection. Once playback operation is complete, the unit will remain at the current audio selection for repeat operation. Depress the START switch/indicator to repeat the selection.
- 3-36. CONTINUOUS PLAYBACK OPERATION.
- 3-37. Access the desired selection for continuous playback operation by depressing the STOP switch/indicator until the selection number is indicated on the TIME/SELECTION display.
- 3-38. After the selection is located, depress the REPEAT switch/indicator twice. The REPEAT switch/indicator will illuminate and a -symbol will illuminate in the first digit of the TIME/SELECTION display to indicate the DV-2A is configured for continuous playback operation.

EXAMPLE:



- 3-39. Depress the START switch/indicator to illuminate the switch/indicator. The DV-2A will respond by continuously playing the selection.
- 3-40. To momentarily interrupt continuous playback operation, depress the PAUSE switch/indicator to illuminate the switch/indicator. To terminate continuous playback operation, depress the STOP switch/indicator to illuminate the switch/indicator and depress the REPEAT switch/indicator to extinguish the switch/indicator. The TIME/SELECTION display symbol will entinguish.
- 3-41. MEMORY CLEAR.
- 3-42. To clear ALL DV-2A memory, simultaneously depress the MEMORY CLEAR and RECORD switch/indicators. The DV-2A microprocessor will respond by re-initializing the digital memory.
- 3-43. AUDIO MONITORING.
- 3-44. The DV-2A headphone system accepts all types of stereophonic headphones. The system will not accept monophonic headphones unless the monophonic headphones are equipped with a stereophonic jack.

CAUTION

DO NOT CONNECT MONOPHONIC HEADPHONES TO THE DV-2A HEADPHONE SYSTEM WITHOUT MODIFICATION.

- 3-45. To monitor record or playback program audio, insert the head-phone jack into the PHONES receptacle.
- 3-46. Operate the PHONES level control to adjust the headphone level as required.

SECTION IV THEORY OF OPERATION

4-1. INTRODUCTION.

4-2. This section presents the theory of operation for the Broadcast Electronics DV-2A digital audio recorder. A simplified schematic of the DV-2A is presented in Figure 4-1. Refer to the schematic as required for the following functional equipment description.

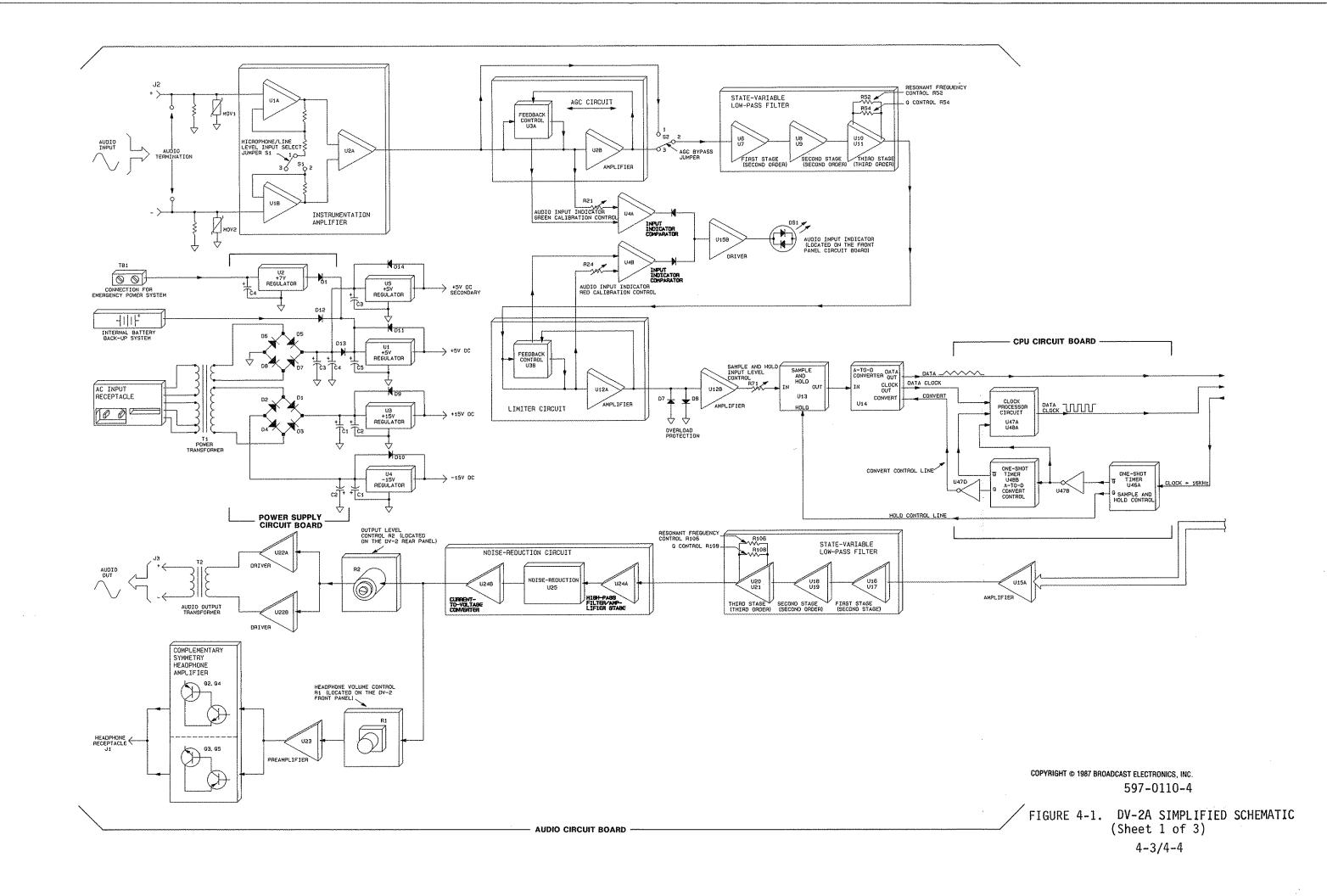
4-3. FUNCTIONAL DESCRIPTION.

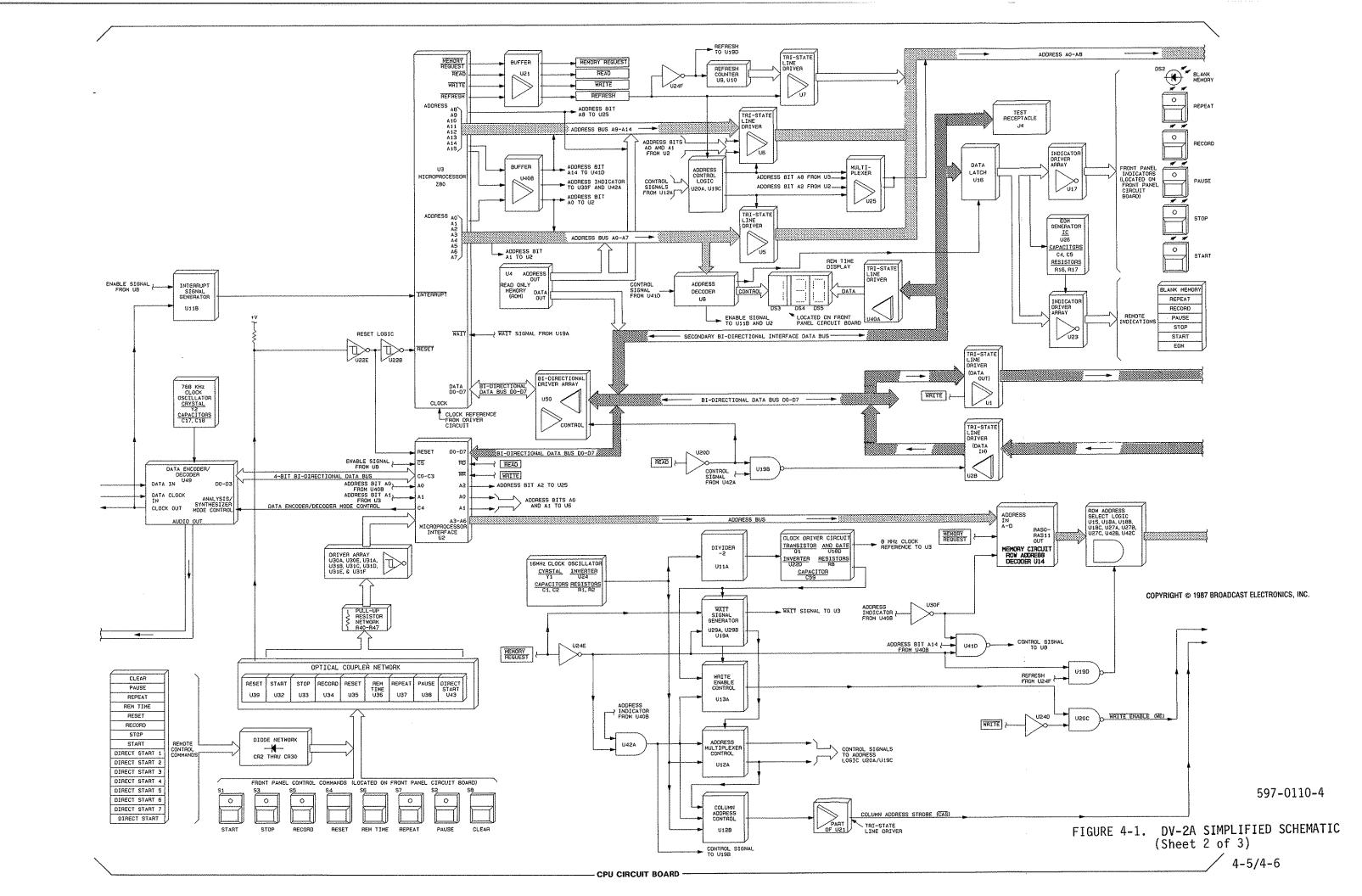
- 4-4. RECORD CIRCUIT.
- 4-5. Record audio is applied to the DV-2A circuitry through audio input receptacle J2. A balanced 20 k Ohm audio impedance is established by a bridged input network. Special audio input impedance requirements may be accommodated by the installation of a termination resistor in the network. Overload protection for the input circuitry is provided by metal-oxide-varistors MOV1 and MOV2.
- 4-6. Audio from the input impedance circuit is routed to integrated circuits U1A/U1B and U2A which are configured as a positive/ negative gain instrumentation amplifier. Control of the amplifier is provided by microphone/line level input select jumper S1. The amplifier will provide a gain of 34 dB when configured for microphone inputs and a gain of -6 dB for line level inputs.
- 4-7. Audio from the instrumentation amplifier is routed to an automatic-gain-control (AGC) circuit and a bypass network. The AGC circuit consists of feedback control stage U3A and amplifier U2B. The circuit will evaluate the applied input signal and generate the appropriate level of gain to maintain a constant record audio level. The AGC circuit output is routed to bypass jumper S2 which selects either AGC controlled audio or audio from the instrumentation amplifier.
- 4-8. Audio from AGC bypass jumper S2 is applied to operational amplifiers U6 through U11 which are configured as a seventh order state-variable low-pass filter. The filter provides sharp attenuation of frequencies above 6635 Hz. Alignment of the filter is provided by Q control R54 and resonant frequency control R52.
- 4-9. The output of the filter is routed to a limiter circuit consisting of feedback control stage U3B and amplifier U12A. The limiter is provided to protect the subsequent sampling circuitry from overvoltage conditions. The output of the limiter circuit is applied to amplifier U12B which provides a gain of approximately 21 dB. The amplifier output is applied through sample and hold circuit input level control R71 to the audio sampling circuitry. Diodes D7 and D8 are provided as a secondary over-voltage protection circuit.

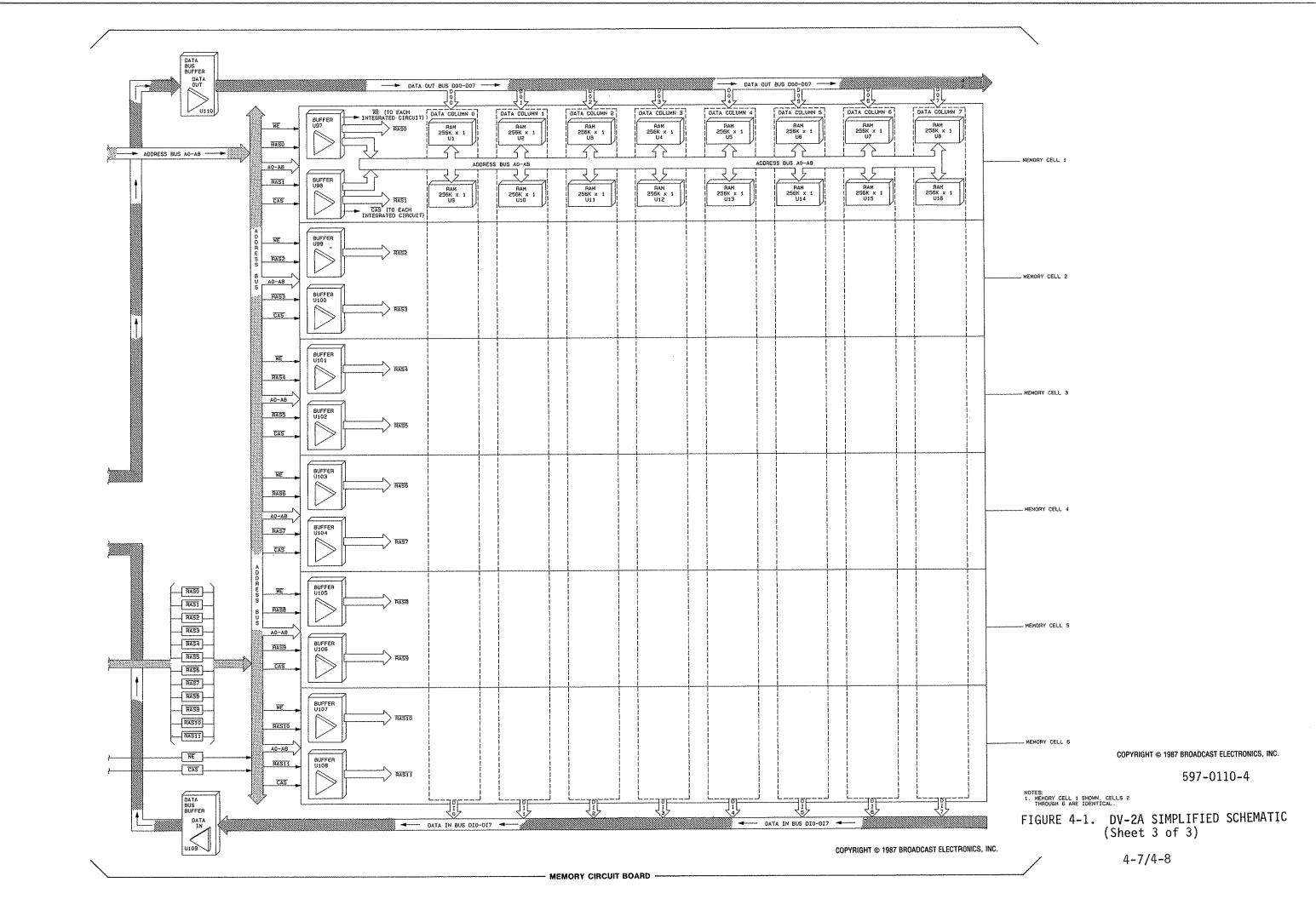
- 4-10. AUDIO INPUT INDICATOR CIRCUIT. Voltage samples from the AGC and limiter circuits are applied to an audio input indicator circuit consisting of comparators U4A/U4B, driver U15B, and bi-color audio input indicator DS1. Samples from the AGC circuit are applied to input indicator comparator U4A. When the voltage from the AGC feedback network increases above the reference established by input indicator calibration control R21, U4A will output a negative voltage to driver stage U15B. U15B will output approximately -10V dc to bias input indicator DS1 into green illumination to indicate a normal audio input level condition.
- 4-11. Samples from the limiter circuit are applied to input indicator comparator U4B. When the voltage from the limiter feedback network increases above the reference, U4B will output a positive voltage to U15B. U15B will output approximately +20V dc to bias input indicator DS1 into red illumination to indicate an excessive audio input level condition.

4-12. AUDIO SAMPLING CIRCUIT.

- 4-13. The audio sampling circuitry consists of a sample-and-hold device, an analog-to-digital converter, a data encoder/decoder, and a timing circuit. Together, the circuitry operates to sample and convert the analog audio information to a digital format for application to a microprocessor circuit.
- 4-14. Audio sampling operations are controlled by data encoder/decoder U49 and a timing circuit consisting of sample-and-hold control logic U46A, A-to-D convert control logic U48B, and clock processor U47A/U48A. Data encoder/decoder U49 is a multi-function device which processes digital audio information to and from the microprocessor. A 16 kHz clock output from U49 is used as a timing reference for sampling operations. The clock signal is applied to one-shot sample-and-hold control timer U46A. The Q output of U46A is used to control the operation of sample-and-hold device U13. The $\overline{\rm Q}$ output of U46A is inverted by U47B and applied to clock processor U48A/U47B and A-to-D convert control timer U48B. The Q output of U48B is designed to control the operation of A-to-D converter U14.
- 4-15. An audio sampling cycle is initiated by the application of a clock pulse to sample-and-hold timer U46A. U46A will generate a LOW-going pulse which instructs sample-and-hold device U13 to route audio samples to A-to-D converter U14. A-to-D convert timing control logic U48B and inverter U47D will route a HIGH control pulse to U14 which enables analog-to-digital data conversion. U14 will output: 1) serial data information to data encoder/decoder U49 and 2) a data timing reference to clock processor circuit U48A/U47A. The clock processor circuit generates and routes a timing reference to data encoder/decoder U49 for input data control applications. U49 will compress and convert the serial data information to a 4-bit parallel format for application to the microprocessor circuit.







4-16. MICROPROCESSOR AND INTERFACE CIRCUITRY.

- 4-17. GENERAL. All data processing operations are controlled by the DV-2A microprocessor circuitry. The circuitry contains a Z-80 microprocessor which is responsible for the storage and acquisition of digital information in the DV-2A memory. A microprocessor interface circuit is incorporated into the design to expand the control and operating characteristics of the microprocessor. Synchronization of microprocessor operations is provided by a timing network. Control information for the microprocessor is implemented through a single ROM integrated circuit.
- 4-18. READ-ONLY-MEMORY (ROM). The microprocessor circuit ROM consists of integrated circuit U4. U4 is a 8192 byte EPROM which provides a non-volatile location for the DV-2A microprocessor instruction code. The code is responsible for the direction of all microprocessor control and processing functions.
- 4-19. MICROPROCESSOR. Integrated circuit U3 is a Z-80 microprocessor which controls all data processing operations to and from the memory circuit. Microprocessor U3 contains: 1) four output commands, 2) sixteen address lines, 3) eight bi-directional data lines, and 4) three internal control functions. The commands are used to synchronize data processing operations and are described as follows.

MICROPROCESSOR COMMAND	DESCRIPTION
READ (RD)	A LOW-active processor command to read information from the memory circuit, information from the interface circuitry, or ROM information.
WRITE (WR)	A LOW-active processor command to write information to the memory or interface circuits.
REFRESH (RFSH)	A LOW-active processor command to refresh the data information in the memory circuit.
MEMORY REQUEST (MRQ)	A LOW-active processor command to perform a memory circuit operation (read, write, or refresh).

4-20. MICROPROCESSOR INTERFACE CIRCUIT. Due to the DV-2A memory and audio sampling circuit designs, the microprocessor requires the operation of an interface circuit for communication purposes. Integrated circuit U2 is a programmable input/output device designed to expand the interfacing capabilities of the microprocessor. U2 is a multi-function device which: 1) processes data information to and from the microprocessor and 2) generates part of the memory addressing information.

- 4-21. MICROPROCESSOR CLOCK CIRCUIT. Timing for microprocessor internal operations is generated by a precision clock oscillator circuit. The clock circuit consists of crystal Y1, inverter U24, capacitors C1, C2, and resistors R1 and R2. The circuit generates a precision 16 MHz output which is routed to divide-by-two counter U11A and a timing circuit. The 8 MHz output of U11A is applied to a clock driver circuit consisting of transistor Q1, AND gate U18D, inverter U22D, resistor R8, and capacitor C59. The output from the driver circuit is applied to the timer circuit and microprocessor U3.
- 4-22. TIMING CIRCUIT. Synchronization signals for microprocessor read and write operations are generated by a timing circuit. The timing circuit consists of five D-type flip-flop stages and the associated control input logic.
- 4-23. When the microprocessor is instructed to perform a memory circuit operation, the MEMORY REQUEST control line will go LOW. The MEMORY REQUEST command is applied to the timing circuit and processed through inverter U24E and AND gate U42A to control a variety of synchronization operations. U42A ANDs the MEMORY REQUEST signal and a microprocessor address identification signal which is buffered by U40B to initiate timing operations for special types of memory addresses.
- 4-24. Wait Signal Generator Circuit. MEMORY REQUEST signals in an inverted and non-inverted format are applied to a WAIT signal generator circuit. A WAIT signal is a synchronization command which temporarily suspends microprocessor addressing operations. This circuit allows the microprocessor to operate at a faster rate than the external input/out-put logic and memory circuits.
- 4-25. The WAIT signal generator consists of D-type flip-flops U29A, U29B, and NAND gate U19A. A timing reference for circuit operations is provided by an 8 MHz signal from the microprocessor clock <u>driver circuit</u>. The circuit will generate one wait period for each <u>MEMORY REQUEST</u> and timing command.
- 4-26. Memory Write Control Logic. D-type flip-flop U13A is configured as the memory write control logic. The control logic is preset for operation by address identification information from U42A. WAIT commands from the WAIT signal generator circuit provide control information. Timing for memory write control logic circuit operation is provided by an 8 MHz reference from the microprocessor driver circuit. The memory write control logic will output a HIGH-going control signal to the write enable logic at the application of WAIT and timing commands.
- 4-27. Address Multiplexer Control Logic. D-type flip flop U12A is configured as the address multiplexer control logic. The control logic is preset for operation by address identification information from U42A. WAIT commands from the WAIT signal generator circuit provide control information. Timing for address multiplexer control logic operation is provided by a 16 MHz reference from the microprocessor clock oscillator circuit. The address multiplexer control logic will output complementary control pulses to subsequent address multiplexing control circuitry at the application of $\overline{\text{WAIT}}$ and timing commands.

- 4-28. <u>Column Address Control Logic.</u> The column address control logic consists of D-type flip-flop U12B. The logic circuit is preset for operation by address identification information from U42A. Multiplex commands from address logic U12A provide control information. Timing for circuit operations is provided by a 16 MHz reference from the microprocessor clock oscillator. The column address logic will output a LOW-going control pulse to the column address circuitry at the application of address multiplexer and timing commands.
- 4-29. ADDRESS CIRCUITRY. Address communication between the microprocessor and the data circuitry is provided by a buss network. Address operations are performed by microprocessor U3 and microprocessor interface device U2. Together, U3 and U2 generate a 22-bit address for accessing or routing information to/from individual circuits such as the memory circuit, the audio sampling circuit, and the front-panel time/selection display.
- 4-30. Memory Circuit Addressing. When memory circuit read/write operations are required, microprocessor U3 and microprocessor interface U2 will select a memory location by generating a 22-bit address. U3 generates 15 bits of the address with address lines A0 through A14. The remaining 7 address bits are generated by lines A0 through A6 of U2. Three address bits from U2 and the 15 address bits from U3 are multiplexed into a 9-bit format by a circuit consisting of: 1) tri-state line drivers U5 and U6, 2) multiplexer U25, and 3) address control logic U19C and U20A. Control of the multiplexing operations is provided by address multiplexer control logic U12A. The following text provides the address format and circuit routing information.

U3 ADDRESS LINE	ADDRESS INFORMATION	ADDRESS LINE CIRCUIT ROUTING
AO Through A7	Memory Component Row	Driver U5
A8	Memory Component Row	Multiplexer U25
A9 Through A14	Memory Component Column	Driver U6
U2 ADDRESS LINE	ADDRESS INFORMATION	ADDRESS LINE CIRCUIT ROUTING
AO, A1	Memory Component Column	Driver U6
A2	Memory Component Column	Multiplexer U25
A3 Through A6	Memory Circuit Row	Decoder U14

4-31. When the microprocessor is required to perform a memory read/write operation, a memory circuit addressing cycle will be initiated. Memory circuit row address select information from U2 will be routed to memory circuit row address decoder U14. When the MEMORY REQUEST and the address identification signal from inverter U30F go L0W, U14 will decode the applied address and select one memory row via the memory circuit row address select logic. Timing pulses from address multiplexer control U12A will operate address control logic U20A and U19C to the row address configuration. The address control logic will enable line driver U5 and configure multiplexer U25 for row address operation. U5 and U25 will operate together to route 9 bits of memory component row address information to the memory circuit.

- 4-32. After the application of all row address information, control commands from logic U12A will configure address multiplexing logic U20A and U19C for column address operation. The logic will: 1) disable line driver U5, 2) enable line driver U6, and 3) configure multiplexer U25 for column address operation. U6 and U25 will operate together to route 9 bits of memory component column address information to the memory circuit. A LOW column address command from U12B will also be routed to the memory circuit for column address control.
- 4-33. <u>Time/Selection Display Addressing</u>. The microprocessor communicates with the front-panel time/selection display through an address buss and decoder network. Address information from the microprocessor is routed through a 3-bit address bus to decoder U8. U8 will decode the address and generate three control commands for application to time/selection displays DS3 through DS5.
- 4-34. DATA SAMPLING AND MEMORY WRITE OPERATION. Data sampling and memory write operations are controlled by the microprocessor and the timing circuitry. The microprocessor requires a series of read and write cycles to access and route data to the memory circuit.
- 4-35. When a memory circuit write operation is required, the microprocessor will initiate the operation by generating a read cycle. U3 will address the data encoder/decoder communication port of U2 (port C) via lines AØ and A1. The microprocessor READ line will go LOW to initiate read operation of U2 and configure bi-directional data driver U50 via inverter U20D to receive data. U2 will output a LOW through the mode control line to operate data encoder/decoder U49 to the synthesizer mode. U49 will convert and compress the serial data from A-to-D converter U14 into a 4-bit parallel data output for application to U2. From U2, the data is routed through the bi-directional data bus and driver array U50 to the microprocessor. The read cycle is repeated to generate an 8-bit data word for memory circuit write operations.
- 4-36. After the completion of the read cycles, the microprocessor will initiate a memory write cycle. The microprocessor will address a selected location in the memory circuit. The microprocessor $\overline{\text{WRITE}}$ line will go LOW to initiate a write logic timing sequence. The $\overline{\text{WRITE}}$ command is applied through inverter U24D to NAND gate U20C. U20C NANDs the inverted $\overline{\text{WRITE}}$ command and a write control signal to generate a LOW-going write enable ($\overline{\text{WE}}$) pulse for application to the memory circuit. With the microprocessor in a write cycle, inverter U20D will output a LOW to configure bi-directional driver array U50 for transmit data operations. This allows the data from the microprocessor to be routed through U50 and driver U1 to the memory circuit.
- 4-37. MEMORY READ AND DATA OUTPUT OPERATION. Memory read and data output operations are also controlled by cycles of microprocessor read and write commands. The commands operate together with the timing circuit to route data information from the memory circuit to the data encoder/decoder for D-to-A conversion.

- 4-38. When a memory read and data output operation is required, the microprocessor will begin the operation with a memory read cycle. The microprocessor will address the selected location in the memory circuit. The READ line will go LOW to configure data bus control logic U20D and U19B for a memory read operation. The logic generates: 1) a HIGH to data driver array U50 which configures the array for receive data operation and 2) a LOW enable command to line driver U28. With the application of the address and control signals, data from the memory location is routed through drivers U28 and U50 to the microprocessor.
- 4-39. After the completion of the read cycle, the microprocessor will initiate a write cycle. The microprocessor will address the data encoder/decoder port of U2 via lines AØ and A1. The $\overline{\text{WRITE}}$ command will go LOW to initiate write operation of U2 and configure driver array U50 for transmit data operations.
- 4-40. With the data bus configured for transmit data operation, the microprocessor will route a 4-bit data word and a control command to U2. U2 routes the data to data encoder/decoder U49. U2 also outputs a HIGH through the mode control line to configure U49 for analysis operation. U49 will convert the digital information to an analog format for application to the output network. The write cycle is repeated to complete the processing of the 8-bit data word from the memory circuit.
- 4-41. TIME/SELECTION DISPLAY WRITE OPERATION. When the micro-processor is required to display time or selection information, the time/selection display will be addressed via decoder U8. Time/selection information is routed in a 4-bit format from the microprocessor through buffer U40A to time/selection display components DS1 through DS3. The data is clocked into the display by control commands from decoder U8.
- 4-42. FRONT-PANEL/REMOTE INDICATOR WRITE OPERATION. When the microprocessor is required to display front-panel or remote indicator information, the remote/local indicators will be addressed via decoder U8. Control commands from microprocessor U3 will be routed through the secondary data bus to latch U16. U8 will output a LOW to enable latch U16 which routes the control commands through driver arrays U17 and U23 to illuminate the appropriate indicators.
- 4-43. END-OF-MESSAGE CIRCUITRY. Integrated circuit U26, capacitors C4, C5 and resistors R16 and R17 operate as an end-of-message circuit. The circuit monitors the start indicator commands from microprocessor U3. When the start indicator control lines goes LOW, the circuit will output a LOW to indicate the end-of-message.
- 4-44. REFRESH CIRCUIT. Due to the use of dynamic RAM in the DV-2A memory circuit, the data must be constantly addressed to prevent erasure.
- At the proper application of control signals, the refresh circuitry will produce an addressing sequence to retain the memory circuit information.

- 4-45. The refresh circuit consists of a counter, tri-state line driver logic, and timing commands. When a refresh cycle is required, the microprocessor REFRESH control line will go LOW. The REFRESH command is: 1) inverted by U24F and applied to integrated circuits U9 and U10, 2) applied to line driver U7, and 3) applied to address control logic U20A and U19C. U9 and U10 are configured as a binary counter. The REFRESH command instructs the counter to output a \emptyset to 255 binary counting sequence to line driver U7. The REFRESH command also enables driver U7 and instructs the address control logic to disable the multiplexing circuitry.
- 4-46. An inverted $\overline{\text{REFRESH}}$ command is routed to NAND gate U19D. U19D NANDs the inverted $\overline{\text{REFRESH}}$ command and a HIGH-going $\overline{\text{MEMORY}}$ REQUEST command from U24E to generate a LOW control signal to the row address select logic. The LOW will generate LOW control pulses from all row address select lines to enable all memory rows. With all memory rows enabled, the addressing information from driver U7 will be recognized by all memory circuit components.
- 4-47. INTERRUPT LOGIC. D-type flip-flop U11B operates as a microprocessor INTERRUPT signal generator. An INTERRUPT command instructs microprocessor U3 to suspend processing operations. U11B operates from a LOW control command from decoder U8 and a clock reference from data encoder/decoder U49. The circuit will generate an INTERRUPT command at the application of the control and timing commands.
- 4-48. RESET LOGIC. The reset logic consists of inverters U22E, U22B and a pull-up resistor. At the application of primary power or a reset command from optical coupler U39, the reset control line will go LOW. The LOW is applied to the inverter logic which outputs HIGH reset command to U2 and a LOW reset command to U3.
- 4-49. MODE CONTROL CIRCUIT. All DV-2A mode control commands are routed to a processing circuit for application to the microprocessor. The processing circuit consists of a diode network, an optical coupler network, a pull-up resistor network, and an inverter array.
- 4-50. Local Mode Control Commands. Front-panel mode commands are entered by switches S1 through S8 which utilize LOW-going pulses for control operations. Each control pulse is applied to an optical coupler network. The coupler network operates in conjunction with the pull-up resistor network and the driver array to generate an 8-bit binary coded command for application to the microprocessor.
- 4-51. Remote Mode Control Commands. The remote mode control system is designed for two types operations: standard remote control and extended direct start control. When the system is operated in the standard remote control configuration, all front-panel commands may be selected by a LOW control signal. In addition, audio selections 1 through 7 may be direct started with LOW-going control commands. Each command is routed through a diode network to produce a corresponding 8-bit code. The code is processed by the optical coupler network, pull-up resistor network, and the inverter array for application to the microprocessor.

- 4-52. When the system is operated in the extended direct start configuration, 7 remote control commands (pause, repeat, rem time, reset, record, stop, and start) operate with a LOW direct start command to form a binary coded command system. The system allows audio selections 8 though 99 to be direct started. The binary command is applied through the diode network to the optical coupler network. The coupler network operates with the resistor network and the inverter array to process the binary code for application to the microprocessor.
- 4-53. MEMORY CIRCUIT.
- 4-54. The DV-2A memory circuit contains approximately 3 megabytes of RAM to provide six minutes and twenty-nine seconds of record time. The RAM is generated by 96 dynamic RAM integrated circuits. Each integrated circuit contains 32K bytes of memory.
- 4-55. Communication between the memory circuit and the microprocessor circuit is provided by data and address busses. The data buss is divided into input and output sections. Integrated circuit U110 provides buffering for the data output buss. Integrated circuit U109 provides buffering for the data input buss.
- 4-56. The memory circuit is divided into 8 columns and twelve rows of memory components. The circuit is further divided into 6 identical memory cells. Each memory cell contains 16 memory components, two address drivers, and an address bus.
- 4-57. Memory cell 1 consists of address buffers U97 and U98 and RAM components U1 through U16. The RAM components are divided into data columns DØ through D7 and address rows RASØ and RAS1.
- 4-58. A memory location in cell 1 is addressed by the microprocessor when either the $\overline{\text{RAS0}}$ or $\overline{\text{RAS1}}$ control lines goes LOW. Memory component row address information is routed through buffers U97 and U98. U97 and U98 apply the information to the memory cell address buss for recognition by the enabled memory row. Next, memory component column address information is routed to the address bus and recognized by the appropriate data column when the $\overline{\text{CAS}}$ (column address select) line goes LOW. Once the memory location is addressed, data will be: 1) written into the location if the $\overline{\text{WE}}$ (write enable) line is LOW or 2) read from the location if the $\overline{\text{WE}}$ (write enable) line is HIGH.
- 4-59. PLAYBACK AUDIO CIRCUIT.
- 4-60. Analog audio information from data encoder/decoder U49 is applied to amplifier stage U15A which is configured for a gain of approximately 22 dB. The amplifier output is applied to operational amplifiers U16 through U21 which are configured as a seventh-order state variable low-pass filter. Playback filter operation is identical to the record filter which provides sharp attenuation of frequencies above 6635 Hz.

- 4-61. The output from the playback low-pass filter is routed to a noise-reduction circuit consisting of integrated circuits U24A/B and U25. The noise reduction circuit incorporates dynamic variable bandwidth limiting and a downward expansion technique to effectively reduce the noise level. The operational noise reduction circuitry is housed on integrated circuit U25. Operational amplifier U24A is configured as a high-pass filter/amplifier stage which controls the circuit sensitivity. Operational amplifier U24B operates as an output current-to-voltage converter. The output from U24B is routed to the output driver head-phone circuitry.
- 4-62. OUTPUT DRIVER CIRCUIT. Audio from the noise-reduction circuit is routed to potentiometer R2 which provides output volume level control. From R2, audio is applied to an output driver circuit consisting of amplifiers U22A/B. U22A/B operate as a balanced output driver network with a gain of 2. The audio output from the circuit is transformer balanced by T2 for application to output receptacle J3.
- 4-63. HEADPHONE CIRCUIT. Audio from the noise-reduction circuit is also applied to the headphone circuit. The headphone circuit consists of a level control, preamplifier stage, and a complementary symmetry output driver stage.
- 4-64. Audio is routed to potentiometer R1 which provides headphone level control. The output from R2 is applied to operational amplifier U23 which is configured as a preamplifier stage. The output from U23 is applied to a complementary symmetry amplifier stage consisting of transistors Q2 through Q5. The stage provides the required gain for application of the audio signal to headphone receptacle J1.
- 4-65. POWER SUPPLY CIRCUIT.
- 4-66. The DV-2A power supply circuitry consists of a power transformer and dual rectifier network which generates a variety of dc operating potentials. An internal battery back-up system and connections for a secondary back-up system are incorporated into the power supply circuit design for emergency power operation.
- 4-67. A 19.5V ac potential from the secondary of power transformer T1 is full-wave rectified by diodes D1 through D4 and filtered by capacitors C1 and C2 into $\pm 18V$ supplies. The $\pm 18V$ supplies are applied to regulators U3 and U4 to produce $\pm 15V$ dc operating potentials.
- 4-68. A 9.5V ac potential is full-wave rectified by diodes D5 through D8 and filtered by capacitors C3 and C4 into a +8V dc supply. The +8V supply is applied to regulator U1 and U5 to produce two +5V dc operating potentials.
- 4-69. EMERGENCY POWER SYSTEMS. The internal battery back-up system is connected to regulator U1. The system provides an emergency +9 volt supply to regulator U1 during power failures. The supply will maintain the regulator operation for approximately 10 minutes.
- 4-70. Terminal strip TB-1 provides the connection for a secondary emergency power system. The system requires any +12V dc source rated at 3 amperes continuous operation. The secondary emergency power source is pre-regulated into a +7V dc supply by U2. The output of U2 is applied to regulator U1 for emergency power applications.

SECTION V MAINTENANCE

5-1. INTRODUCTION.

5-2. This section provides general maintenance information, electrical adjustment procedures, and troubleshooting information for the Broadcast Electronics DV-2A digital audio recorder.

5-3. <u>SAFETY CONSIDERATIONS.</u>

5-4. Low voltages are used throughout the DV-2A circuit boards, however maintenance with power energized is always considered hazardous and caution should be observed. All high voltages have been shielded, however do not touch any components within the DV-2A chassis with power energized. Good judgment, care, and common sense must be practiced to prevent accidents. The procedures contained in this section should be performed only by experienced and trained maintenance personnel.

5-5. FIRST LEVEL MAINTENANCE.

5-6. First level maintenance consists of precautionary procedures applied to the equipment to prevent future failures. The procedures are performed on a regular basis and the results recorded in a performance log.

WARNING

DISCONNECT ALL DV-2A PRIMARY POWER BEFORE ATTEMPTING ANY EQUIPMENT MAINTENANCE.

5-7. GENERAL.

5-8. Clean the DV-2A chassis interior of accumulated dust as required using a nylon-bristle brush and vacuum cleaner. Check the circuit boards for improperly seated semiconductors and components damaged by overheating. Also, periodically check the circuit boards and chassis for loose hardware.

5-9. INTERNAL BATTERY BACK-UP SYSTEM.

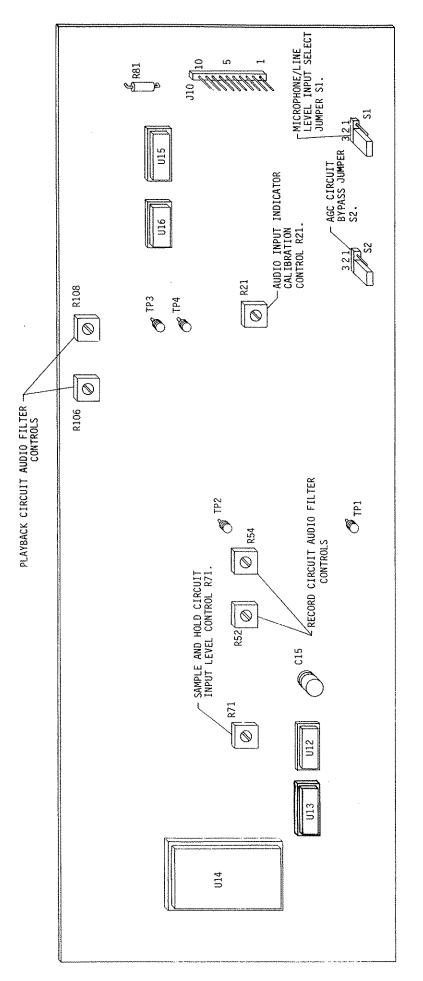
5-10. The batteries in the DV-2A internal emergency power system must be checked at regular intervals to ensure proper operation. It is strongly recommended that the batteries be inspected every three months. It is also recommended that the batteries be replaced every six months, regardless of the condition. If a power failure of approximately ten minutes occurs, the batteries in the system will discharge and require immediate replacement.

- 5-11. SECONDARY BATTERY BACK-UP SYSTEM.
- 5-12. If an automotive battery is used in the DV-2A secondary emergency power system, inspect the battery every three months for proper operation. Replace/recharge the battery as required to maintain peak operational performance.

5-13. SECOND LEVEL MAINTENANCE.

- 5-14. Second level maintenance consists of procedures required to restore the DV-2A to operation after a fault has occurred. The following procedures are divided into electrical adjustments and trouble-shooting.
- 5-15. The maintenance philosophy of the DV-2A consists of isolating a problem to a specific assembly with subsequent troubleshooting as required to isolate the defective components. The defective components may be repaired locally or the entire device may be returned to Broadcast Electronics, Inc. for repair or replacement.
- 5-16. ELECTRICAL ADJUSTMENTS.
- 5-17. The following text provides adjustment procedures for all controls associated with the DV-2A digital audio recorder. Refer to the procedures as required to adjust a specific control.
- 5-18. AUDIO CIRCUIT BOARD ADJUSTMENTS.
- 5-19. RECORD CIRCUIT AUDIO FILTER ALIGNMENT. Potentiometers R52 and R54 adjust the record circuit audio filter. Due to the critical function of the filter, field alignment is not recommended. Therefore, it is suggested the defective audio circuit board be returned to Broadcast Electronics Inc. for repair or exchange. If shipment to the factory is not practical, contact the Broadcast Electronics Customer Service Department for a recommended adjustment procedure and a list of required equipment.
- 5-20. PLAYBACK CIRCUIT AUDIO FILTER ALIGNMENT. Potentiometers R106 and R108 adjust the playback circuit audio filter. Due to the critical function of the filter, field alignment is not recommended. Therefore, it is suggested the defective audio circuit board be returned to Broadcast Electronics Inc. for repair or exchange. If shipment to the factory is not practical, contact the Broadcast Electronics Customer Service Department for a recommended adjustment procedure and a list of required equipment.
- 5-21. OUTPUT LEVEL ADJUSTMENT. OUTPUT VOLUME control R2 on the DV-2A rear-panel assembly adjusts the unit output level. Adjustment of the control will not be required unless a replacement potentiometer is installed. If output level adjustment is required, refer to SECTION II, INSTALLATION and perform the OUTPUT LEVEL adjustment procedure.

- 5-22. SAMPLE AND HOLD CIRCUIT INPUT LEVEL CALIBRATION. Potenti-ometer R71 adjusts the input level to the sample and hold circuit. Adjustment of the sample and hold circuit input level will not be required unless replacement components are installed in the circuit. To calibrate the sample and hold circuit, proceed as follows.
- 5-23. Required Equipment. The following equipment is required to calibrate the sample and hold circuit.
 - A. Number 2 Phillips Screwdriver, 4 inch (10.2 cm) blade.
 - B. Non-Metallic Adjustment Tool.
 - C. Calibrated Low Distortion Audio Generator, +26 dBm output, 600 Ohm output impedance (Potomac AG-51 or equivalent).
 - D. Calibrated Oscilloscope, 10 MHz bandwidth (Tektronix 7603 Oscilloscope Main Frame or equivalent).
- 5-24. <u>Procedure.</u> To adjust the sample and hold circuit input level, proceed as follows:
- 5-25. Disconnect the DV-2A primary power and remove the top-panel.
- 5-26. Connect the audio generator to the audio IN receptacle (J2) on the DV-2A rear-panel.
- 5-27. Connect the oscilloscope to the audio OUT receptacle (J1) on the DV-2A rear-panel.
- 5-28. Refer to Figure 5-1 and install:
 - 1. AGC circuit bypass jumper S2 in position 1-2.
 - 2. Microphone/Line level select jumper S1 in position 2-3.
- 5-29. Apply power to the DV-2A.
- 5-30. Adjust the audio generator for a 400 Hz output at +20 dBm.
- 5-31. Operate the STOP and RECORD switch/indicators to illuminate the switch/indicators.
- 5-32. Refer to Figure 5-1 and adjust sample and hold circuit input level calibration control R71 until the oscilloscope presentation begins to clip, then adjust the control slightly for an unclipped signal presentation.
- 5-33. Disconnect the DV-2A primary power.



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FIGURE 5-1. AUDIO CIRCUIT BOARD ADJUSTMENT CONTROLS

- 5-34. Remove all test equipment, install the audio circuit board jumpers in the desired positions, replace the DV-2A top-panel, and return the unit to service.
- 5-35. AUDIO INPUT INDICATOR CALIBRATION. Potentiometer R21 calibrates the audio input indicator. Adjustment of the control will not be required unless replacement components are installed in the indicator circuitry. To calibrate the audio input indicator, proceed as follows.
- 5-36. Required Equipment. The following equipment is required to calibrate the audio input indicator.
 - A. Number 2 Phillips Screwdriver, 4 inch (10.2 cm) blade.
 - B. Non-Metallic Adjustment Tool.
 - C. Calibrated Low Distortion Audio Generator, +26 dBm output, 600 Ohm output impedance (Potomac AG-51 or equivalent).
- 5-37. Procedure. To align the audio input indicator, proceed as follows:
- 5-38. Disconnect the DV-2A primary power and remove the top-panel.
- 5-39. Connect the audio generator to the audio IN receptacle (J2) on the DV-2A rear-panel.
- 5-40. Refer to Figure 5-1 and install:
 - A. AGC circuit bypass jumper S2 in position 1-2.
 - B. Microphone/Line level select jumper S1 in position 2-3.
- 5-41. Apply power to the DV-2A.
- 5-42. Adjust the audio generator for a 400 Hz output at -15 dBm.
- 5-43. Refer to Figure 5-1 and adjust audio input indicator calibration control R21 until the front-panel AUDIO INPUT indicator illuminates green.
- 5-44. Disconnect the DV-2A primary power.
- 5-45. Remove all test equipment, install the audio circuit board jumpers in the desired positions, replace the DV-2A top-panel, and return the unit to service.

5-46. TROUBLESHOOTING.

5-47. Troubleshooting within the DV-2A is not considered hazardous due to the low voltages and currents involved. All high voltages used within the DV-2A have been shielded; however, do not touch any component within the digital recorder when power is energized.

WARNING DISCONNECT ALL DV-2A PRIMARY POWER BEFORE REPLACING ANY COMPONENTS.

CAUTION INADVERTENT CONTACT BETWEEN ADJACENT COMPONENTS WITH TEST EQUIPMENT CAN CAUSE SERIOUS DAMAGE TO THE DV-2A CIRCUITRY.

- 5-48. The troubleshooting philosophy for the DV-2A consists of isolating a problem to a specific circuit board. The problem may be isolated by referencing the following information and Table 5-1 which presents DV-2A digital audio recorder troubleshooting.
- 5-49. Once trouble is isolated and power is totally deenergized, refer to the schematic diagrams and the theory of operation to assist in problem resolution. The defective component may be repaired locally or the entire device may be returned to Broadcast Electronics Inc. for repair or replacement.
- 5-50. MEMORY CIRCUIT BOARD TROUBLESHOOTING. The memory circuit contains twelve 32.7 second record time locations. The record locations are arranged in a sequential order and stored in corresponding memory circuit components (refer to Table 5-2). Memory circuit board troubleshooting consists of determining the defective record time location. Refer to Table 5-2 and determine the defective record time location and the corresponding memory circuit components.

TABLE 5-1. DV-2A TROUBLESHOOTING (Sheet 1 of 2)

SYMPTOM	REMEDY
DEFECTIVE AUDIO INPUT INDICATOR	 Check indicator DS1 on the front-panel circuit board. Check integrated circuit U15B on the audio circuit board. Check integrated circuit U4 on the audio circuit board.

TABLE 5-1. DV-2A TROUBLESHOOTING (Sheet 2 of 2)

(Shee	(Sheet 2 of 2)			
SYMPTOM	:	REMEDY		
DEFECTIVE TIME/SELECTION DISPLAY	1.	Check display components DS3 through DS5 on the front-panel circuit board.		
	2.	Check integrated circuits U40A U8, and U41D on the CPU circuit board.		
DEFECTIVE FRONT-PANEL BLANK MEMORY AND SWITCH INDICATORS	1.	Check integrated circuits U16 and U17 on the CPU circuit board.		
DEFECTIVE HEADPHONE SYSTEM	1.	Check transistors Q2 through Q5 on the audio circuit board.		
	2.	Check integrated circuit U23 on the audio circuit board.		
	3.	Check potentiometer R1 on the DV-2A front-panel.		
DEFECTIVE REMOTE CONTROL SYSTEM	1.	Check diodes CR2 through CR30 on the CPU circuit board.		
	2.	Check optical couplers U32 through U39 and U43 on the CPU circut board.		
	3.	Check inverters U3OA, U3OE, and U31 on the CPU circuit board.		
NO RECORD AUDIO	1.	Check the record audio playback system.		
	2.	Ensure jumper S1 is installed.		
	3.	Refer to Figure 5-2.		
NO PLAYBACK AUDIO	1.	Refer to Figure 5-3.		

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FIGURE 5-3. TROUBLESHOOTING TREE, NO PLAYBACK AUDIO

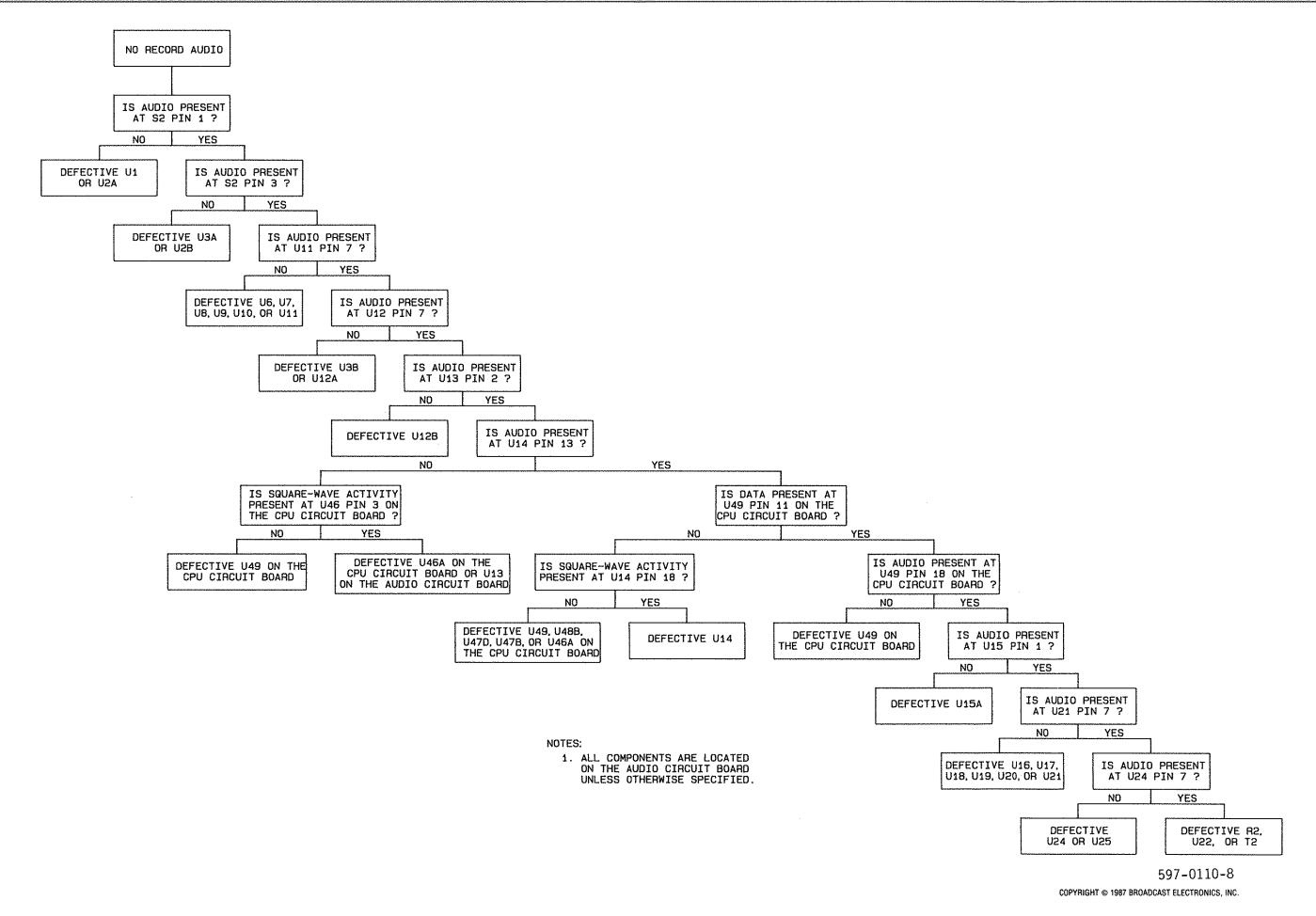


FIGURE 5-2. TROUBLESHOOTING TREE, NO RECORD AUDIO

TABLE 5-2. MEMORY CIRCUIT BOARD TROUBLESHOOTING.

RECORD TIME LOCATION	RECORD TIME (IN SECO		CORRESPONDING COMPON	
	FROM	T0	FROM	TO
1	0	32.7	U1	U8
2	32.7	65.5	U9	U16
3	65.5	98.3	U17	U24
4	98.3	131	U25	U32
5	131	163.8	U33	U40
6	163.8	196.6	U41	U48
7	196.6	229.4	U49	U56
8	229.4	262	U57	U64
9	262	294.9	U65	U72
10	294.9	327.7	U73	U80
11	327.7	360.5	U81	U88
12	360.5	389.1	U89	U96

5-51. CPU CIRCUIT BOARD TROUBLESHOOTING. Due to the complexity of the CPU circuit board design, troubleshooting is limited to: 1) circuit board substitution, 2) master clock circuit evaluation, and 3) integrated circuit substitution. If is determined the CPU circuit board is defective, perform the troubleshooting techniques as required or return the circuit board to Broadcast Electronics Inc. for repair or exchange.

WARNING	DISCONNECT POWER BEFORE REMOVING OR REPLACING CIRCUIT BOARDS OR COMPONENTS.
CAUTION	WHEN REPLACING A COMPONENT MOUNTED ON A HEAT-SINK, ENSURE A THIN FILM OF A ZINC-BASED
CAUTION	HEAT-SINK COMPOUND IS USED TO ASSURE GOOD HEAT DISSIPATION.

- 5-52. COMPONENT REPLACEMENT. The circuit boards used in the DV-2A are double-sided with plated-through holes. Due to the plated-through hole design, solder fills the holes by capillary action. This condition requires that defective components be removed carefully to avoid damage to the circuit board.
- 5-53. On all circuit boards, the adhesion between the copper trace and the circuit board fails at almost the same temperature as solder melts. A circuit board trace can be destroyed by excessive heat or lateral movement during soldering. Use of a small soldering iron with steady pressure is required for circuit board repairs.

- 5-54. To remove a soldered component from a circuit board, cut the leads from the body of the defective component while the device is soldered to the board. Grip a component lead with needle-nose pliers. Touch the soldering iron to the lead at the solder connection on the circuit side of the board. When the solder begins to melt, push the lead through the back side of the board and cut off the clinched end of the lead. Each lead may now heated independently and pulled out of each hole. The holes may be cleared of solder by careful re-heating with a low wattage iron and removing residual solder with a soldering vacuum tool.
- 5-55. Install the new component and apply solder from the circuit side of the board. If no damage has been incurred to the plated-through holes, soldering of the component side of the board will not be required.

WARNING

MOST SOLVENTS WHICH REMOVE ROSIN FLUX ARE VOLATILE AND TOXIC BY NATURE AND SHOULD BE USED ONLY IN SMALL AMOUNTS IN A WELL VENTILATED AREA AWAY FROM FLAME, CIGARETTES, AND HOT SOLDERING IRONS.

WARNING OBSERVE THE MANUFACTURERS CAUTIONARY INSTRUCTIONS.

- 5-56. After soldering, remove residual flux with a suitable solvent. Rubbing alcohol is highly diluted and is not effective.
- 5-57. The board should be checked to ensure the flux has been completely removed. Rosin flux is not normally corrosive, however in time, the flux will absorb enough moisture to become conductive and create problems.
- 5-58. INTEGRATED CIRCUITS. Special care should be exercised with integrated circuits. Each integrated circuit must be installed by matching the integrated circuit notch with the notch on the socket. Do not attempt to remove an integrated circuit from a socket with your fingers. Use an integrated circuit puller to lightly pry the component from the socket.

SECTION VI PARTS LISTS

6-1. INTRODUCTION.

6-2. This section provides descriptions and part numbers of electrical components, assemblies, and selected mechanical parts required for maintenance of the Broadcast Electronics DV-2A digital audio recorder. Each table entry in this section is indexed by reference designators appearing on the applicable schematic diagram.

TABLE 6-1. REPLACEABLE PARTS LISTS

TABLE NO.	DESCRIPTION	PART NO.	PAGE NO.
6-2	DV-2A FINAL ASSEMBLY	900-1000- 001 -30	•
6-3	MEMORY CIRCUIT BOARD ASSEMBLY	910-0038	6-3
6-4	FRONT PANEL CIRCUIT BOARD ASSEMBLY	910-0101	6-3
6-5	CPU CIRCUIT BOARD ASSEMBLY	910-0102	6-3
6-6	AUDIO CIRCUIT BOARD ASSEMBLY	910-0104	6-6
6-7	POWER SUPPLY CIRCUIT BOARD ASSEMBLY	910-0105	6-9
6-8	CABLE HARNESS ASSEMBLY	940-0031	6-10
6-9	ACCESSORY KIT	950-0038	6-10

TABLE 6-2. DV-2A FINAL ASSEMBLY - 900-1000-001/-301

REF. DES.	DESCRIPTION	PARY NO.	QYY.
C1 THRU C5	Capacitor, Electrolytic, 10 uF, 35V	023-1076	5
C6 THRU C10	Capacitor, Ceramic, 0.001 uF, 1kV	002-1034	5
D1	Diode, MR751, Silicon, 100V @ 6 Amperes	202-0751	1
	117V Operation —		
F1, SPARE	Fuse, AGC, 1 1/2A, 250V, Slow-Blow	334-0150	2
	220V Operation		
F1, SPARE	Fuse, AGC, 0.75A, 250V, Slow-Blow	334-0075	2
J1	Phone Jack, 1/4 Inch (0.635 cm), 3 Conductor (PHONES Receptacle)	417-0311	1
J2	Receptacle, Female, 3-Pin, XLR Type (IN Receptacle)	829-4214	1
J3	Receptacle, Male, 3-Pin, XLR Type (OUT Receptacle)	829-4213	1
J13	Connector Housing, 4-Pin	418-0233	1
P2	Connector Housing, 6-Pin	418-0670	1
R1	Potentiometer, Log Taper, 10 k Ohm ±10%, 1/2W (PHONES LEVEL Control)	191-1053	1
R2	Potentiometer, Cermet Linear, Slotted Shaft, 10 k Ohm ±10%, 1W (OUYPUY VOLUME Control)	191-1053D	1
R3	Resistor, 1.3 k Ohm ±5%, 1/4W	100-1343	1
R4	Resistor, 240 Ohm ±5%, 1/4W	100-2433	1
11	Transformer, Power,	370-0027	1
	Dual Primáry: 110V/22OV ±10%, 50/60 Hz, Single Phase Dual Secondary: ±18V dc @ 250 mA +10V dc @ 2A		
12	Transformer, Audio Output	371-0009	1
	Primary Impedance: 600 Ohms Secondary Impedance: 600 Ohms Frequency Response: ±2 dB, 30 Hz to 20 Hz Maximum Level: +15 dB		
ΥB1	Barrier Strip, 2 Terminals	412-0102	1
U1	Integrated Circuit, LM323K, Three-Terminal Fixed-Positive- Voltage Regulator, 5V @ 3 Amperes, TO-3 Case	227-0323	1
U2	Integrated Circuit, LM350K, Three-Terminal Adjustable Positive Voltage Regulator, 1.2 to 33V @ 3 Ampere, TO-3 Case	227-0350	1
U3	Integrated Circuit, MC7815Cĭ, Voltage Regulator, 15V @ 1A, TO-220 Case	227-7815C	1
U4	Integrated Circuit, LM7915CY, Voltage Regulator, -15V @ 1A, YO-220 Case	227-7915C	1
U5	Integrated Circuit, MC1805CY, Voltage Regulator, 5V @ 1.0 A, YO-220 Case	227-7805	1
# ** ** **	Receptacle, Connector (for P2)	417-0053	5
	Pin, Connector (for J13)	417-0036	4
	Insulator, Front Panel	407-0092	1
	Socket, Transistor, TO-3 (for U1 and U2)	417-0298	2
	Cover, Transistor, TO-3 (for U1)	407-3000	1
	Insulator, Mica, YO-3 (for U1 and U2)	418-0010	2
	Transistor Mounting Insulator, TO-220 Case (for U3, U4, and U5)	409-7403	3
	Spring, Battery Holder Fused Power Connector/Voltage Selector/EMI Filter, 120/240V	430-0016	1 1
	Fuse Clips, AGC	360-6504 415-1001	2
	Knob, Black, RB-67-0-SB Rogan (PHONES LEVEL)	415-1001 481-0022	1
	Blank Circuit Board, Battery Holder	510-0103	1
	Memory Circuit Board Assembly	910-0038	1
wat dath day and	Front Panel Circuit Board Assembly	910-0101	i
	CPU Circuit Board Assembly	910-0102	1
	Audio Circuit Board Assembly	910-0104	i
	Power Supply Circuit Board Assembly	910-0105	1
			_
***	Cable Harness Assembly	940-0031	1

TABLE 6-3. MEMORY CIRCUIT BOARD ASSEMBLY - 910-0038

REF. DES.	DESCRIPYION	PART NO.	QTY.
C1 THRU C96	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	96
C97 THRU C108	Capacitor, Silvered Mica, 100 pF ±5%, 500V	040-1022	12
C109 YHRU C117	Capacitor, Mica, 50 pF ±5%, 500V	040-5013	9
J1	Connector, Header, 40-Pin Dual In-line	417-0117	1
J2	Connector, 4-Pin	418-0255	1
U1 THRU U96	Integrated Circuit, 41256, 256K x 1 Dynamic Random Access Memory, 150 ns, 16-Pin DIP	220-4256	96
U97 THRU U110	Integrated Circuit, SN74LS244N, Octal Tri-State Bus Driver, 20-Pin DIP	228-2244	14
XU1 THRU XU96	Socket, 16-Pin DIP	417-1604	96
XU97 THRU XU110	Socket, 20-Pin DIP	417-2004	14
	Blank Circuit Board	510-0038	1

TABLE 6-4. FRONT PANEL CIRCUIT BOARD ASSEMBLY - 910-0101

REF. DES.	DESCRIPTION	PART NO.	QYY.
DS1	Indicator, LED, Green/Red Bi-Color, OPL710, Y-1 3/4 Bulb, 2.5V @ 40 mA Maximum	320-0018	1
DS 2	Indicator, LED, Yellow, 521-9176, 3V @ 40 mA Maximum	323-9225	1
DS3 THRU DS5	Indicator, LED, Numerical Display, HP-5082-7300	323-7300	3
J2	Connector, Header, 13-Pin Dual In-line	417-2600	1
S1	Switch, Momentary Contact, SPSY, LED, Green	340-0081	1
\$2	Switch, Momentary Contact, SPST, LED, Yellow	340-0080	1
\$3	Switch, Momentary Contact, SPSY, LED, Red	340-0079	1
54	Switch, Momentary Contact, SPSY, Gray	340-0078	1
\$5	Switch, Momentary Contact, SPSY, LED, Red	340-0079	1
\$6	Switch, Momentary Contact, SPSY, Gray	340-0078	1
S7	Switch, Momentary Contact, SPSY, LED, Yellow	340-0080	1
\$8	Switch, Momentary Contact, SPSY, Gray	340-0078	1
	Blank Circuit Board	510-0101	1

TABLE 6-5. CPU CIRCUIT BOARD ASSEMBLY - 910-0102 (Sheet 1 of 3)

REF. DES.	DESCRIPTION	PARY NO.	QTY.
C1	Capacitor, Mica, 10 pF ±5%, 500V	042-1012	1
C2	Capacitor, Mica, 1000pF ±5%, 500V	041-1032	1
C3	Capacitor, Electrolytic, 100 uF, 25V	023-1084	1
C4	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	1
C5 THRU C12	Capacitor, Electrolytic, 10 uF, 35V	023-1076	8
C13	Capacitor, Electrolytic, 22 uF, 50V	024-2274	1
C14 YHRU C16	Capacitor, Mica, 1000 pf ±5%, 500V	041-1032	3
C17,C18	Capacitor, Mica, 50 pF ±5%, 500V	040-5013	2
C19	Capacitor, Mica, 10 pF ±5%, 500V	042-1012	1
C20 THRU C25, C27 THRU C39, C41 THRU C58	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	37
C59	Capacitor, Mica, 33 pF ±5%, 500V	042-3312	1
CR1	Diode, 1N4148, Silicon, 75V @ 0.3 Amperes	203-4148	1
CR2 THRU CR30	Diode, 1N4005, Silicon, 600V @ 1 Ampere	203-4005	29
J1	Connector Header, 40-Pin Dual In-line	417-0117	1

TABLE 6-5. CPU CIRCUIT BOARD ASSEMBLY - 910-0102 (Sheet 2 of 3)

REF. DES.	DESCRIPTION	PART NO.	QĩY.
J2,J3	Receptacle, Male, 13-Pin Dual In-line	417-2600	2
J4, J5	Socket, 16-Pin DIP	417-1604	2
J6	Connector, Receptacle, 12-Pin	417-1276	1
Q1	Yransistor, 2N3906, PNP, Silicon, Y0-92 Case	210-3906	1
R1,R2	Resistor, 560 Ohm ±5%, 1/4W	100-5633	2
R3 R4 THRU R7	Resistor, 100 Ohm ±5%, 1/4W	100-1033	1
R8	Resistor, 10 k Ohm ±5%, 1/4W	100-1053	4
R9	Resistor, 1.2 k Ohm ±5%, 1/4W Resistor, 220 Ohm ±5%, 1/4W	100-1243 100-2233	1 1
R10 THRU R15	Resistor, 100 0hm ±5%, 1/4W	100-2233	6
R16	Resistor, 100 k Ohm ±5%, 1/4W	100-1063	1
R17	Resistor, 47 k Ohm ±5%, 1/4W	100-4753	1
R18 YHRU R39	Resistor, 220 Ohm ±5%, 1/4W	100-2233	22
R40 THRU R47	Resistor, 10 k Ohm ±5%, 1/4W	100-1053	8
R48	Resistor, 8.2 k Ohm ±5%, 1/4W	100-8243	1
R50	Resistor, 2.7 k Ohm, 1/4W	100-2743	1
R51	Resistor, 2.2 k Ohm, 1/4W	100-2243	1
R52 THRU R66	Resistor, 100 Ohm ±5%, 1/4W	100-1033	15
บ1	Integrated Circuit, SN74LS244N, Octal Yri-State Bus Driver, 20-Pin DIP	228-2244	1
U2	<pre>Integrated Circuit, 8255A, Programmable Peripheral Interface, 24 Parallel Input/Output Lines, 40-Pin DIP</pre>	229-8255	1
U3	Integrated Circuit, Z80H, Microprocessor, High Speed 8-Bit, 8 MHz Clock, 40-Pin DIP	220-0080	1
U4	Integrated Circuit, AM2764A-2DC, 8Kx8 EPROM, Programmed with the DV-2A Control Program, 28-Pin DIP	220-2764	1
U5 THRU U7	Integrated Circuit, SN74LS244N, Octal Tri-State Bus Driver,	228-2244	3
U8	20-Pin DIP Integrated Circuit, SN74LS155N, Schottky Decoder/	228-0006	1
U9 , U10	Demultiplexer, 16-Pin DIP Integrated Circuit, SN74LS93N, 4-Bit Binary Counter,	228-0010	2
U11	14-Pin DIP Integrated Circuit, SN74LS74AN, Dual D-Type Flip-Flop,	228-0074	1
U12,U13	14-Pin DIP Integrated Circuit, SN74S74N, Schottky, Dual D-Type	220-7474	2
U14	Positive-Edge-Triggered Flip-Flop, 14-Pin DIP Integrated Circuit, F74154PC, TTL, 4-Line to 6-Line Decoder,	228-4154	1
U15	24-Pin DIP Integrated Circuit, 74LSO8PC, Low Power Schottky, Quad	228-2408	1
U16	2-Input AND Gate, 14-Pin DIP Integrated Circuit, SN74LS377N, Octal D-Yype Flip-Flop,	228-2377	1
U17	20-Pin DIP Integrated Circuit, ULN2003A, 7 Section NPN Darlington	229-2003	1
U18	Driver, CMOS, 16-Pin DIP Integrated Circuit, 74LSO8PC, Low Power Schottky, Quad	228-2408	1
U19 , U20	2-Input AND Gate, 14-Pin DIP Integrated Circuit, 74SOON, Schottky, Quad 2-Input NAND	220-7400	2
U 2 1	Gate, 14-Pin DIP Integrated Circuit, SN74LS244N, Octal Tri-State Bus Driver,	228-2244	1
U22	20-Pin DIP Integrated Circuit, SN74LS14N, Hex Schmitt-Trigger Inverter,	228-2414	1
U23	14-Pin DIP Integrated Circuit, ULN2003A, 7 Section NPN Darlington	229-2003	1
U24	Driver, CMOS, 16-Pin DIP Integrated Circuit, SN74SO4N, Schottky Hex Inverter,	228-0008	1
U25	14-Pin DIP Integrated Circuit, SN74LS244N, Octal Tri-State Bus Driver,	228-2244	1
U26	20-Pin DIP Integrated Circuit, NE555N, Timer, 8-Pin DIP	229-0555	1
U27	Integrated Circuit, 74LSO8PC, Low Power Schottky, Quad	228-2408	1
U28	2-Input AND Gate, 14-Pin DIP Integrated Circuit, SN74LS244N, Octal Yri-State Bus Driver,	228-2244	1
U29	20-Pin DIP Integrated Circuit, SN74S74N, Schottky, Dual D-Type	220-7474	1

TABLE 6-5. CPU CIRCUIT BOARD ASSEMBLY - 910-0102 (Sheet 3 of 3)

REF. DES.	DESCRIPTION	PART NO.	QTY.
U30,U31	Integrated Circuit, SN74LS14N, Hex Schmitt-Trigger Inverter,	228-2414	2
U32 THRU U39	14-Pin DIP Integrated Circuit, 4N33, Optical Isolator, NPN Photo Transistor/Infared Emitting Diode Type, 1500V Isolation,	229-0033	8
U40	Response: 30 kHz Maximum, Current: 50 mA Maximum, 6-Pin DIP Integrated Circuit, SN74LS244N, Octal Tri-State Bus Driver,	228-2244	1
U41	20-Pin DIP Integrated Circuit, SN74LS10N, Low Power Schottky, 3-Input	228-2410	1
U42	NAND Gate, 14-Pin DIP Integrated Circuit, 74L508PC, Low Power Schottky, Quad	228-2408	1
U43	2-Input AND Gate, 14-Pin DIP Integrated Circuit, 4N33, Optical Isolator, NPN Photo Transistor/Infared Emitting Diode Type, 1500V Isolation,	229-0033	1
U46	Response: 30 kHz Maximum, Current: 50 mA Maximum, 6-Pin DIP Integrated Circuit, MC14013CP, Dual D-Type Flip-Flop, CMOS, 14-Pin DIP	228-4013	1
U47	Integrated Circuit, MC14011BCP, Quad 2-Input NAND Gate, CMOS, 14-Pin DIP	228-4011	1
U48	Integrated Circuit, MC14013BCP, Dual D-Type Flip-Flop, CMOS, 14-Pin DIP	228-4013	1
U49 U50	Integrated Circuit, Encoder/Decoder Integrated Circuit, SN74LS245N, Octal Tri-State Bus Driver, 20-Pin DIP	220-1000 220-0245	1 1
XU1	Socket, 20-Pin DIP	417-2004	1
XU2,XU3	Socket, 40-Pin DIP	417-4005	2
XU4	Socket, 28-Pin DIP	417-2804	1
XU5 THRU XU7	Socket, 20-Pin DIP	417-2004	3
XU8	Socket, 16-Pin DIP	417-1604	1
XU9 THRU XU13	Socket, 14-Pin DIP	417-1404	5
XU14	Socket, 24-Pin DIP	417-2404	1
XU15	Socket, 14-Pin DIP	417-1404	1
XU16	Socket, 20-Pin DIP	417-2004	1
XU17	Socket, 16-Pin DIP	417-1604	1
XU18 THRU XU20	Socket, 14-Pin DIP	417-1404	3
XU21	Socket, 20-Pin DIP	417-2004	1
XU22	Socket, 14-Pin DIP	417-1404	1
XU23	Socket, 16-Pin DIP	417-1604	1
XU24	Socket, 14-Pin DIP	417-1404	1
XU25	Socket, 20-Pin DIP	417-2004	1
XU26	Socket, 8-Pin DIP	417-0804	1
XU27	Socket, 14-Pin DIP	417-1404	1
XU28	Socket, 20-Pin DIP	417-2004	1
XU29 THRU XU31	Socket 14-Pin DIP	417-1404	3
XU32 THRU XU39	Socket, 6-Pin DIP	417-0600	8
XU40	Socket, 20-Pin DIP	417-2004	1
XU41,XU42	Socket, 14-Pin DIP	417-1404	2
XU43	Socket, 6-Pin DIP	417-0600	1
XU46 THRU XU48	Socket, 14-Pin DIP	417-1404	3
XU49	Socket, 24-Pin DIP	417-2404	1
XU50	Socket, 20-Pin DIP	417-2004	1
Y1	Crystal, 16 MHz ±0.05% from -20°C to 50°C, A/T Cut, NE18A Case	390-0015	1
Y2	Crystal, 768 kHz ±0.01% from 0°C to 50°C, D/T Cut, NE33 Case	390-0016	1
	Blank Circuit Board	510-0102	1

TABLE 6-6. AUDIO CIRCUIT BOARD ASSEMBLY - 910-0104 (Sheet 1 of 4)

REF. DES.	DESCRIPTION	PART NO.	QTY.
C1,C2	Capacitor, Electrolytic, 10 uF, 25V, Non-Polarized	023-1075	2
C3	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	1
C4 THRU C6	Capacitor, Sivered Mica, 100 pF ±5%, 500V	040-1022	3 2
C7,C8 C9	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	2
C10	Capacitor, Electrolytic, 10 uF, 25V, Non-Polarized	023-1075	1
C10	Capacitor, Silvered Mica, 100 pF ±5%, 500V	040-1022	1 1
C12	Capacitor, Electrolytic, 100 uF, 25V Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	023-1084	1
C12	Capacitor, Electrolytic, 10 uF, 25V, Non-Polarized	003-1054	1
C14	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	023-1075	1 1
C15	Capacitor, Electrolytic, 100 uF, 25V	003-1054 023-1084	i 1
C16,C17	Capacitor, Electrolytic, 10 uF, 25V, Non-Polarized	023-1004	1 2
C18	Capacitor, Electrolytic, 1 uF, 50V	024-1064	1
C19,C20	Capacitor, Electrolytic, 10 uF, 25V, Non-Polarized	023-1075	1 2
C21	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	í
C22	Capacitor, Electrolytic, 10 uF, 25V, Non-Polarized	023-1075	i
C23 THRU	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	4
C26		000 100.	•
C27,C28	Capacitor, Mica, 500 pF ±1%, 500V	042-5021	2
C29,C30	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	$\bar{2}$
C31,C32	Capacitor, Mica, 500 pF ±1%, 500V	042-5021	$\bar{\tilde{2}}$
C33,C34	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	2 2 2 2 2
C35,C36	Capacitor, Mica, 500 pF ±1%, 500V	042-5021	2
C37,C38	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	2
C39	Capacitor, Mica, 1000 pF ±1%, 100V	041-1031	1
C40	Capacitor, Electrolytic, 10 uF, 25V Non-Polarized	023-1075	1
C41	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	1
C42 THRU	Capacitor, Electrolytic, 10 uF, 25V, Non-Polarized	023-1075	3
C44			
C45	Capacitor, Electrolytic, 1 uF, 50V	024-1064	1
C46,C47	Capacitor, Electrolytic, 10 uF, 25V, Non-Polarized	023-1075	2
C48	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	1
C49	Capacitor, Electrolytic, 10 uF, 25V, Non-Polarized	023-1075	1
C50	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	1
C51	Capacitor, Mica, 1000 pF ±1%, 100V	041-1031	1
C52,C53	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	2
C54	Capacitor, Electrolytic, 10 uF, 35V	023-1076	1
C55	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	1
C56	Capacitor, Electrolytic, 10 uF, 35V	023-1076	1
C57 THRU	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	7
C63	Assertice Mississian and Elegan N. B. J. C.	004 0004	_
C64	Capacitor, Electrolytic, 3.3 uF, 50V, Non-Polarized	024-3364	1
C65	Capacitor, Mica, 33 pF ±5%, 500V	042-3312	1
C67,C68	Capacitor, Mica, 500 pF ±1%, 500V	042-5021	2
C69 THRU	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	4
C72 C73,C74	Capacitor, Mica, 500 pF ±1%, 500V	042-5021	2
C75 THRU	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	2
C78	capacitor, nonotycine ceramite, o.t ut 120%, 500	003-1034	4
C79,C80	Capacitor, Mica, 500 pF ±1%, 500V	042-5021	2
C81 THRU	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	4
C84	capacitor, nonosyume decimine, off at 120%, 50%	003 1034	77
C85	Capacitor, Mica, 1000 pF ±1%, 100V	041-1031	1
C86	Capacitor, Electrolytic, 10 uF, 25V, Non-Polarized	023-1075	i
C87,C88	Capacitor, Electrolytic, 10 uF, 35V	023-1076	ż
C89	Capacitor, Mica, 33 pF ±5%, 500V	042-3312	ī
C90	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	i
C91	Capacitor, Electrolytic, 10 uF, 25V, Non-Polarized	023-1075	i
C92	Capacitor, Silvered Mica, 100 pF ±5%, 500V	040-1022	i
C93,C94	Capacitor, Mica, 22 pF ±5%, 500V	040-2213	ż
C95	Capacitor, Mylar, 0.22 uF ±10%, 100V	030-2253	1
C96	Capacitor, Ceramic, 0.001uF ±10%, 200V	030-1033	1
C97	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	1
C98	Capacitor, Mylar, 0.01 uF ±10%, 100V	031-1043	1
C99	Capacitor, Polyester, 0.47 uF ±10%, 100V	038-4753	1
C100	Capacitor, Mica, 500 pF ±1%, 500V	042-5021	1

TABLE 6-6. AUDIO CIRCUIT BOARD ASSEMBLY - 910-0104 (Sheet 2 of 4)

REF. DES.	DESCRIPTION	PART NO.	QTY.
C101	Capacitor, Electrolytic, 22 uF, 50V	024-2274	1
C102,C103	Capacitor, Monolythic Ceramic, 0.1 uF ±20%, 50V	003-1054	2
C104	Capacitor, Electrolytic, 10 uF, 25V, Non-Polarized	023-1075	1
D1,D2	Diode, Silicon Zener, 1N4728, 3.3V ±5%, 1W	201-4728	2
D3,D4	Diode, 1N4148, Silicon, 75V @ 0.3 Amperes	203-4148	2
D5,D6	Diode, Silicon Zener, 1N4728, 3.3V ±5%, 1W	201-4728	2 2
D7,D8	Diode, 1N4148, Silicon, 75V @ 0.3 Amperes	203-4148	2
J1Ó THRU	Connector Header, 8-Pin In-line	417-0080	3
J12	·		_
J13	Socket, 16-Pin DIP	417-1604	1
J14	Socket, 4-Pin	418-0255	1
MOV1,MOV2	Metal Óxide Varistor, V47MA2A, 27V ac RMS, 0.19 Joules	140-0017	ż
Q2	Transistor, 2N3904, NPN, Silicon, TO-92 Case	211-3904	1
Q3	Transistor, 2N3906, PNP, Silicon, TO-92 Case	210-3906	i
Q4	Transistor, TIP32A, PNP, Silicon, TO-220 AB Case	218-0032	i
Q5	Transistor, TIP31A, NPN, Silicon, TO-220 AB Case	219-0031	i
R1	Resistor, 20 k Ohm ±5%, 1/4W		1
R2		100-2053	1
R3	Resistor, 100 k Ohm ±5%, 1/4W	100-1063	1
	Resistor, 20 k Ohm ±5%, 1/4W	100-2053	1
R4	Resistor, 100 k Ohm ±5%, 1/4W	100-1063	1
R5	Resistor, (REFER TO RN16)	400 4000	
R6	Resistor, 100 Ohm ±5%, 1/4W	100-1033	1
R7 THRU R13	Resistor, (REFER TO RN16)		_
R14 THRU	Resistor, 470 k Ohm ±5%, 1/4W	100-4763	3
R16			
R17	Resistor, 10 k Ohm ±5%, 1/4W	100-1053	1
R18	Resistor, 16 k Ohm ±5%, 1/4W	100-1653	1
R19	Resistor, 1 k Ohm ±5%, 1/4W	100-1043	1
R20	Resistor, 91 k Ohm ±5%, 1/4W	100-9153	1
R21	Potentiometer, 1 Meg Ohm ±20%, 1W	177-1074	1
R22,R23	Resistor, 9.1 k Ohm ±5%, 1/4W	100-9143	2
R25,R26	Resistor, 100 k Ohm ±5%, 1/4W	100-1063	1 2 2 1
R27	Resistor, 3 k Ohm ±5%, 1/4W	100-3043	1
R28	Resistor, 1 k Ohm ±5%, 1/4W	100-1043	1
R29	Resistor, 470 Ohm ±5%, 1/4W	100-4733	1
R30	Resistor, 95.3 k Ohm ±1%, 1/4W	103-9535	1
R31	Resistor, 76.8 k Ohm ±1%, 1/4W	103-7685	1
R32	Resistor, 95.3 k Ohm ±1%, 1/4W	103-9535	1
R33,R34	Resistor, 100 k Ohm ±1%, 1/4W	103-1062	2
R35	Resistor, 76.8 k Ohm ±1%, 1/4W	103-7685	1
R36	Resistor, 6810 Ohms ±1%, 1/4W	103-6814	i
R37,R38	Resistor, 100 k Ohm ±1%, 1/4W	103-1062	ż
R39	Resistor, 7680 Ohms ±1%, 1/4W	103-7684	1
R40	Resistor, 53.6 k Ohm ±1%, 1/4W	103-5365	i
	Resistor, 205 k Ohm ±1%, 1/4W	103-2056	2
R41,R42	Resistor, 100 k Ohm ±1%, 1/4W	103 2030	2
R43,R44			1
R45	Resistor, 53.6 k Ohm ±1%, 1/4W	103-5365	
R46	Resistor, 17.8 k Ohm ±1%, 1/4W	103-1785	1
R47,R48	Resistor, 100 k 0hm ±1%, 1/4W	103-1062	2
R49	Resistor, 40.2 k Ohm ±1%, 1/4W	103-4025	1
R50	Resistor, 787 k Ohm ±1%, 1/4W	103-7876	1
R51	Resistor, 45.3 k Ohm ±1%, 1/4W	103-4535	1
R52	Potentiometer, 5 k Ohm ±10%, 1/2W	177-5044	1
R53	Resistor, 620 k Ohm ±1%, 1/4W	100-6263	1
R54	Potentiometer, 100 k Ohm ±10%, 1/2W	177-1064	1
R55,R56	Resistor, 100 k Ohm ±1%, 1/4W	103-1062	2 1
R57	Resistor, 47.5 k Ohm ±1%, 1/4W	103-4755	1
R58	Resistor, 12.4 k Ohm ±1%, 1/4W	103-1245	1
R59,R60	Resistor, 100 k Ohm ±1%, 1/4W	103-1062	2 1
R61	Resistor, 66.5 k Ohm ±1%, 1/4W	103-6655	1
R62	Resistor, 75 k Ohm ±5%, 1/4W	100-7553	1
	Resistor, 10 k 0hm ±5%, 1/4W	100-1053	1
R63	1/03/30014 10 K 01111 12/04 1/711	100 1000	
R63 R64	Resistor, 91 k Ohm ±5%, 1/4W	100-9153	i

TABLE 6-6. AUDIO CIRCUIT BOARD ASSEMBLY - 910-0104 (Sheet 3 of 4)

REF. DES.	DESCRIPTION	MADT NO	
		PART NO.	QTY.
R66	Resistor, 16 k Ohm ±5%, 1/4W	100-1653	1
R67,R68 R69	Resistor, 9.1 k Ohm ±5%, 1/4W	100-9143	2
R70	Resistor, 100 Ohm ±5%, 1/4W	100-1033	1
R71	Resistor, 51 k Ohm ±5%, 1/4W	100-5153	1
R81	Potentiometer, 10 k Ohm ±10%, 1/2W Resistor, 20 k Ohm ±5%, 1/4W	177-1054	1
R82	Resistor, 10 k Ohm ±5%, 1/4W	100-2053	1
R83	Resistor, 120 k Ohm ±5%, 1/4W	100-1053	1
R84	Resistor, 100 k Ohm ±1%, 1/4W	100-1263	1
R85	Resistor, 95.3 k Ohm ±1%, 1/4W	103-1062	1
₹86	Resistor, 76.8 k Ohm ±1%, 1/4W	103-9535 103-7685	1
R87	Resistor, 95.3 k Ohm ±1%, 1/4W	103-7665	1 1
R88	Resistor, 100 k Ohm ±1%, 1/4W	103-1062	1
R89	Resistor, 76.8 k Ohm ±1%, 1/4W	103-7685	i
390	Resistor, 6810 Ohms ±1%, 1/4W	103-6814	i
R91,R92	Resistor, 100 k Ohm ±1%, 1/4W	103-1062	2
₹93	Resistor, 7680 Ohms ±1%, 1/4W	103-7684	1
R94	Resistor, 205 k Ohm ±1%, 1/4W	103-2056	i
R95	Resistor, 53.6 k Ohm ±1%, 1/4W	103-5365	i
R96	Resistor, 205 k Ohm ±1%, 1/4W	103-2056	i
R97,R98	Resistor, 100 k Ohm ±1%, 1/4W	103-1062	2
₹99	Resistor, 53.6 k Ohm ±1%, 1/4W	103-5365	1
R100	Resistor, 17.8 k Ohm ±1%, 1/4W	103-1785	i
R101,R102	Resistor, 100 k Ohm ±1%, 1/4W	103-1062	ż
103	Resistor, 40.2 k Ohm ±1%, 1/4W	103-4025	ī
1104	Resistor, 787 k Ohm ±1%, 1/4W	103-7876	ì
1105	Resistor, 45.3 k Ohm ±1%, 1/4W	103-4535	i
2106	Potentiometer, 5 k Ohm ±10%, 1/2W	177-5044	i
1107	Resistor, 732 k Ohm ±1%, 1/4W	103-7326	i
2108	Potentiometer, 100 k Ohm ±10%, 1/2W	177-1064	i
R109,R110	Resistor, 100 k Ohm ±1%, 1/4W	103-1062	ż
2111	Resistor, 47.5 k Ohm ±1%, 1/4W	103-4755	1
R112	Resistor, 12.4 k Ohm ±1%, 1/4W	103-1245	i
R113,R114	Resistor, 100 k 0hm ±1%, 1/4W	103-1062	2
₹115	Resistor, 66.5 k Ohm ±1%, 1/4W	103-6655	1
₹116	Resistor, 10 Ohm ±5%, 1/4W	100-1023	1
R117	Resistor, 11.5 k Ohm ±1%, 1/4W	103-1155	1
₹118	Resistor, 34.8 k Ohm ±1%, 1/4W	103-3485	1
8119	Resistor, 301 Ohm ±1%, 1/4W	100-3031	1
1120	Resistor, 100 k Ohm ±5%, 1/4W	100-1063	1
1121	Resistor, 10 k Ohm ±1%, 1/4W	100-1051	1
1122	Resistor, 8.25 k Ohm ±1%, 1/4W	103-8254	1
123	Resistor, 40.2 k Ohm ±1%, 1/4W	103-4025	1
1124	Resistor, 10 Ohm ±5%, 1/4W	100-1023	1
125	Resistor, 301 Ohm ±1%, 1/4W	100-3031	1
126	Resistor, 1 k Ohm ±1%, 1/4W	100-1041	1
127	Resistor, 10 k Ohm ±5%, 1/4W	100-1053	1
128	Resistor, 1 k Ohm ±1%, 1/4W	100-1041	1
129	Resistor, 3.16 k Ohm $\pm 1\%$, $1/4W$	103-3164	1
130	Resistor, 1.5 k Ohm ±5%, 1/4W	100-1543	1
131	Resistor, 100 Ohm ±5%, 1/4W	100-1033	1
132	Resistor, 1.5 k Ohm ±5%, 1/4W	100-1543	1
133,R134	Resistor, 10 Ohm ±5%, 1W	120-1023	2
135	Resistor, 33 k Ohm ±5%, 1/4W	100-3353	1
1136	Resistor, 47 k Ohm ±5%, 1/4W	100-4753	1
2137	Resistor, 220 k Ohm ±5%, 1/4W	100-2263	1
1138	Resistor, 7.5 k Ohm ±5%, 1/4W	100-7543	1
8139	Resistor, 100 k Ohm ±5%, 1/4W	100-1063	1
2140	Resistor, 15 k Ohm ±5%, 1/4W	100-1553	1
1141	Resistor, 1.5 Meg Ohm ±5%, 1/4W	100-1573	1
1142	Resistor, 4.7 k Ohm ±5%, 1/4W	100-4743	1
R143	Resistor, 150 k Ohm ±5%, 1/4W	100-1563	1

TABLE 6-6. AUDIO CIRCUIT BOARD ASSEMBLY - 910-0104
(Sheet 4 of 4)

REF. DES.	DESCRIPTION	PART NO.	QTY.
R144	Resistor, 1.5 Meg Ohm ±5%, 1/4W	100-1573	1
R145	Resistor, 68 k Ohm ±5%, 1/4W	100-6853	1
R146,R147	Resistor, 10 Ohm ±5%, 1/4W	100-1023	2
R148	Resistor, 5.1 k Ohm ±5%, 1/4W	100-5143	1
RN16	Resistor Network, 8-10 k Ohm ±1%, 1/4W, 16-Pin DIP	226-1055	1
S1,S2	Switch, Jumper, Programmable, 2-Pin	340-0004	2
U1 , U2	Integrated Circuit, NE5532A, Dual Low Noise Operational Amplifier, 8-Pin DIP	221-5532	2
U3	Integrated Ćircuit, NE572N, Programmable Analog Compandor, 16-Pin DIP	220-0572	1
U4,U6 THRU U11	Integrated Circuit, TL072CP, Dual JFET-Input Operational Amplifier, 8-Pin DIP	221-0072	7
Ŭ12	Integrated Circuit, NE5532A, Dual Low Noise Operational Amplifier, 8-Pin DIP	221-5532	1
U13	Integrated Circuit, HA1-2425-5, Sample and Hold Circuit, MOSFET, 14-Pin DIP	220-2425	1
U14	Integrated Circuit, ADC80AG-12, Analog-to-Digital Converter, 12-Bit, 32-Pin DIP	220-0800	1
U15 THRU U21	Integrated Circuit, TLO72CP, Dual JFET-Input Operational Amplifier, 8-Pin DIP	221-0072	7
U22	Integrated Circuit, NE5532A, Dual Low Noise Operational Amplifier, 8-Pin DIP	221-5532	1
U23	Integrated Ćircuit, NE5534AN, Low Noise Operational Amplifier, 8-Pin DIP	221-5534	1
U24	Integrated Circuit, TLO72CP, Dual JFET-Input Operational Amplifier, 8-Pin DIP	221-0072	1
U25	Integrated Circuit, CRL2200, Single-Channel Noise Reduction System, 16-Pin DIP	220-2200	1
XU1,XU2	Socket, 8-Pin DIP	417-0804	10
XU3	Socket, 16-Pin DIP	417-1604	1
XU4,XU6 THRU XU12	Socket, 8-Pin DIP	417-0804	9
XU13	Socket, 14-Pin DIP	417-1404	1
XU14	Socket, 32-Pin DIP	417-3200	1
XU15 THRU XU24	Socket, 8-Pin DIP	417-0804	10
XU25	Socket, 16-Pin DIP	417-1604	1
	Connector Header, 3-Pin In-Line	417-0003	2
	Blank Circuit Board	510-0104	1

TABLE 6-7. POWER SUPPLY CIRCUIT BOARD ASSEMBLY - 910-0105

REF. DES.	DESCRIPTION	PART NO.	QTY.
C1 THRU C4	Capacitor, Electrolytic, 4700 uF, 50V	014-4793	4
D1 THRU D4	Diode, MR502, Silicon, 200V @ 3 Amperes	202-0502	4
D5 THRU D8	Diode, MR751, Silicon, 100V @ 6 Amperes	202-0751	4
D9 THRU D11	Diode, 1N4005, Silicon, 600V @ 1 Ampere	203-4005	3
D12.D13	Diode, MR751, Silicon, 100V @ 6 Amperes	202-0751	2
D14	Diode, 1N4005, Silicon, 600V @ 1 Ampere	203-4005	1
J1	Connector, 12-Pin	417-1276	1
J2	Receptacle, Male, 6-Pin	417-0677	1
J3	Connector, 9-Pin	418-0900	1
	Blank Circuit Board	510-0105	ĺ

TABLE 6-8. CABLE HARNESS ASSEMBLY - 940-0031

REF. DES.	DESCRIPTION	PART NO.	QTY.
J1	Connector, Female, 25-Pin D-Type (Remote Control)	417-0129	1
P1	Connector, Housing, 12-Pin	418-1271	1
P1,P1	Connector, Ribbon Cable, 40-Pin Dual In-Line	417-0118	2
P1, P2, P3	Connector, Ribbon Cable, 26-Pin Dual In-line	417-0047	3
P2	Connector, Housing, 4-Pin	418-0240	1
P3	Connector, 9-Pin	417-0059	1
P5	Connector, Ribbon Cable, 16-Pin Dual In-line	417-1602	2
P6	Connector, Housing, 12-Pin	418-1271	1
P10 THRU P12	Connector, Housing, 8-Pin	417-0046	3
P13.P14	Connector, Housing, 4-Pin	418-0240	2
P15 THRU P17	Socket, Transistor, TO-220	417-0216	3
	Pins, Connector (for P15, P16, and P17)	417-0217	9
	Pins, Connector (for P10, P11, and P12)	417-8766	19
	Pins, Connector (for P1, P2, P3, P6, P13, and P14)	417-0053	39

TABLE 6-9. ACCESSORY KIT - 950-0038

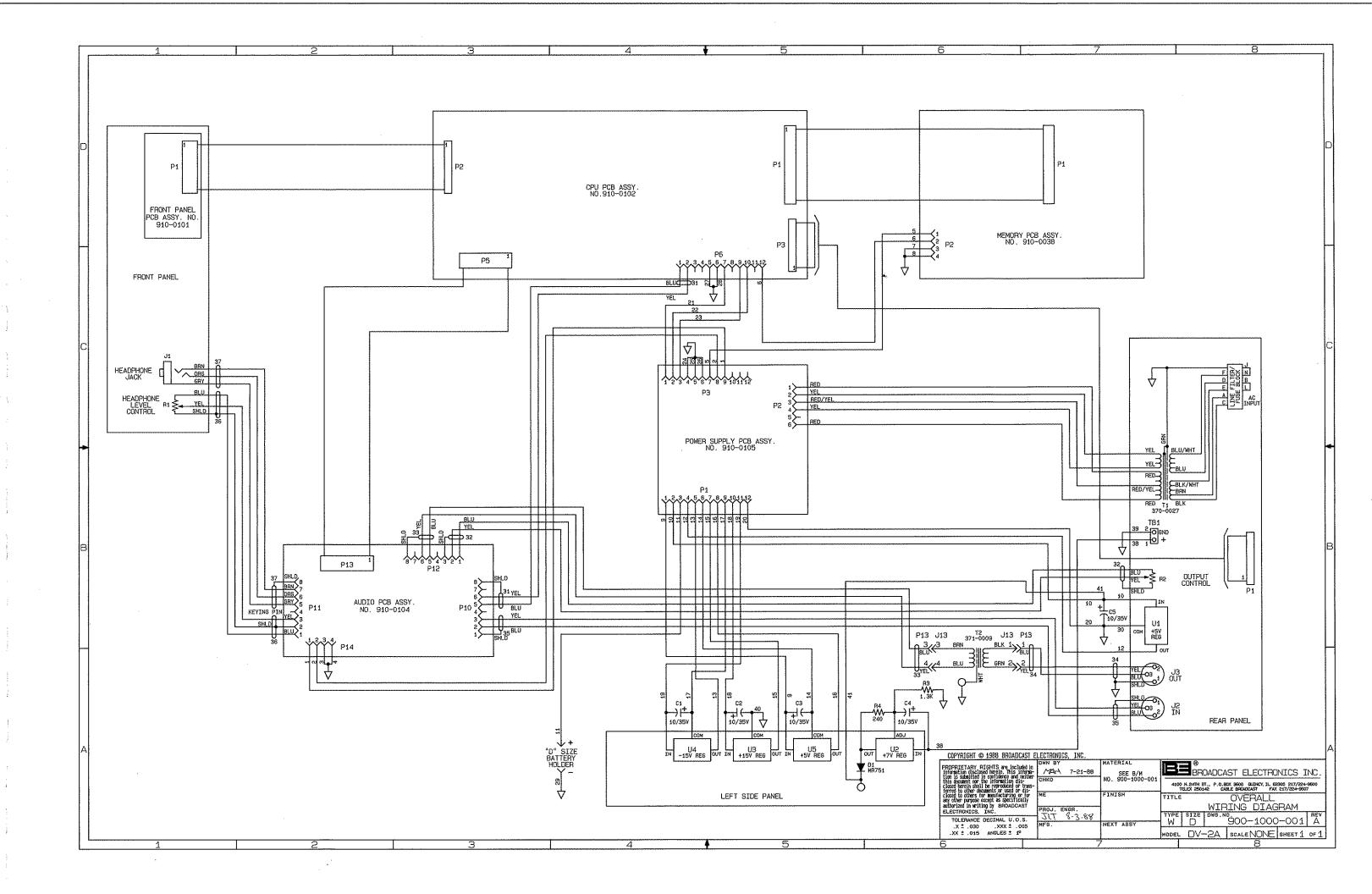
REF. DES.	DESCRIPTION	PART NO.	QYY.
	AC Line Cord, N.E.M.A. 3-Wire North American Plug	682-0001	1
	Plug, 25-Pin, D-Type	418-3219	1
	Connector Housing	418-3223	1
	Plug, Male, 3-Pin, XLR Type (for Input J2)	829-4217	1
	Plug, Female, 3-Pin, XLR Type (for Output J3)	829-4216	1

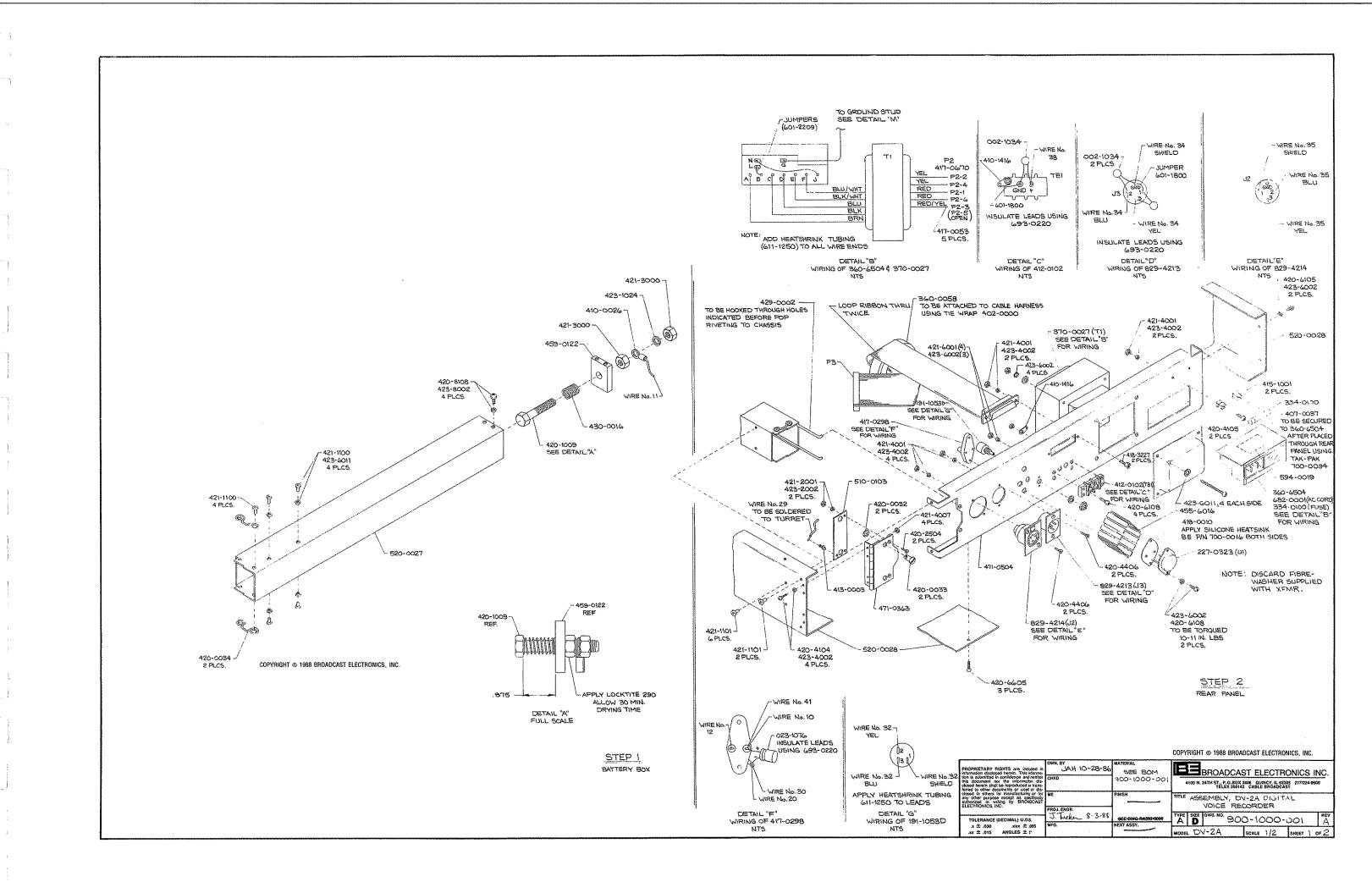
SECTION VII DRAWINGS

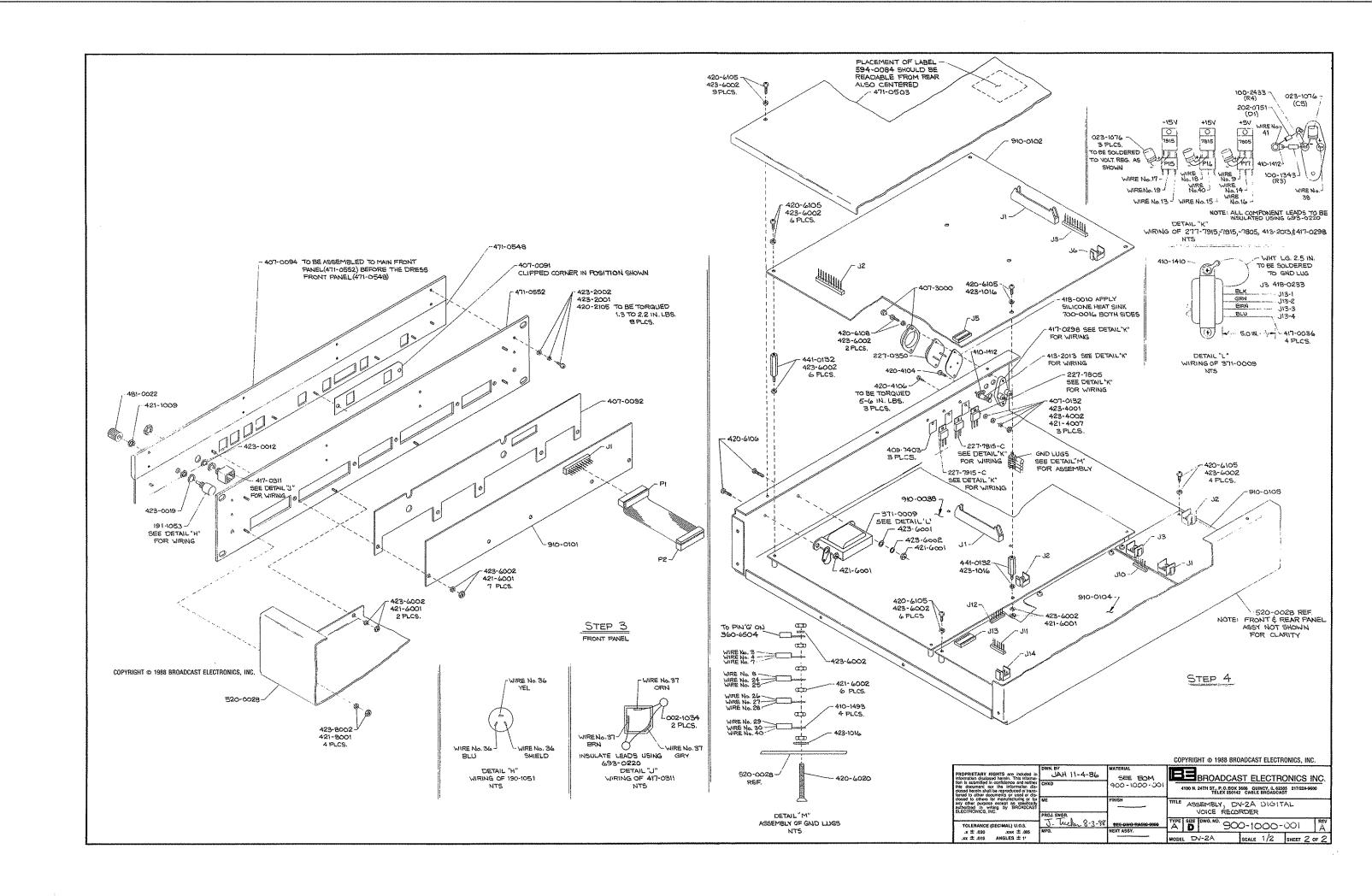
7-1. <u>INTRODUCTION</u>.

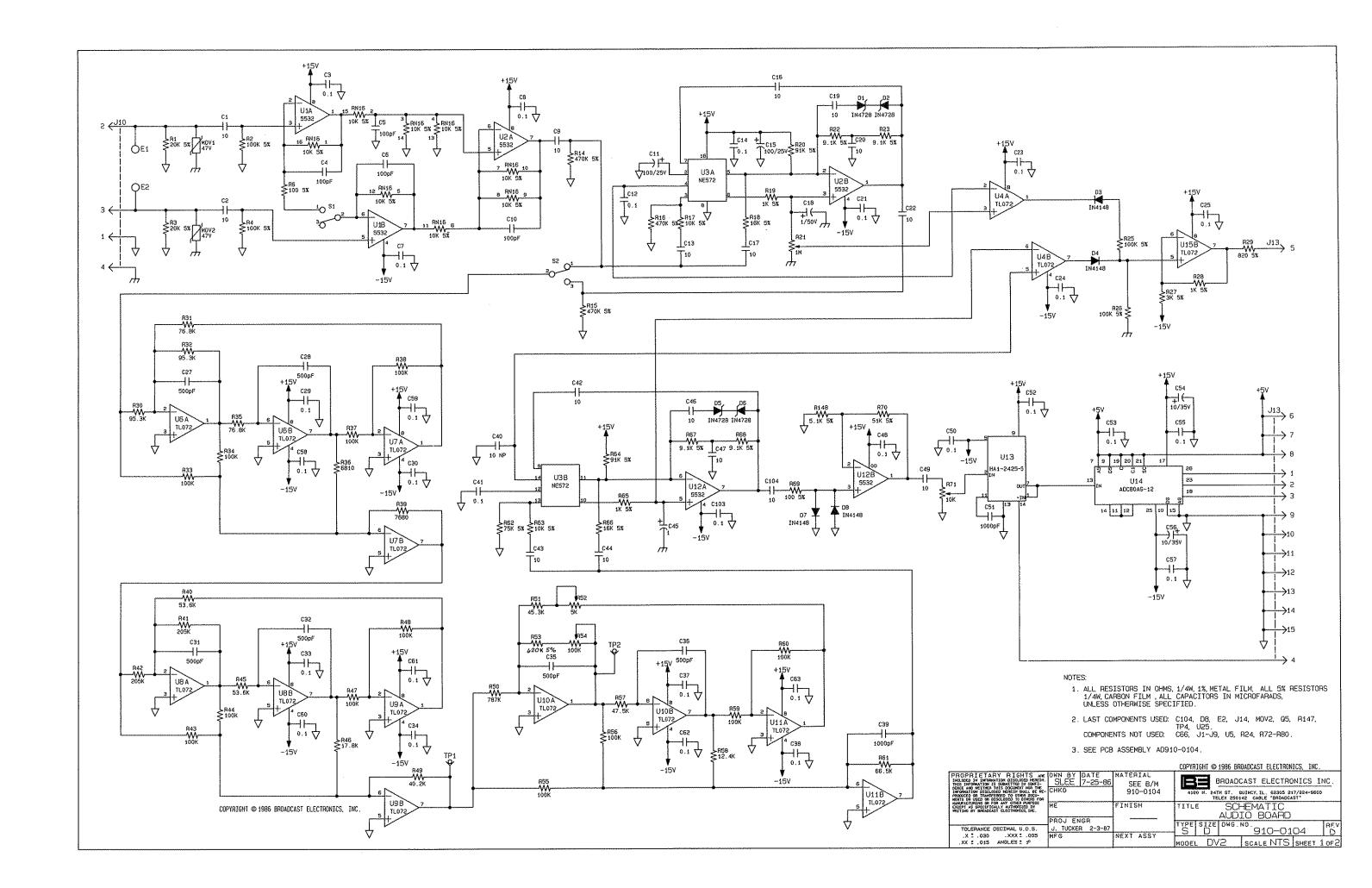
7-2. This section provides assembly drawings, wiring diagrams, and schematic diagrams as listed below for the Broadcast Electronics DV-2A digital audio recorder.

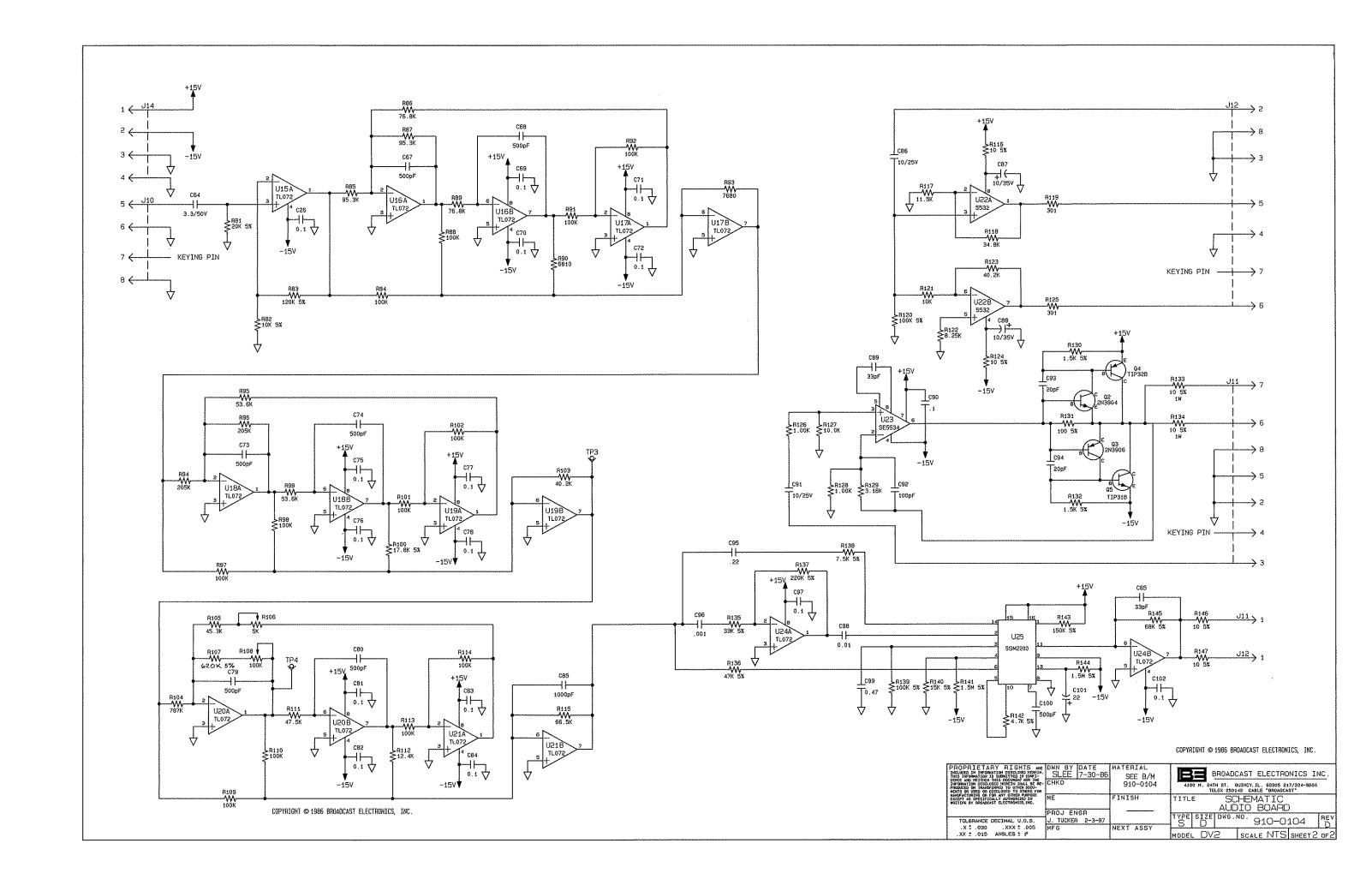
FIGURE	TITLE	NUMBER
7-1	WIRING DIAGRAM, DV-2A OVERALL	WD900-1000-001
7-2	ASSEMBLY DIAGRAM, DV-2A OVERALL	AD900-1000-001
7-3	SCHEMATIC DIAGRAM, AUDIO CIRCUIT BOARD	SD910-0104
7-4	ASSEMBLY DIAGRAM, AUDIO CIRCUIT BOARD	AD910-0104
7-5	SCHEMATIC DIAGRAM, CPU CIRCUIT BOARD	SD910-0102
7-6	ASSEMBLY DIAGRAM, CPU CIRCUIT BOARD	AD910-0102
7-7	SCHEMATIC DIAGRAM, MEMORY CIRCUIT BOARD	SD910-0038
7-8	ASSEMBLY DIAGRAM, MEMORY CIRCUIT BOARD	AD910-0038
7-9	SCHEMATIC DIAGRAM, FRONT PANEL CIRCUIT BOARD	SC910-0101
7-10	ASSEMBLY DIAGRAM, FRONT PANEL CIRCUIT BOARD	AB910-0101
7-11	SCHEMATIC DIAGRAM, POWER SUPPLY CIRCUIT BOARD	SB910-0105
7-12	ASSEMBLY DIAGRAM, POWER SUPPLY CIRCUIT BOARD	AC910-0105

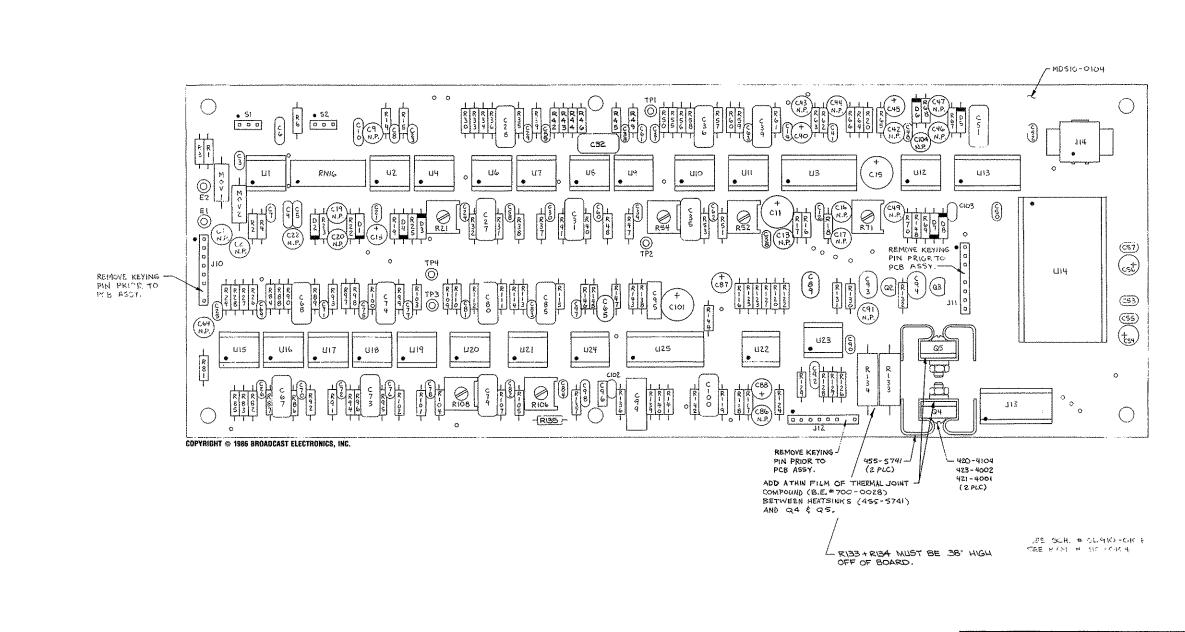






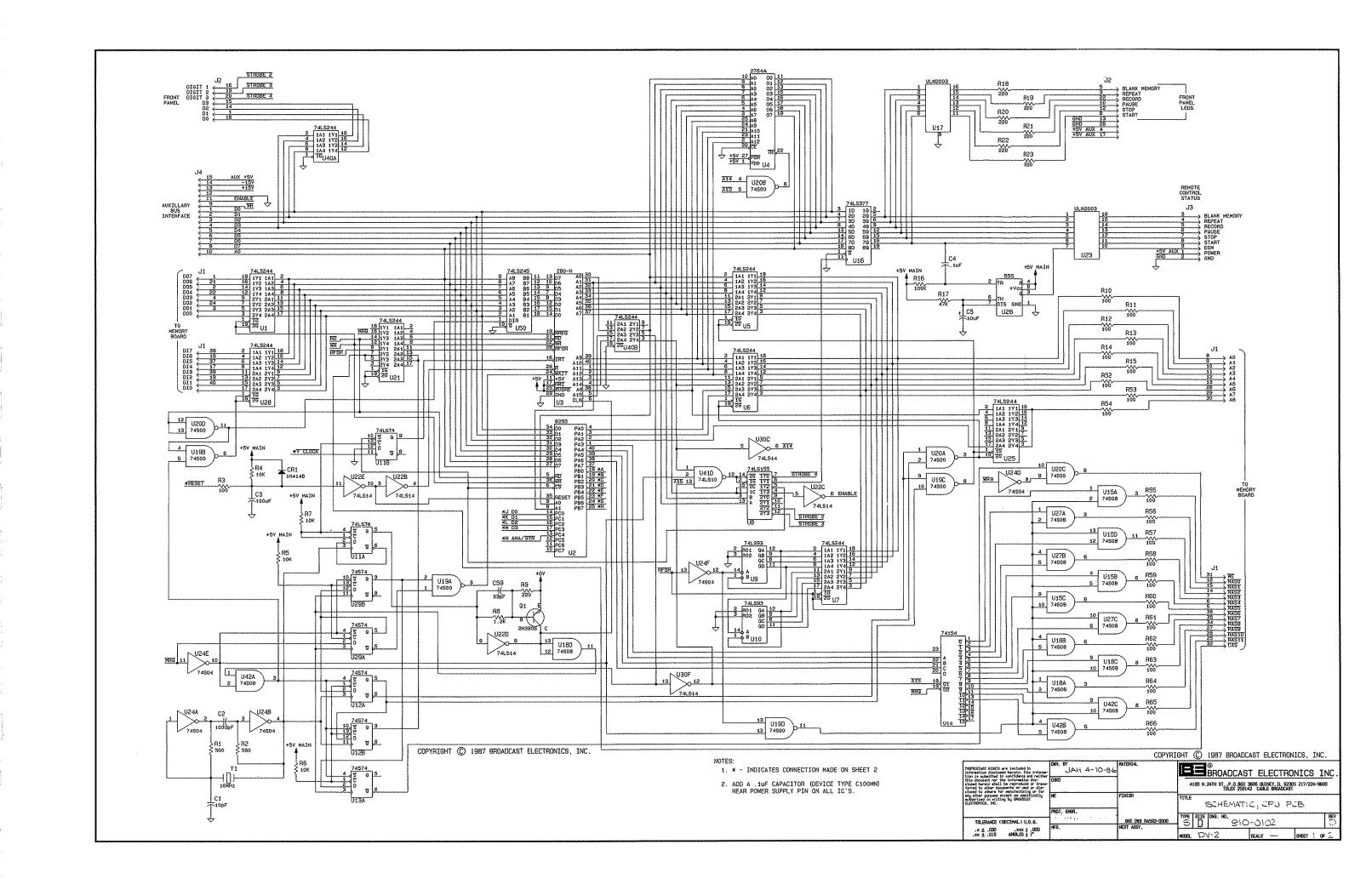


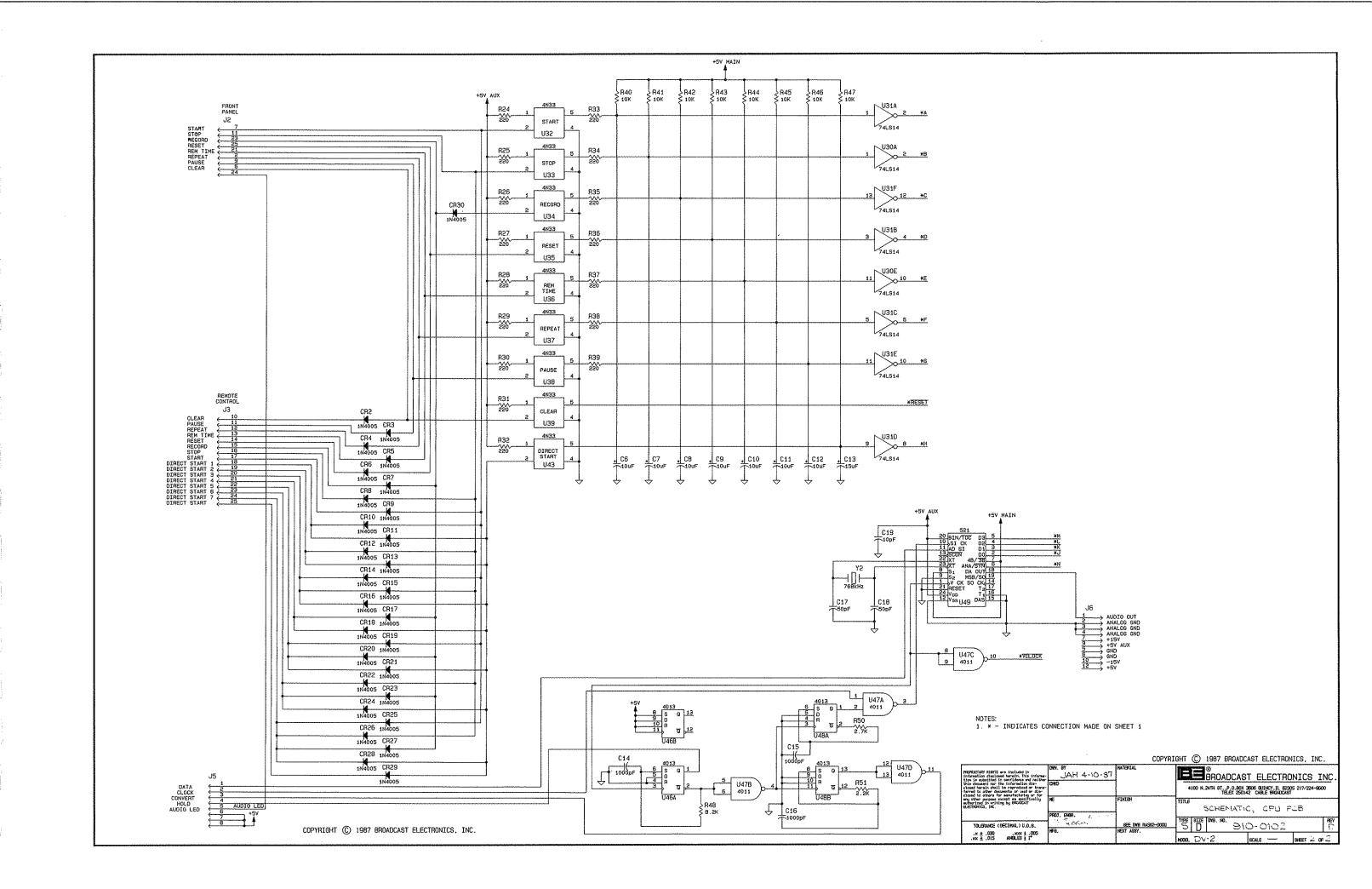


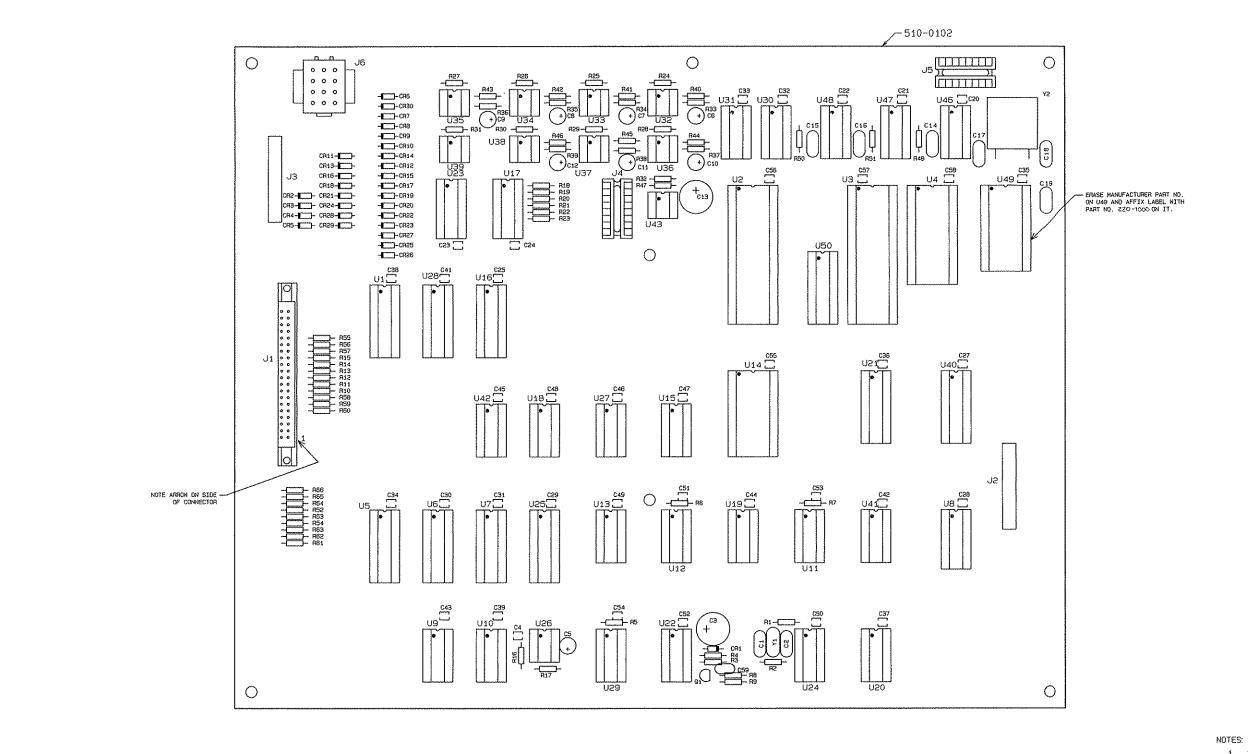


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closed to others for manufacturing or for any other purpose except as specifically authorized in writing by BROADCAST ELECTRONICS, INC.	ME PROJ. ENGR.	FINISH	MILE L'E VOIENT
TOLERANCE (DECIMAL) U.O.S. x ± .030 xxx ± .005	. かん. ころ・** MFG.	SEE DWG RAS92-0000 NEXT ASSY,	TYPE SIZE DWG. NO. 910-0104 F
.xx ± .015 ANGLES ± 1°			MODEL SYL SCALE 2 / SHEET 1 OF



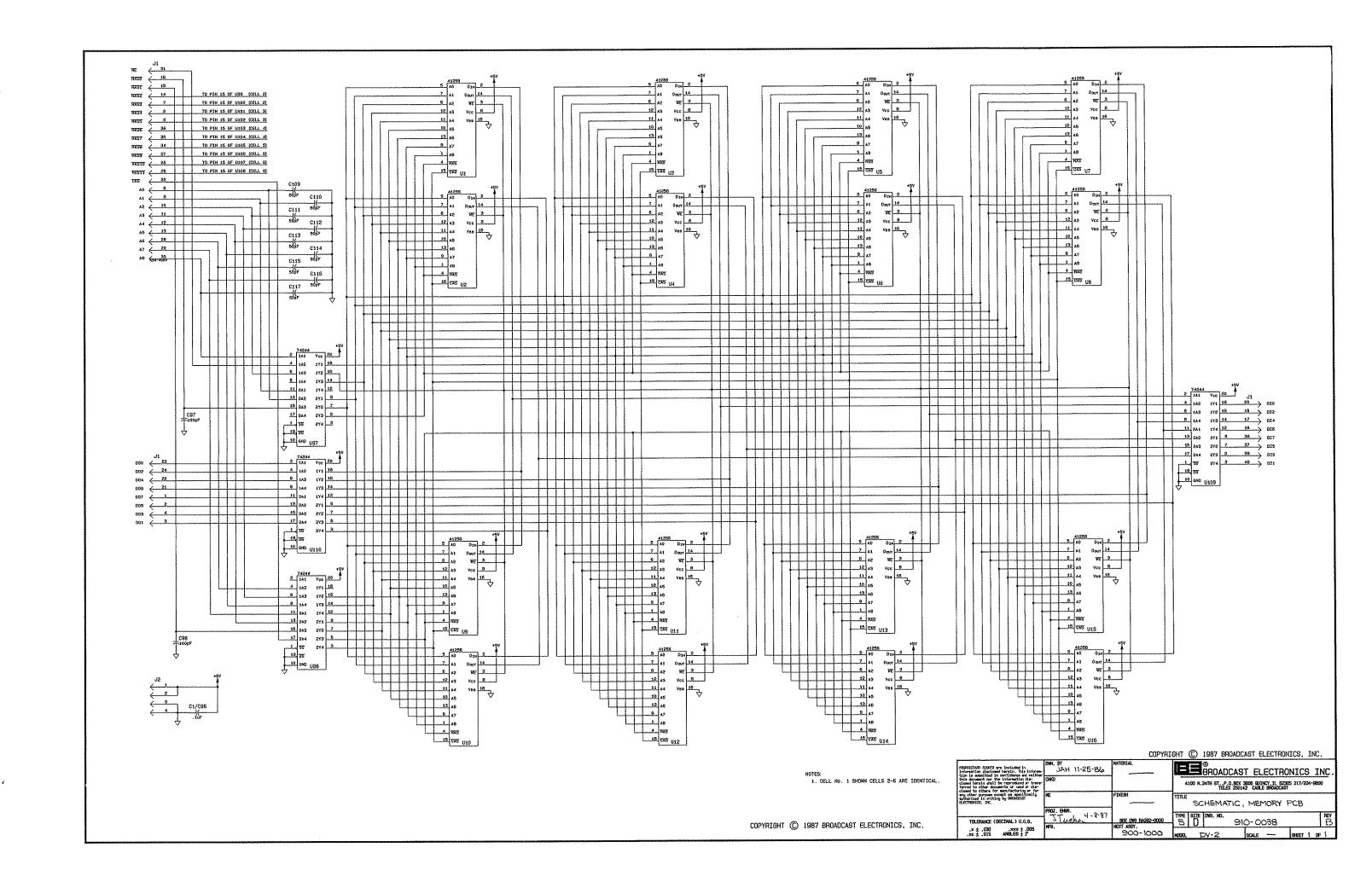


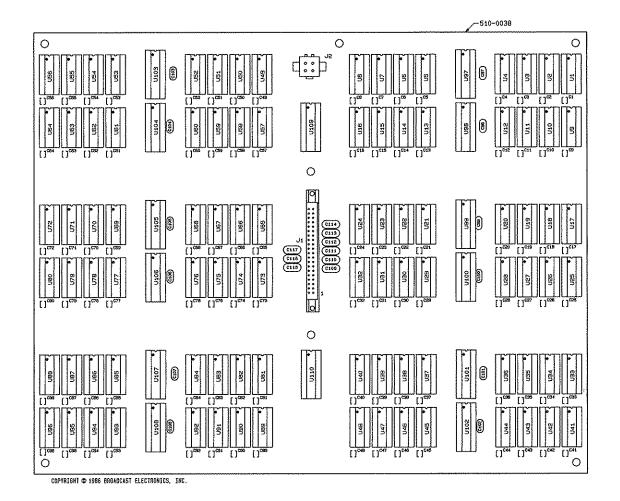


1. SEE SCHEMATIC NO. SD910-0102.

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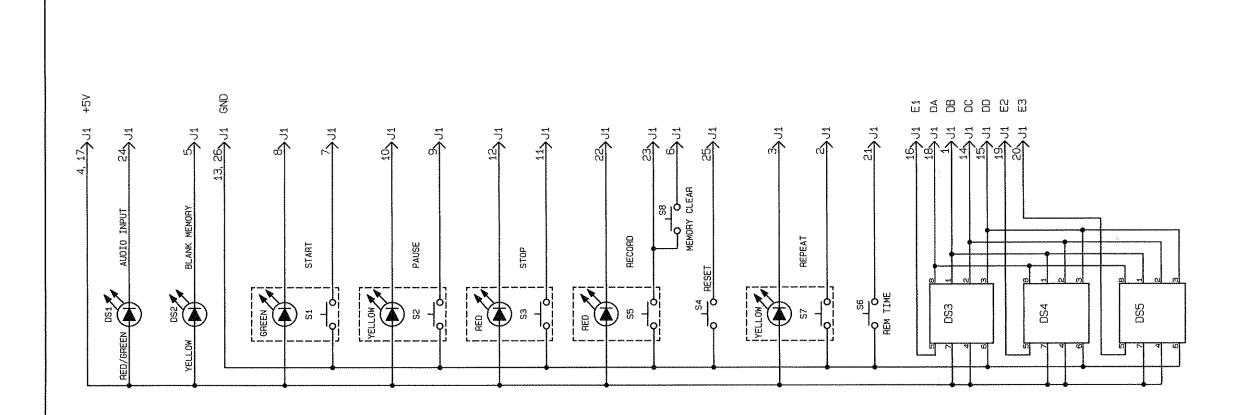
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TOLERANCE DECIMAL U.O.S.	##09 ENSH ##6 2 * -7	NEXT ASSY	TYPE SIZE DWG.NO. 910-0102 REV MODEL DV-2 SCALE1.5/1 SHEET 1 OF 1





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NAME ACTUALING OR FOR ANY OTHER PURPOSE EXCEPT AS SPECIFICALLY AUTHORIZED IN MRITING BY BROADCAST ELECTRONICS, INC.	иЕ	FINISH	TITLE PCB ASSEMBLY
***************************************	PHON ENCH		MEMORY BOARD TYPE SIZE DWG.NO REV
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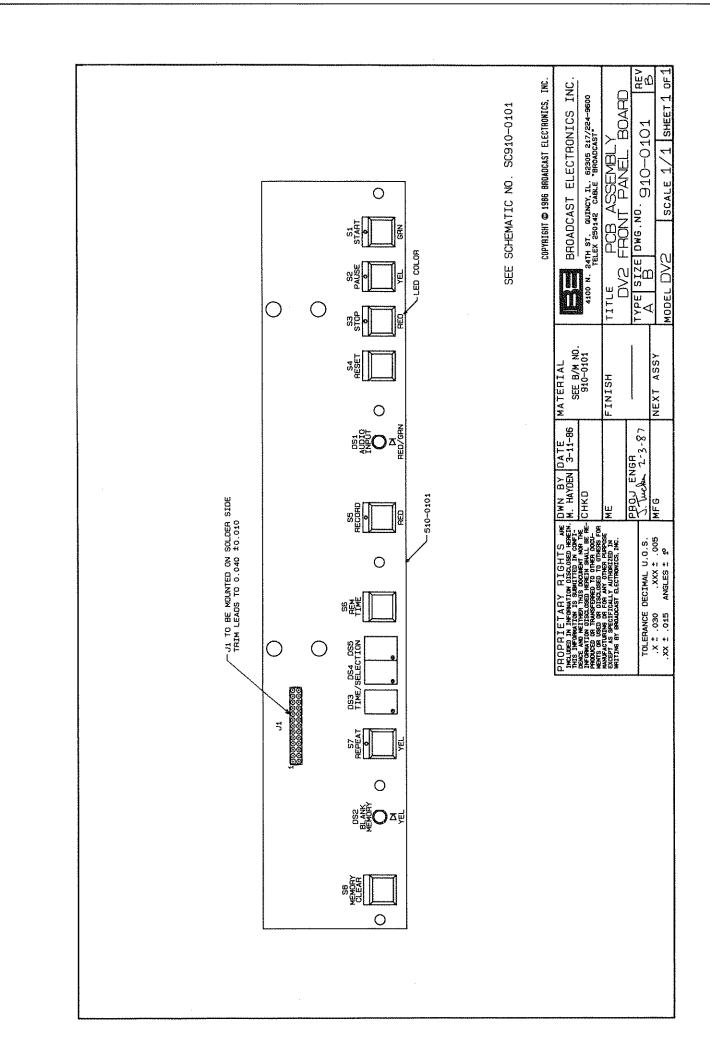


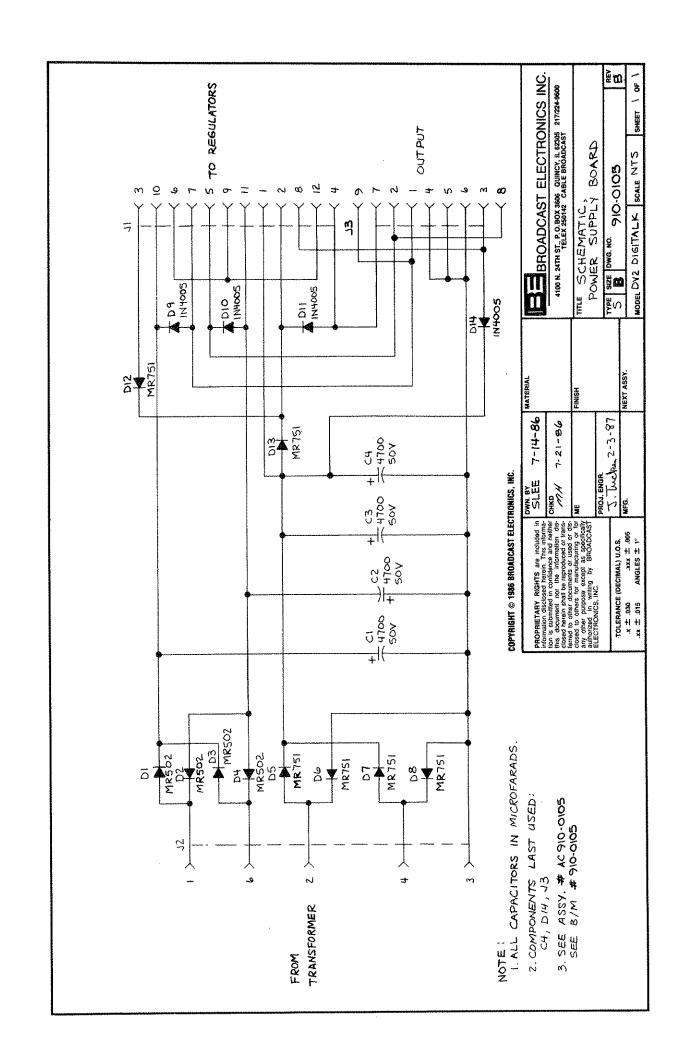
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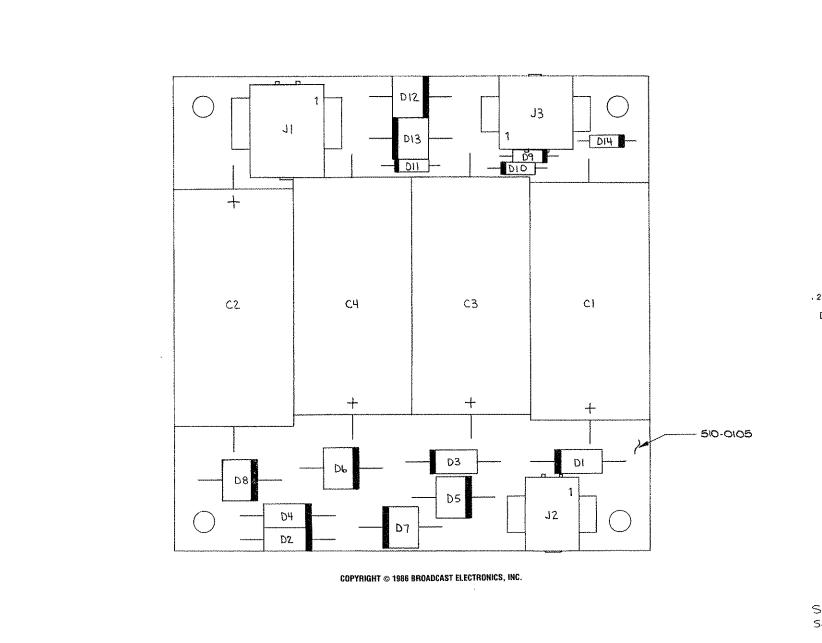
- ALL RESISTORS IN OHMS, 1/4W, 5%: ALL CAPACITORS IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.
- 2. LAST COMPONENTS USED: DS5, J1, S8
- 3. SEE PCB ASSEMBLY AB910-0101

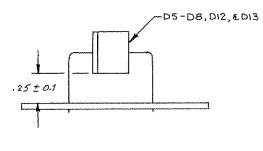
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SEE SCHEMATIC # SB 910-0105 SEE B/M # 910-0105

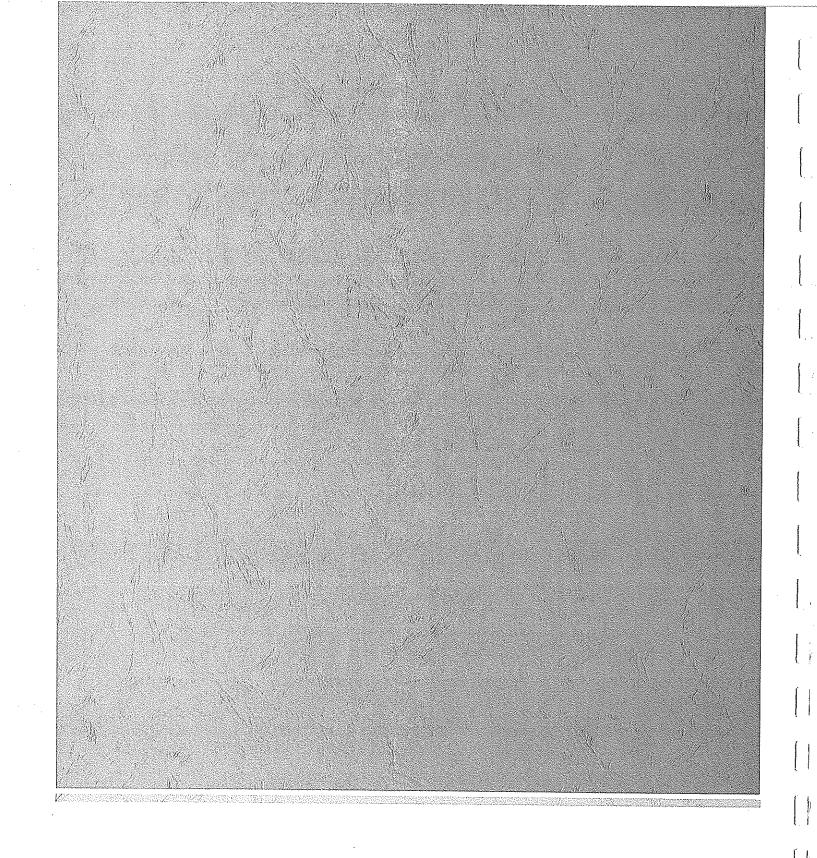
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APPENDIX A MANUFACTURERS DATA

A-1. INTRODUCTION.

- A-2. This appendix provides technical data associated with the maintenance of the DV-2A digital audio recorder. The information contained in this appendix is presented in the following order.
 - A. Technical Information, Zilog Central Processing Unit, 780.
 - B. Technical Information, Signetics Programmable Analog Compandor, NE572.
 - C. Technical Information, Intel Programmable Communication Interface, 8255A.
 - D. Technical Information, Motorola 256K-Bit Dynamic RAM, MCM6256AP.
 - E. Technical Information, CRL Dynafex Noise Reduction System, CRL2200.



MASTER COPY

Z80° CPU Contral Processing Unit



Product Specification

Features

- The instruction set contains 158 instructions. The 78 instructions of the 8080A are included as a subset; 8080A software compatibility is maintained.
- Six MHz, 4 MHz and 2.5 MHz clocks for the Z80B, Z80A, and Z80 CPU result in rapid instruction execution with consequent high data throughput.
- The extensive instruction set includes string, bit, byte, and word operations. Block searches and block transfers together with indexed and relative addressing result in the most powerful data handling capabilities in the microcomputer industry.
- The Z80 microprocessors and associated family of peripheral controllers are linked by a vectored interrupt system. This system

- may be daisy-chained to allow implementation of a priority interrupt scheme. Little, if any, additional logic is required for daisy-chaining.
- Duplicate sets of both general-purpose and flag registers are provided, easing the design and operation of system software through single-context switching, background-foreground programming, and single-level interrupt processing. In addition, two 16-bit index registers facilitate program processing of tables and arrays,
- There are three modes of high speed interrupt processing: 8080 compatible, non-Z80 peripheral device, and Z80 Family peripheral with or without daisy chain.
- On-chip dynamic memory refresh counter.

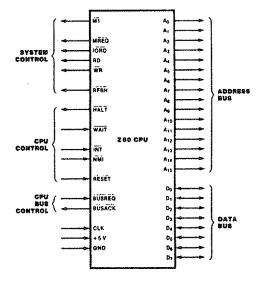


Figure 1. Pin Functions

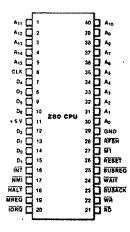


Figure 2. Pin Assignments

General Description

The Z80, Z80A, and Z80B CPUs are thirdgeneration single-chip microprocessors with exceptional computational power. They offer higher system throughput and more efficient memory utilization than comparable secondand third-generation microprocessors. The internal registers contain 208 bits of read/write memory that are accessible to the programmer. These registers include two sets of six generalpurpose registers which may be used individually as either 8-bit registers or as 16-bit register pairs. In addition, there are two sets of accumulator and flag registers. A group of "Exchange" instructions makes either set of main or alternate registers accessible to the programmer. The alternate set allows operation in foreground-background mode or it may

be reserved for very fast interrupt response.

The Z80 also contains a Stack Pointer, Program Counter, two index registers, a Refresh register (counter), and an Interrupt register. The CPU is easy to incorporate into a system since it requires only a single +5 V power source, all output signals are fully decoded and timed to control standard memory or peripheral circuits, and is supported by an extensive family of peripheral controllers. The internal block diagram (Figure 3) shows the primary functions of the Z80 processors. Subsequent text provides more detail on the Z80 I/O controller family, registers, instruction set, interrupts and daisy chaining, and CPU timing.

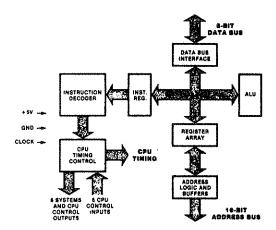


Figure 3. Z80 CPU Block Diagram

PROGRAMMABLE ANALOG COMPANDOR

NE572

DESCRIPTION

The NE572 is a dual channel, high performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full wave rectifier to detect the average value of input signal; a linearized, temperature compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The NE572 is intended for noise reduction in high performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

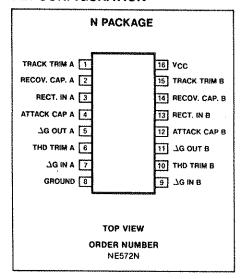
FEATURES

- Independent control of attack and recovery time.
- Improved low frequency gain control ripple
- Complementary gain compression and expansion with external Op Amp
- Wide dynamic range—greater than 110dB
- Temperature compensated gain control
- Low distortion gain ceil
- Low noise 6μV typical
- Wide supply voltage range—6V-22V
- System level adjustable with external components.

APPLICATIONS

- Dynamic noise reduction system
- Voltage control amplifier
- Stereo expandor
- Automatic level control
- High level limiter
- Low level noise gate
- State variable filter

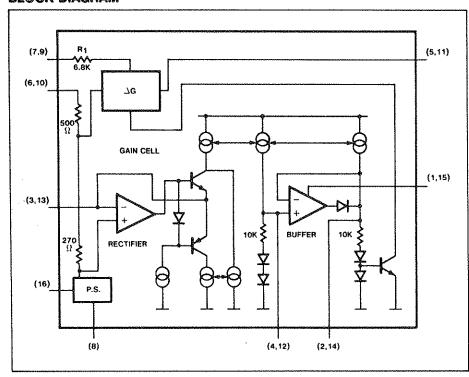
PIN CONFIGURATION



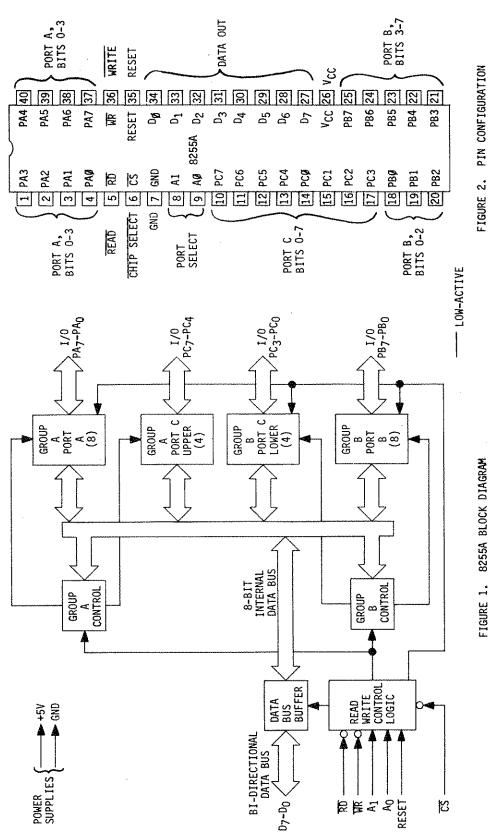
ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
VCC	Supply voltage	22	VDC
TA	Operating temperature range	0 to 70	°C
PD	Power dissipation	500	mW

BLOCK DIAGRAM



15



8255A BLOCK DIAGRAM FIGURE 1.

The Intel 8255A is a general purpose programmable I/O device designed for use with Intel microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE O), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE I, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

597-0036-30

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Advance Information

256K-Bit Dynamic RAM

The MCM6256AP is a 262,144 bit, high-speed, dynamic Random Access Memory. Organized as 262,144 one-bit words and fabricated using N-channel silicon-gate MOS technology, this new single +5 volt supply dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row and column address inputs, the MCM6256AP requires only nine address lines and permits packaging in standard 16-pin 300 mil wide dual-in-line packages. Complete address decoding is done on-chip with address latches incorporated. Data out (Q) is controlled by CAS allowing greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM6256AP incorporates a one transistor cell design and dynamic storage techniques.

The MCM6256AP features "page mode" which allows random column accesses of the 512 bits within the selected row.

- Organized as 262,144 Words of 1 Bit
- Single +5 Volt Operation (±10%)
- Maximum Access Time: MCM6256AP12 = 120 ns

MCM6256AP15 = 150 ns

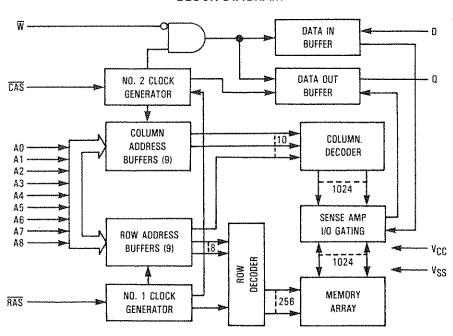
● Low Power Dissipation: MCM6256AP12—330 mW Maximum (Active)

MCM6256AP15-275 mW Maximum (Active)

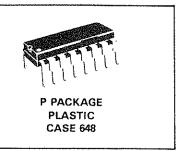
28 mW Maximum (Standby)

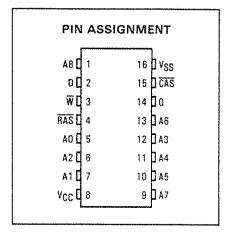
- Three-State Data Output
- Early-Write Common I/O Capability
- 9 256 Cycle, 4 ms Refresh
- RAS-Only Refresh Mode
- Page Mode Capability

BLOCK DIAGRAM



MCM6256AP





PIN NAMES			
A0-A8 Address Input			
D Data In			
Q Data Out			
W Read/Write Input			
RAS Row Address Strobe			
CAS Column Address Strobe			
V _{CC} Power (+5 V)			
Vss Ground			

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This document contains information on a new product. Specifications and information herein are subject to change without notice.



Circuit Research Labs. Inc

DYNAFEX® NOISE REDUCTION SYSTEM

DESCRIPTION

The CRL 2200 is a patented single-channel noise reduction system utilizing the proprietary Dynafex® circuitry from Circuit Research Labs., Inc. The monolithic device provides up to 30 dB of noise reduction without the encode/decode process and can be used to eliminate noise from virtually any audio source.

The circuit incorporates dynamically variable bandwidth limiting and a unique type of downward expansion. The bandwidth limiting portion continuously analyzes and responds to frequency content of the input signal, while the expander section analyzes and responds to signal amplitude. By utilizing these two types of noise reduction simultaneously, a greater amount of noise reduction can be realized than in typical dynamic filtering schemes. By being a single-ended system, the Dynafex circuitry provides a much wider range of applications than a companding type device.

FEATURES

- Up to 30 dB of Noise Reduction
- Useful on any Audio Signal
- Dynamic Range of 110 dB
- THD of 0.04%
- Operates from ± 12 to ± 18 Volts

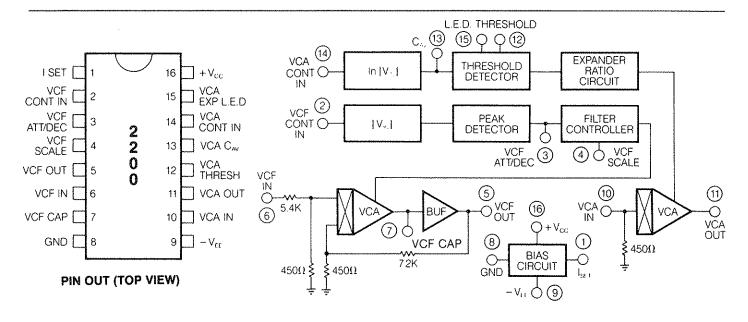
Complete Control of all Filter Parameters

- Adjustable Filter Attack and Release Time
- Adjustable Expander Section Response Time
- Control Over VCA Shut-Down Level
- Downward Expansion Indicator Output

APPLICATIONS

- Studio and Sound Reinforcement Mixing Consoles
- Audio and Video Tape Recorders
- Digital Signal Processing
- Motion Picture Equipment
- High-End Consumer Hi-Fi Systems

- Telecommunications Systems
- Two-Way Radio
- Cable Television Operations
- Video and Audio Tape Duplication
- Electronic Musical Instruments



^{*}CRL 2200, formerly SSM 2200 from Solid State Micro Technology for Music, Inc. Dynafex is a registered trademark of Circuit Research Labs., Inc.

Dynafex is a registered trademark of Circuit Research Labs., Inc Japanese and other international patents pending. Rev. July 1986

PRODUCT WARRANTY

LIMITED ONE YEAR

While this warranty gives you specific legal rights, which terminate one (1) year (6 months on turntable motors) from the date of shipment, you may also have other rights which vary from state to state.

Broadcast Electronics, Inc. ("BE"), 4100 North 24th Street, P. O. Box 3606, Quincy, Illinois 62305, hereby warrants cartridge machines, consoles, transmitters and other new Equipment manufactured by BE against any defects in material or workmanship at the time of delivery thereof, that develop under normal use within a period of one (1) year (6 months for turntable motors) from the date of shipment. Other manufacturers' Equipment, if any, shall carry only such manufacturers' standard warranty. This warranty extends to the original user and any subsequent purchaser during the warranty period. BE's sole responsibility with respect to any Equipment or parts not conforming to this warranty is to replace such equipment or parts upon the return thereof F.O.B. BE's factory or authorized repair depot within the period aforesaid.

In the event of replacement pursuant to the foregoing warranty, only the unexpired portion of the warranty from the time of the original purchase will remain in effect for any such replacement. However, the warranty period will be extended for the length of time that the original user is without the services of the Equipment due to its being serviced pursuant to this warranty. The terms of the foregoing warranty shall be null and void if the Equipment has been altered or repaired without specific written authorization of BE, or if Equipment is operated under environmental conditions or circumstances other than those specifically described in BE's product literature or instruction manual which accompany the Equipment purchased. BE shall not be liable for any expense of any nature whatsoever incurred by the original user without prior written consent of BE.

BE shall not be liable to the original user for any and all incidental or consequential damages for breach of either expressed or implied warranties. However, some states do not allow the exclusion or limitation of incidental or consequential damages, so the above limitation or exclusion may not apply to you. All express and implied warranties shall terminate at the conclusion of the period set forth herein.

Except as set forth herein, and except as to title, there are no warranties, or any affirmations of fact or promises by BE, with reference to the Equipment, or to merchantability, fitness for a particular application, signal coverage, infringement, or otherwise, which extend beyond the description of the Equipment in BE's product literature or instruction manual which accompany the Equipment. Any card which is enclosed with the Equipment will be used by BE for survey purposes only.

BROADCAST ELECTRONICS, INC. 4100 North 24th Street, P. O. Box 3606, Quincy, Illinois 62305